設計技術から見た
半導体集積回路の省電力技術

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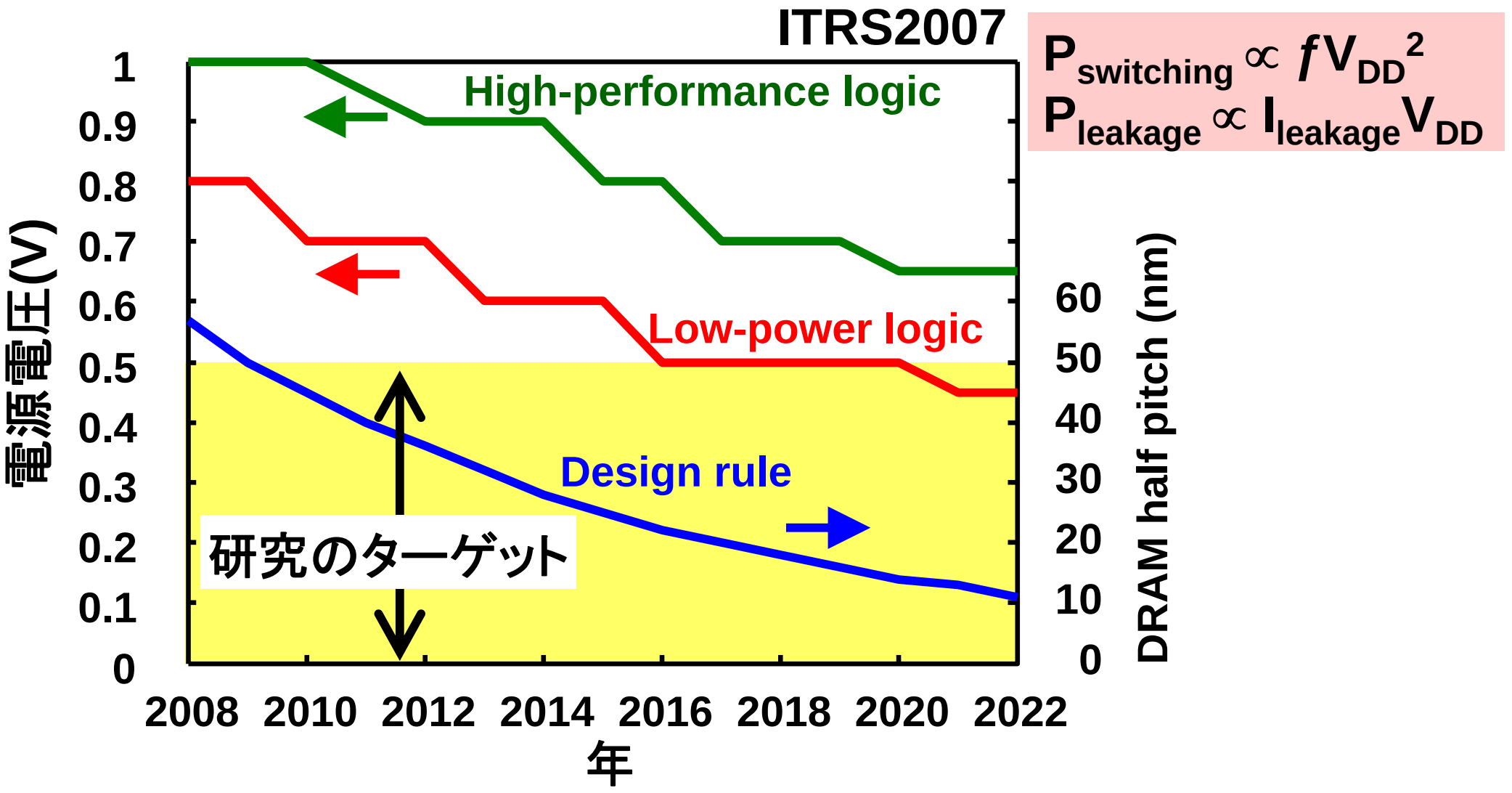
高宮　真

Outline

- 低電力設計技術の動向
  (1)低電圧、(2)細粒度制御、(3)3次元
- ロジック回路の電源電圧の下限(V_{DDmin})
- 細粒度基板バイアス制御による低電力化
- 3次元SSDのNANDフラッシュ向け昇圧回路による低電力化

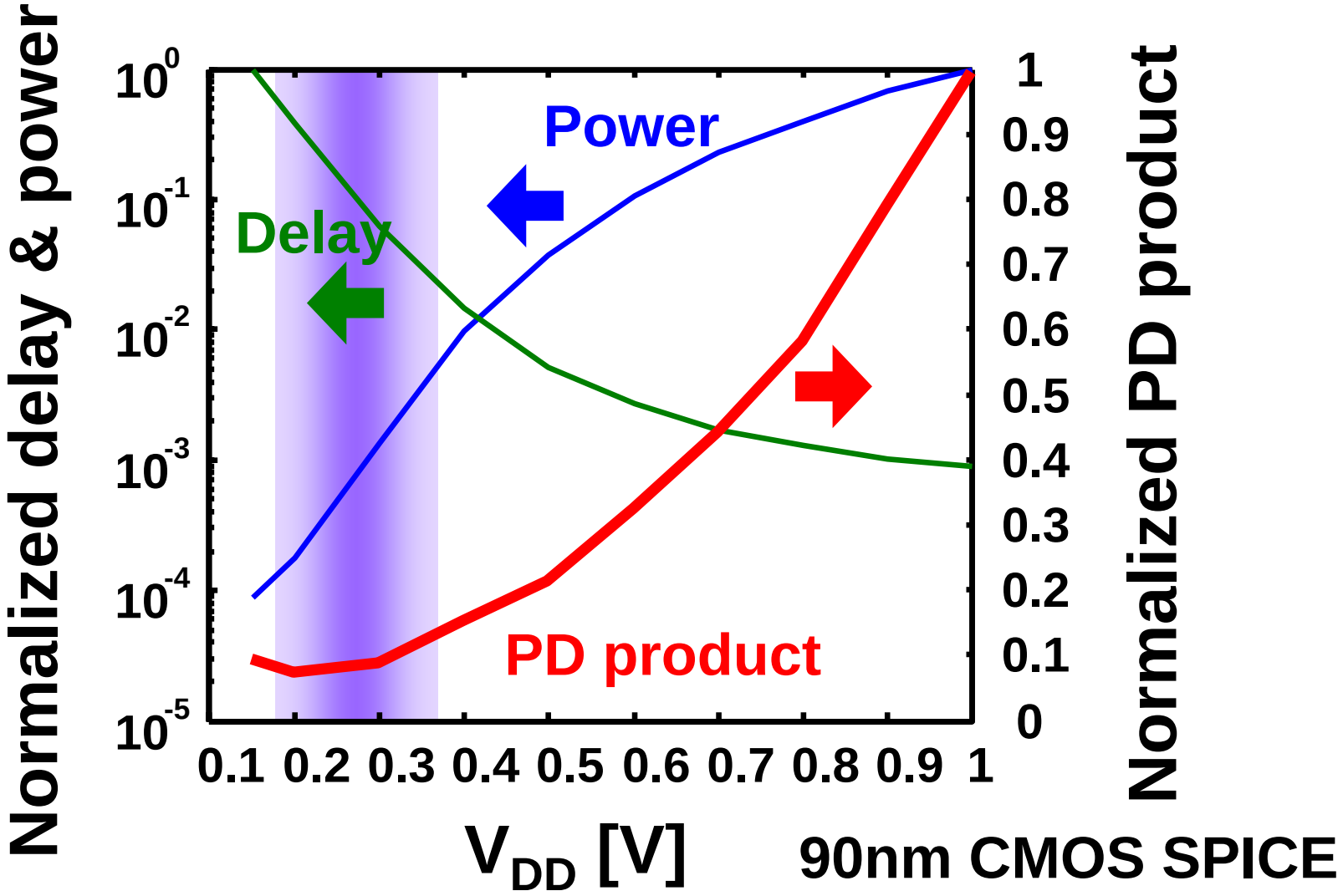
(SSD: Solid State Drive)

電源電圧(V_{DD})の低減の必要性



■ 90nm→65nm→45nmとV_{DD}=1Vが続いたが、
今後は電力と信頼性の観点から、V_{DD}の低減が必須

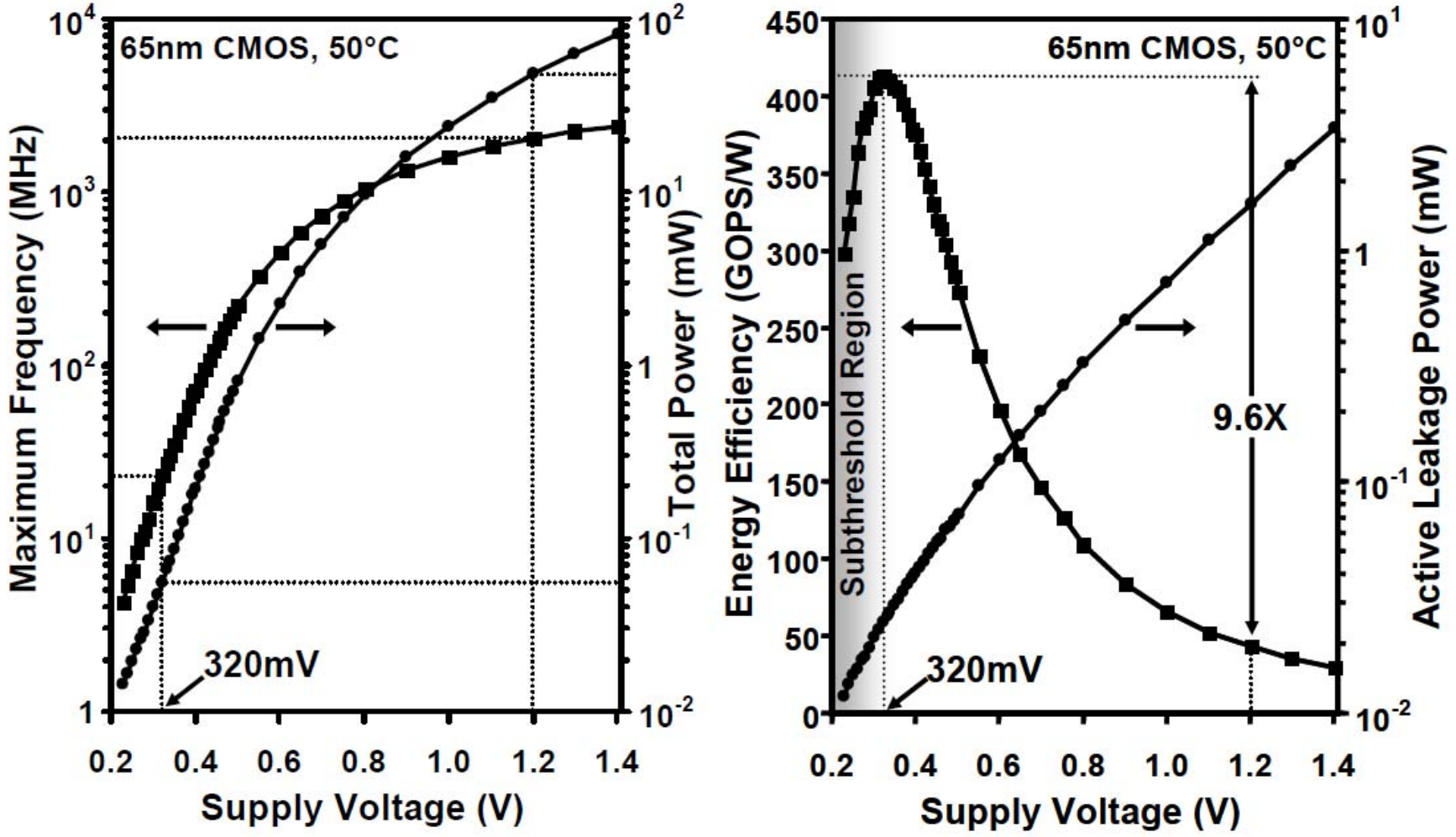
エネルギー効率最適は低V_{DD}で実現



◆ Power, Delay積(PD積=エネルギー)はV_{DD}=0.2-0.3Vで最小
→速度が問われないアプリでは低V_{DD}がenergy efficient

Energy Efficientな超低V_{DD}ロジック

■超低V_{DD}ロジックに関する初めての企業(Intel)からの報告

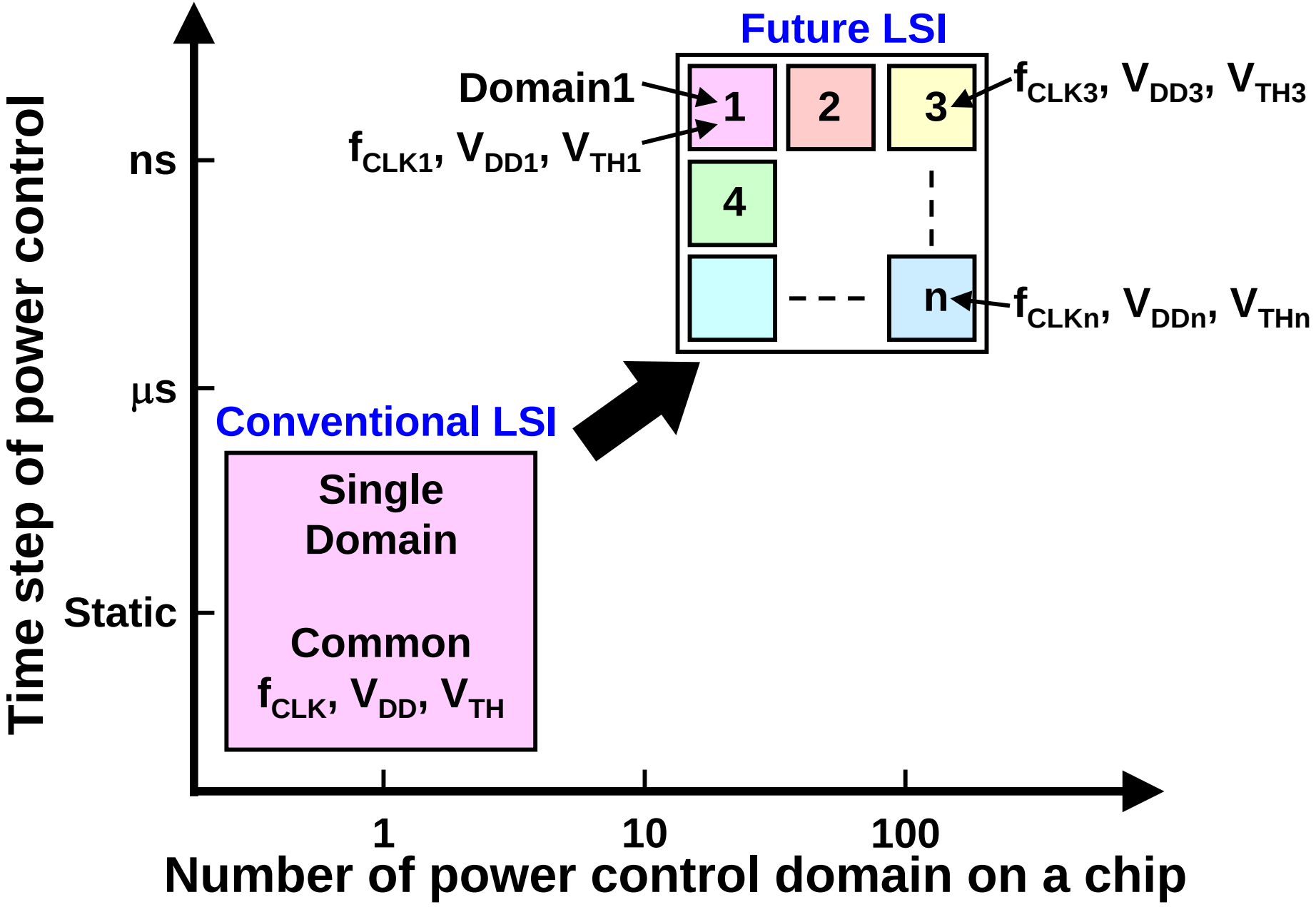


■ V_{DD}=230mVまで動作はするが、320mVがエネルギー効率最高

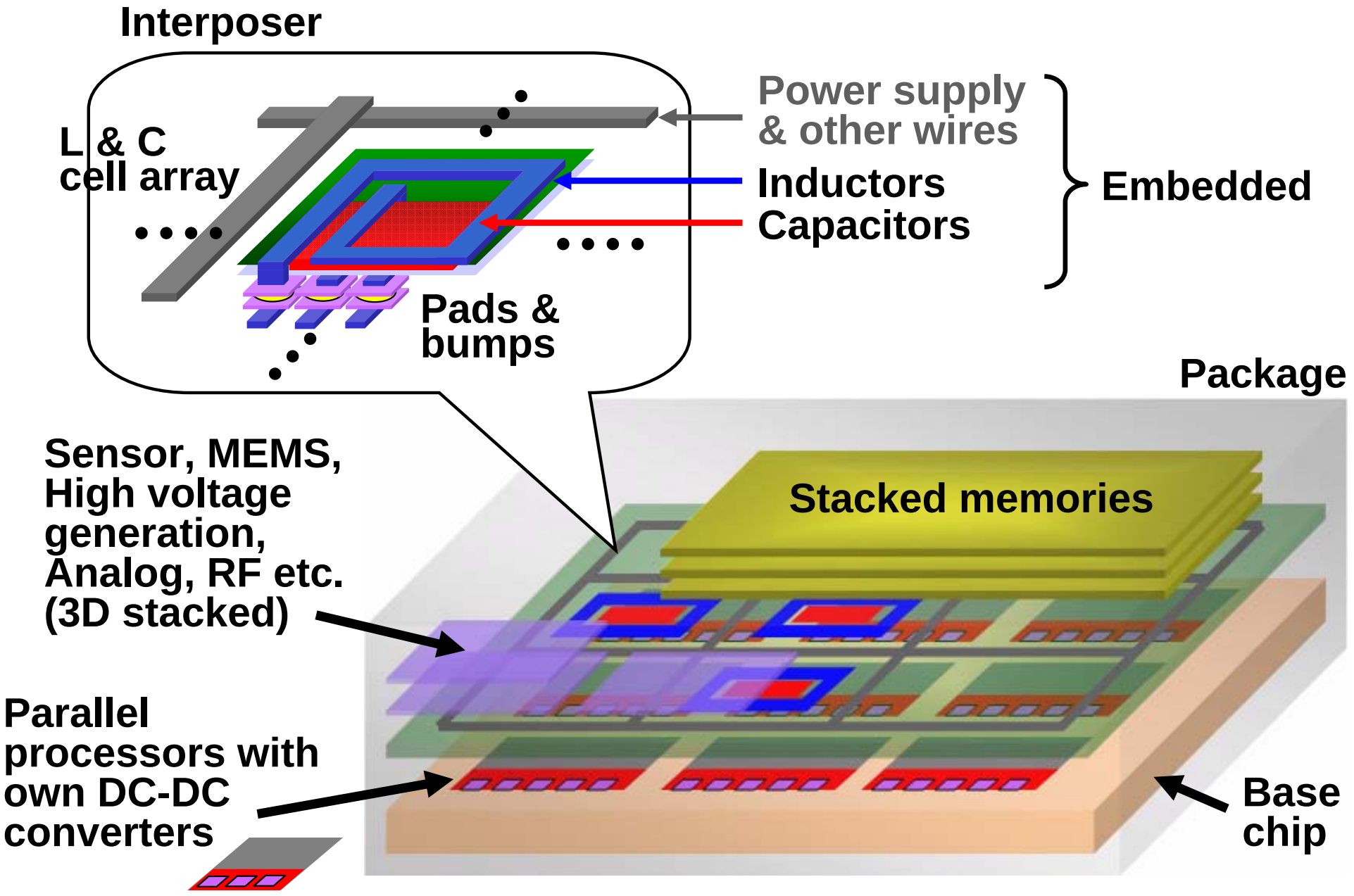
H. Kaul, M. Anders, S. Mathew, S. Hsu, A. Agarwal, R. Krishnamurthy, and S. Borkar, "A 320mV 56μW 411GOPS/Watt ultra-low voltage motion estimation accelerator in 65nm CMOS," IEEE ISSCC, pp. 316-317, Feb. 2008.

時空間の細粒度電圧制御がトレンド

近年の低電力VLSI回路技術の方向性



細粒度制御には3次元技術との連携が必須



細粒度と3次元に対する我々の取り組み

- 電源電圧の下限(V_{DDmin})の追求
  - チップ内トランジスタばらつき測定[1]
  - ロジック回路のV_{DDmin}[2-3] ← 今回発表
- 空間的細粒度制御
  - 製造後の細粒度基板バイアス制御による低電力化[4] ← 今回発表
  - メニーコア向けテスト手法[5]
  - 3次元積層を用いたオンチップDC-DCコンバータ[6-7]
- 時間的細粒度制御
  - 電源電圧、基板バイアスを高速に変化させる加速回路[8-11]
  - 電源ノイズキャンセル回路[12]
- 3次元集積技術
  - 3次元SSDのNANDフラッシュ向け昇圧回路による低電力化[13] ← 今回発表

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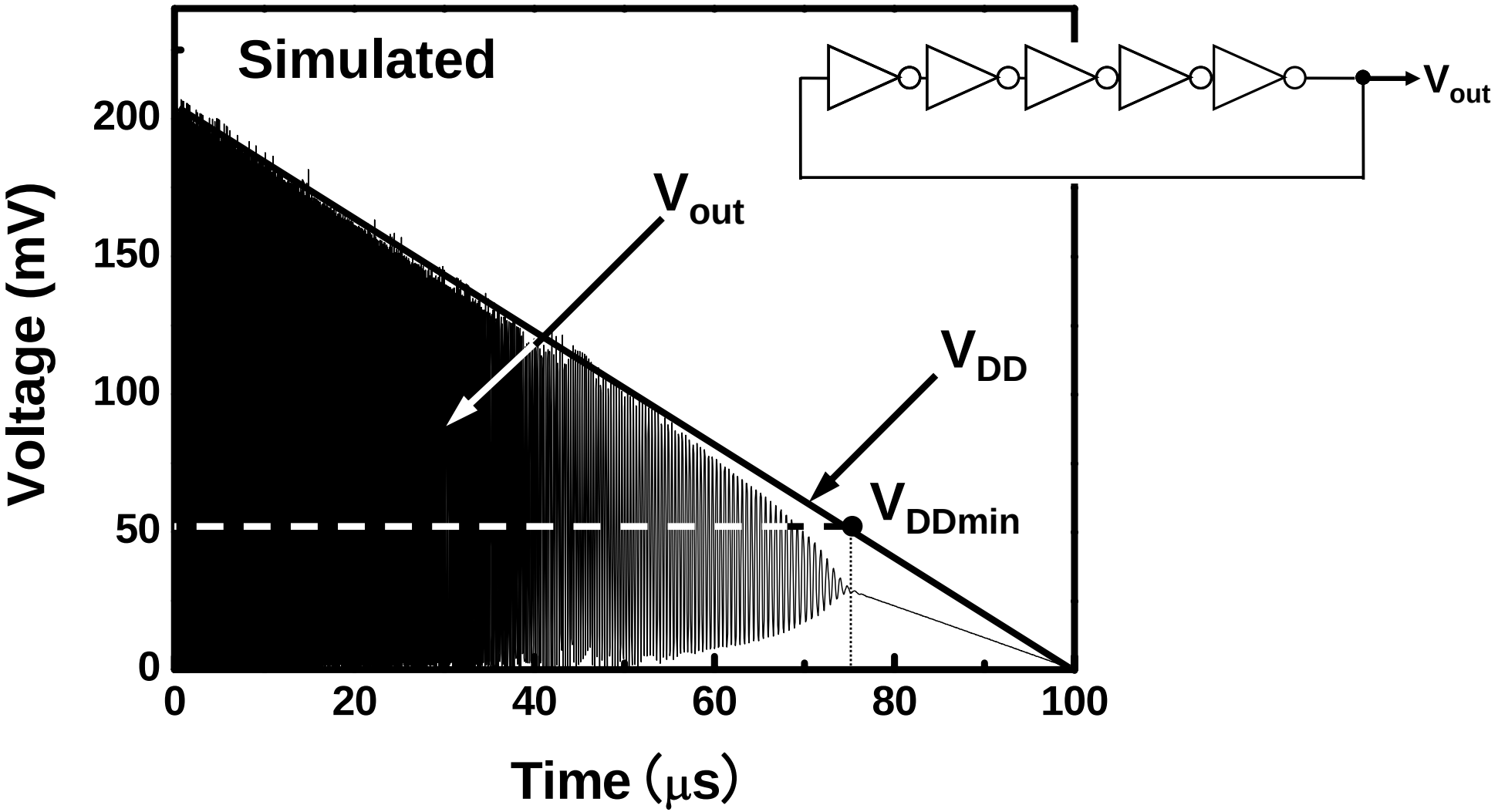
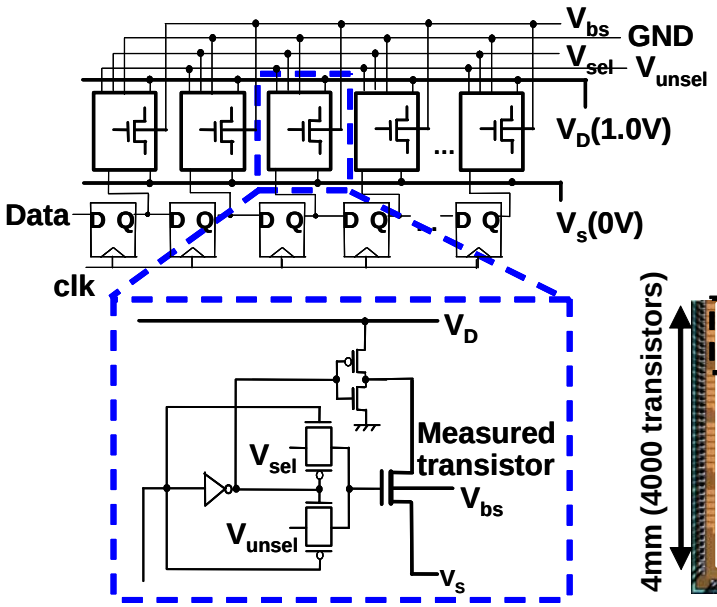
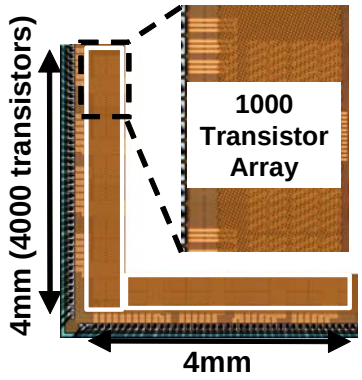
Minimum Operating Voltage (V_{DDmin})



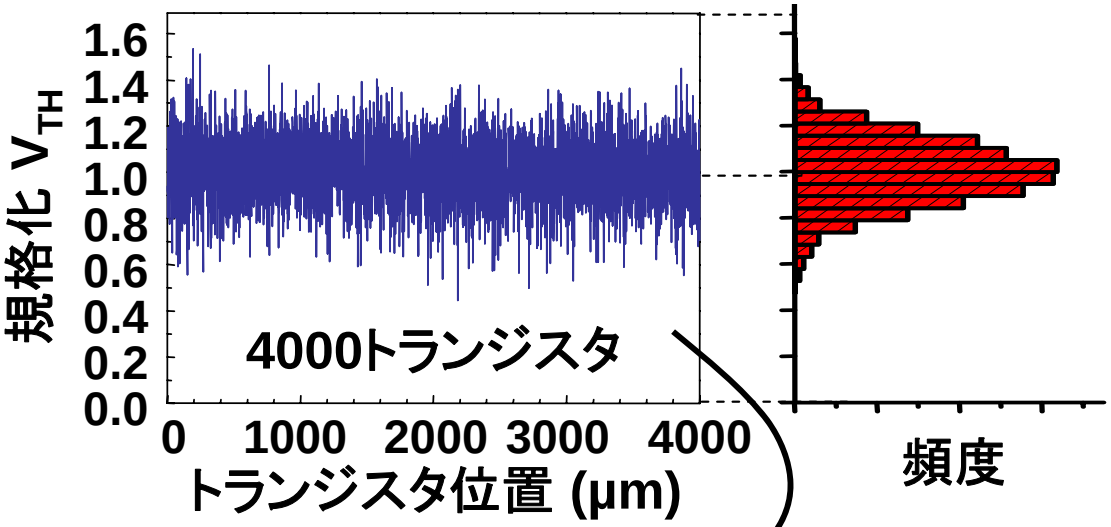
- V_{DDmin} is defined as the supply voltage (V_{DD}) when the RO's stop oscillation.
- RO's are useful V_{DDmin} detectors.

チップ内トランジスタばらつき

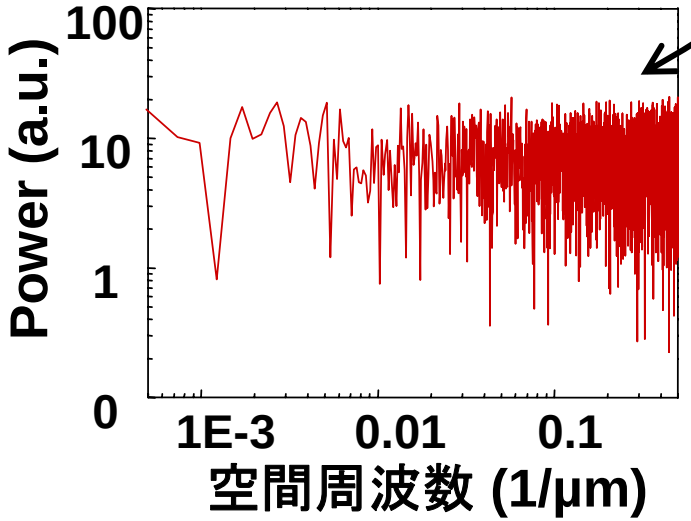




トランジスタばらつき測定回路



フーリエ変換

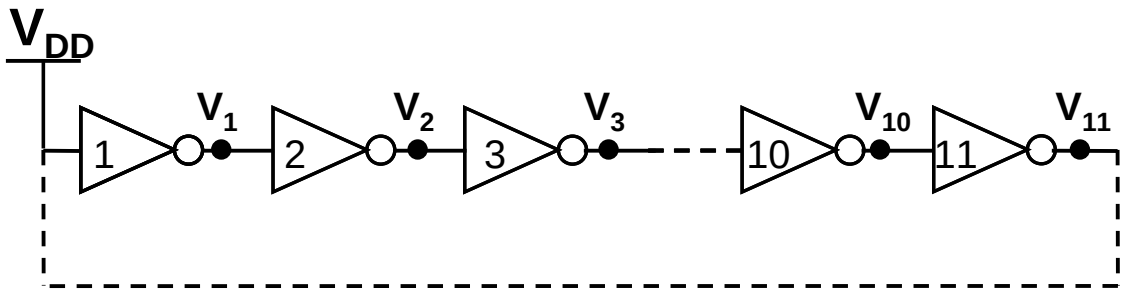


キー技術
(1) 挟ピッチかつ広範囲のTrアレー
(2) 非選択Trのリークカット

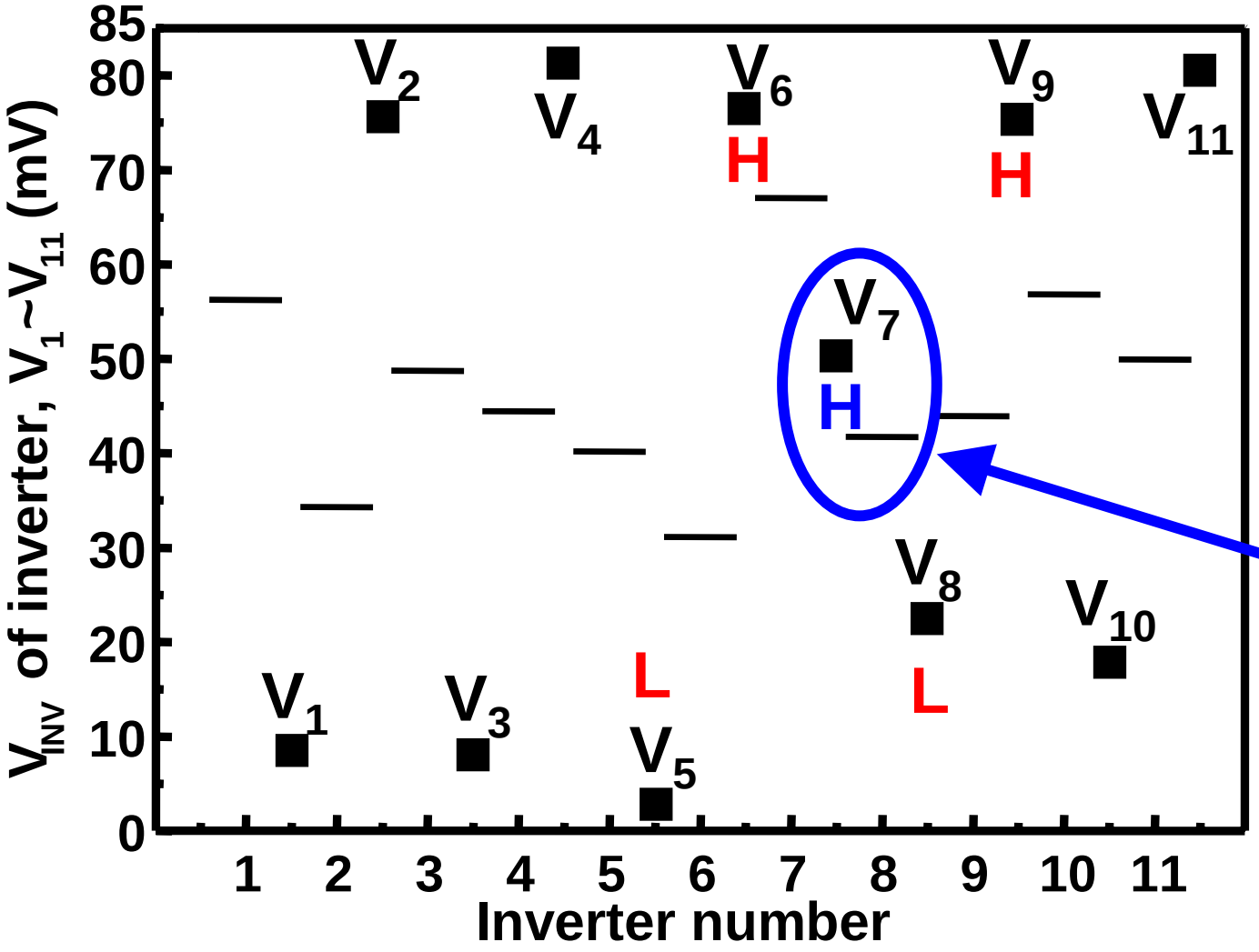
チップ内V_{TH}ばらつきはランダム

◆ チップ内V_{TH}ばらつきは4mmの範囲内でランダム
→細粒度の基板バイアス制御では補償不可

Analysis of Origin of V_{DDmin}



Each transistor has random V_{TH}.



V_{INV} —

V_1~V_{11} ■

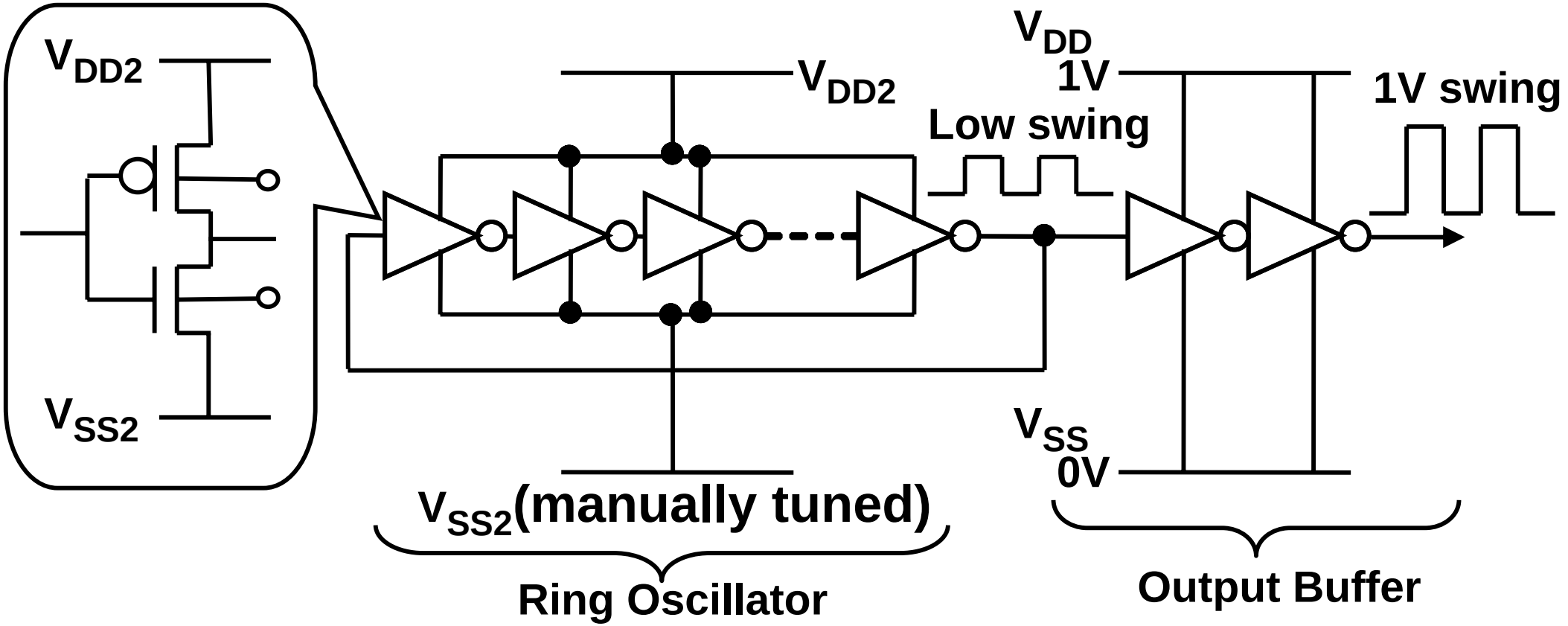
V_{DD}=85mV

Fail

$V_{OUT\_LOW\_7} > V_{INV\_8}$

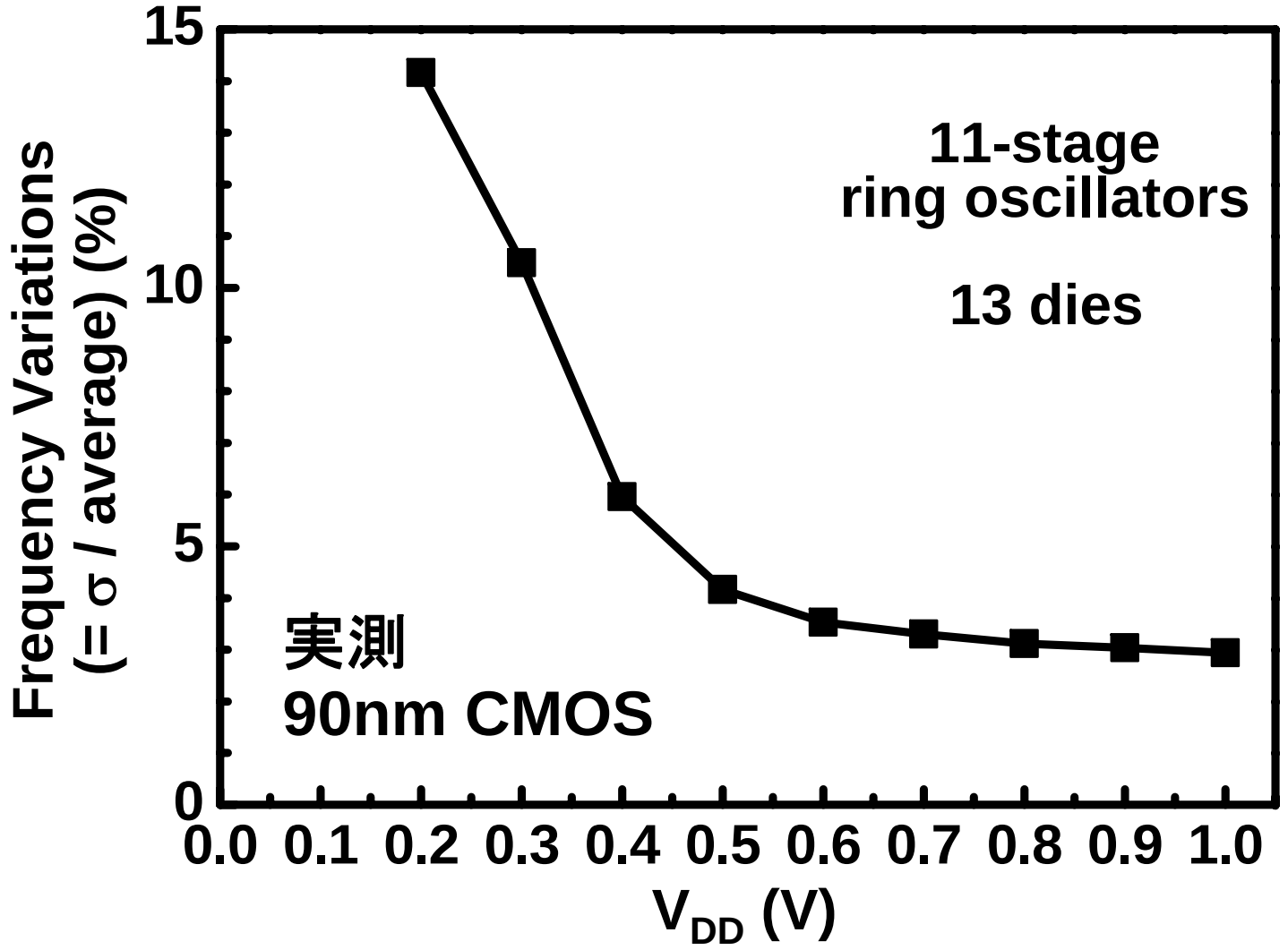
Monte Carlo SPICE

RO Circuits to Enable V_{DDmin} Measurement



- The low swing output of RO is amplified to 1-V swing by the output buffer.

V_{DD} Dependence of Oscillation Frequency variation



$$\Delta t_{pd} = \frac{dt_{pd}}{dV_{TH}} \Delta V_{TH}$$

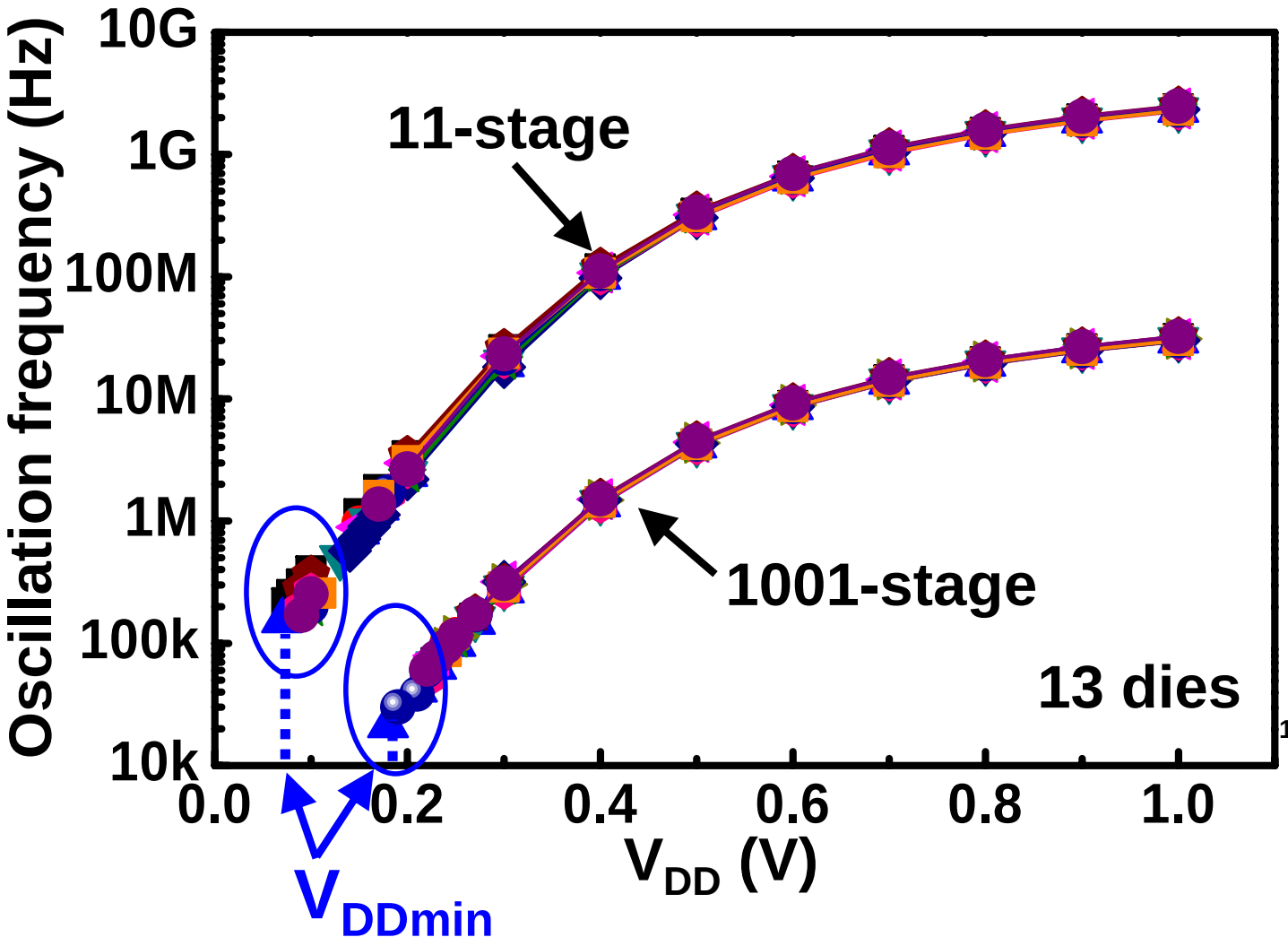
$$t_{pd} \propto \frac{CV_{DD}}{(V_{DD} - V_{TH})^{\alpha}}$$

$$\rightarrow \frac{\Delta t_{pd}}{t_{pd}} \propto \frac{\alpha}{V_{DD} - V_{TH}} \Delta V_{TH}$$

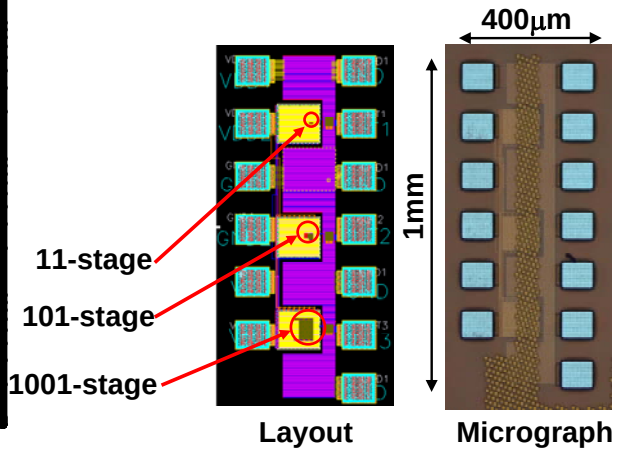
$$\rightarrow \frac{\Delta f}{f} \propto -\frac{\Delta t_{pd}}{t_{pd}} \propto \frac{\alpha}{V_{DD} - V_{TH}} \Delta V_{TH}$$

◆ **Relative frequency variations increases with reduced V_{DD}.**

ゲート遅延のV_{DD}依存

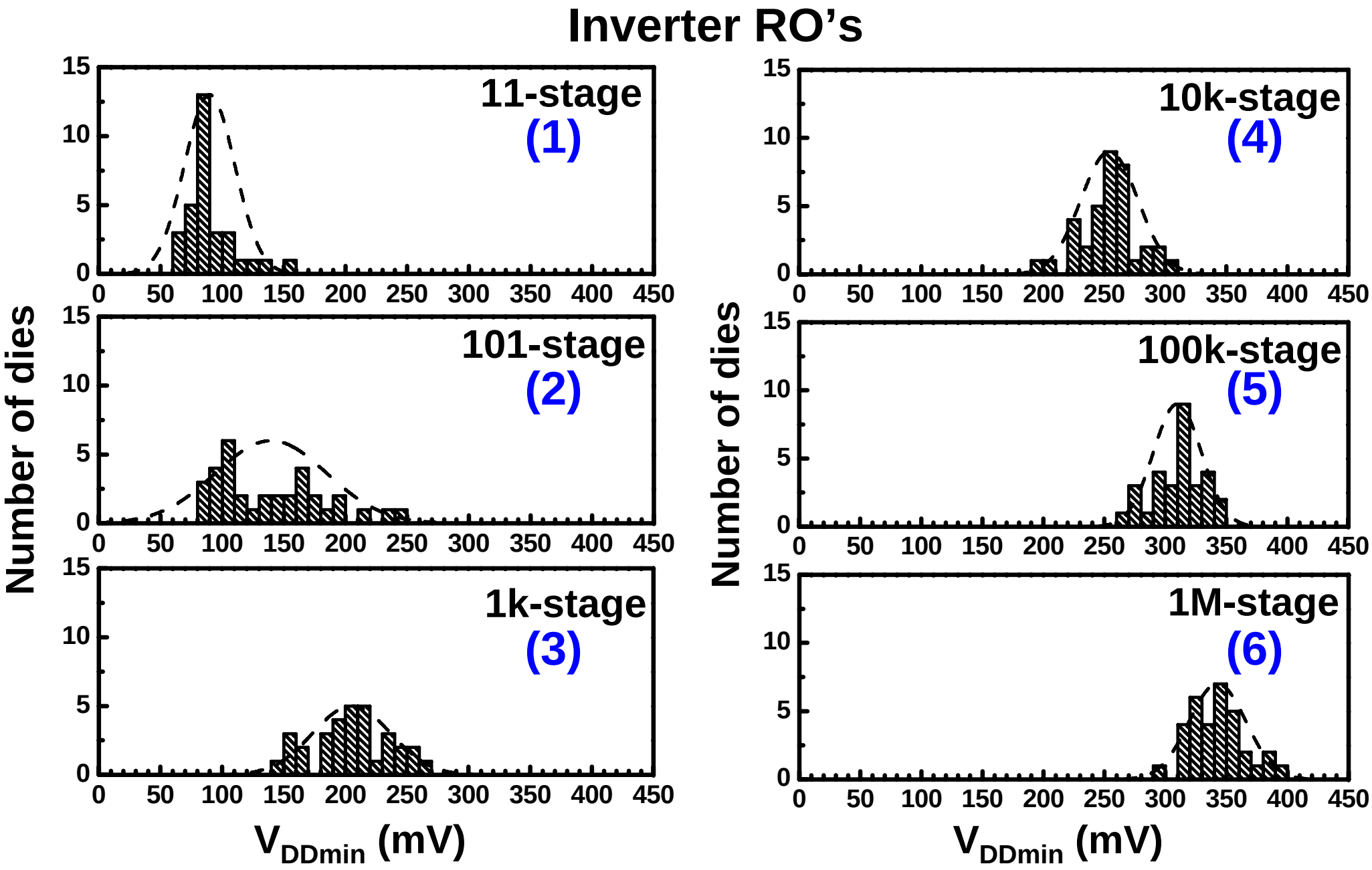


実測
90nm CMOS
インバータRO

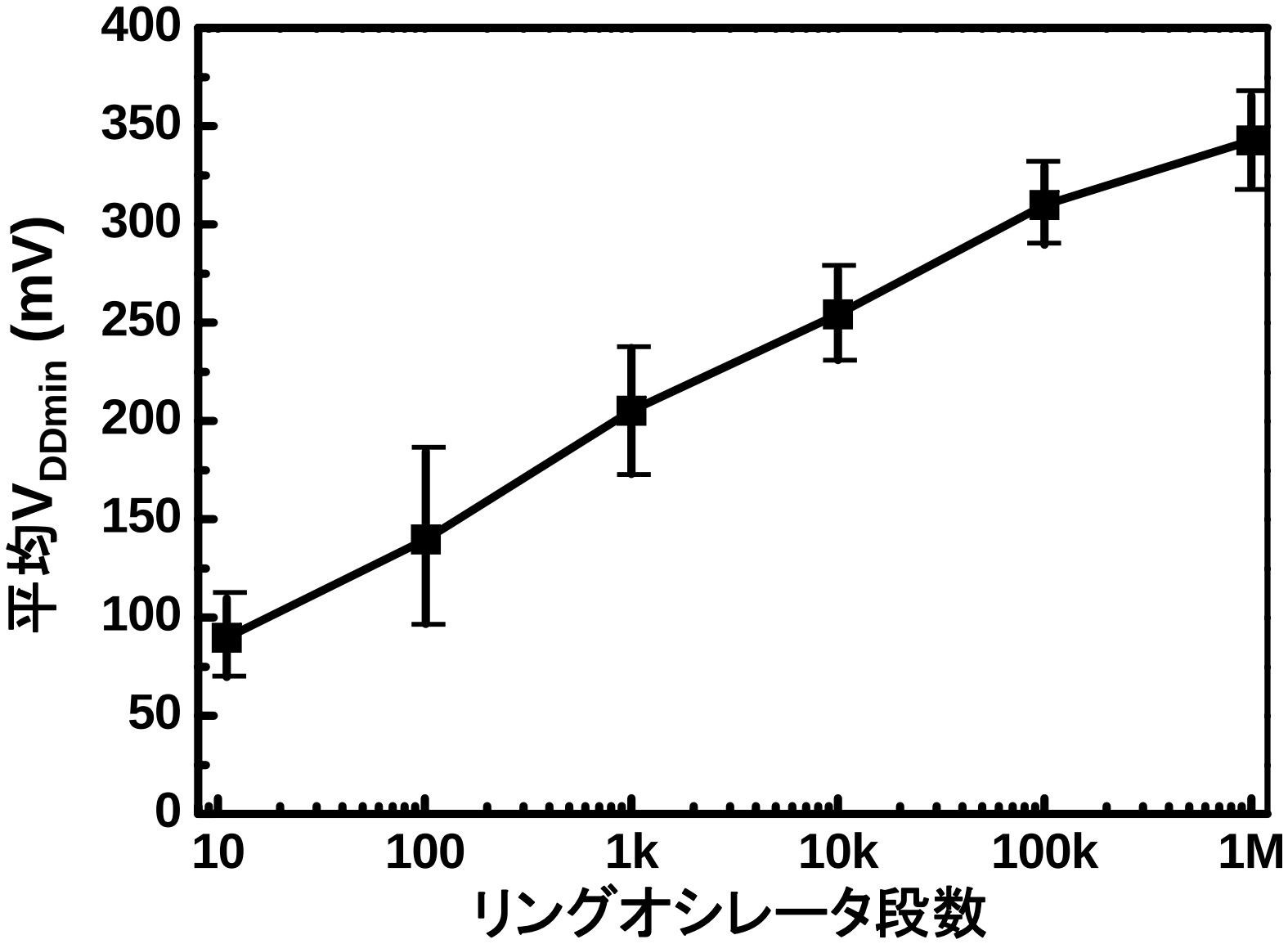


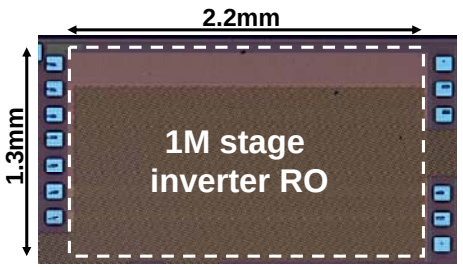
- 低V_{DD}回路の問題：低速、PVTばらつきに敏感
- 対策：並列動作、adaptive制御

Measured Die-to-Die Distribution of V_{DDmin}



論理ゲートのV_{DDmin}をROで調査

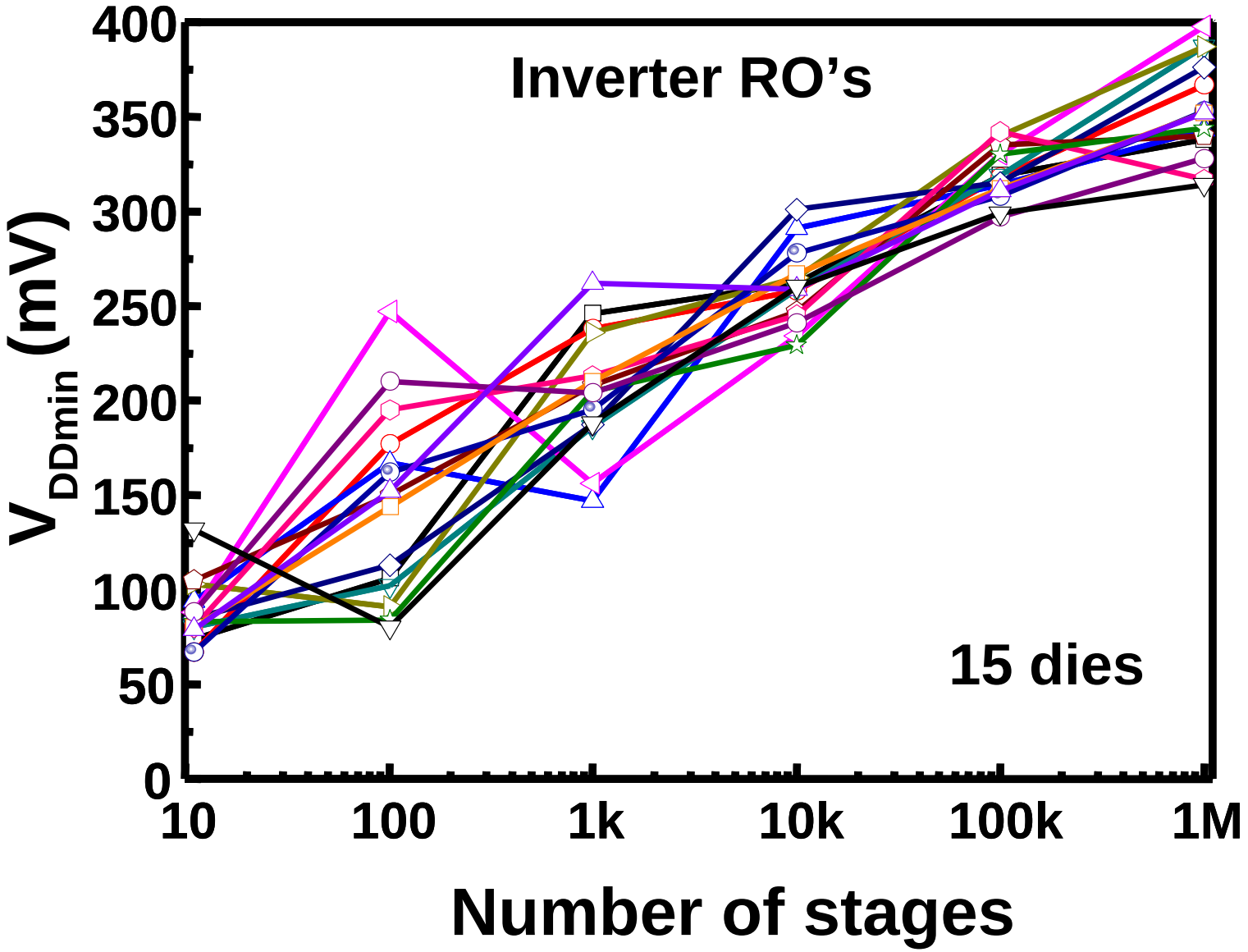




実測
90nm CMOS
インバータRO
複数チップ測定

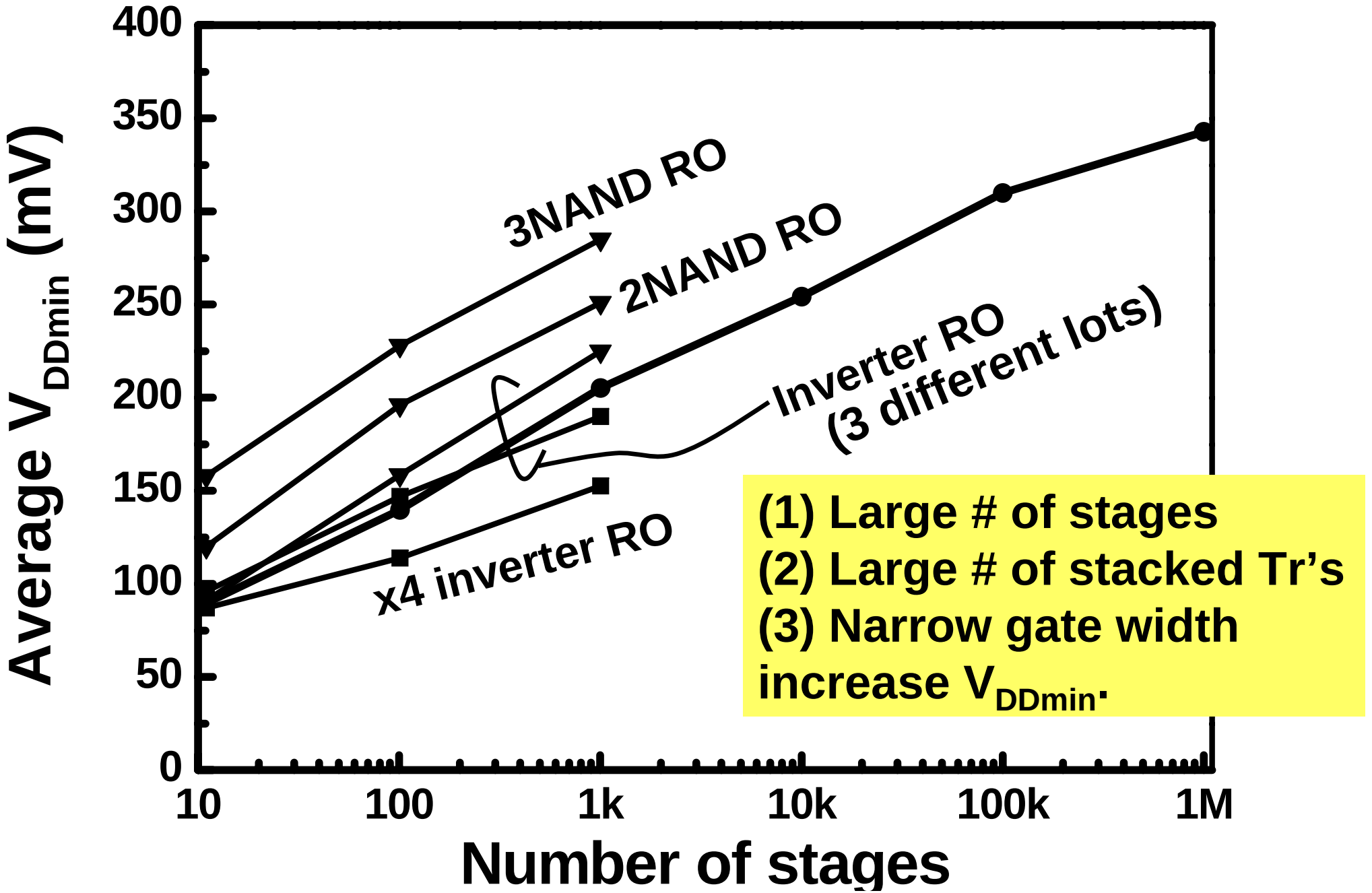
■ 大規模になるほど、より高いV_{DDmin}が必要に
→大規模ロジックになるほど、低V_{DD}化が困難

Analysis of Die-to-Die V_{DDmin} Variations

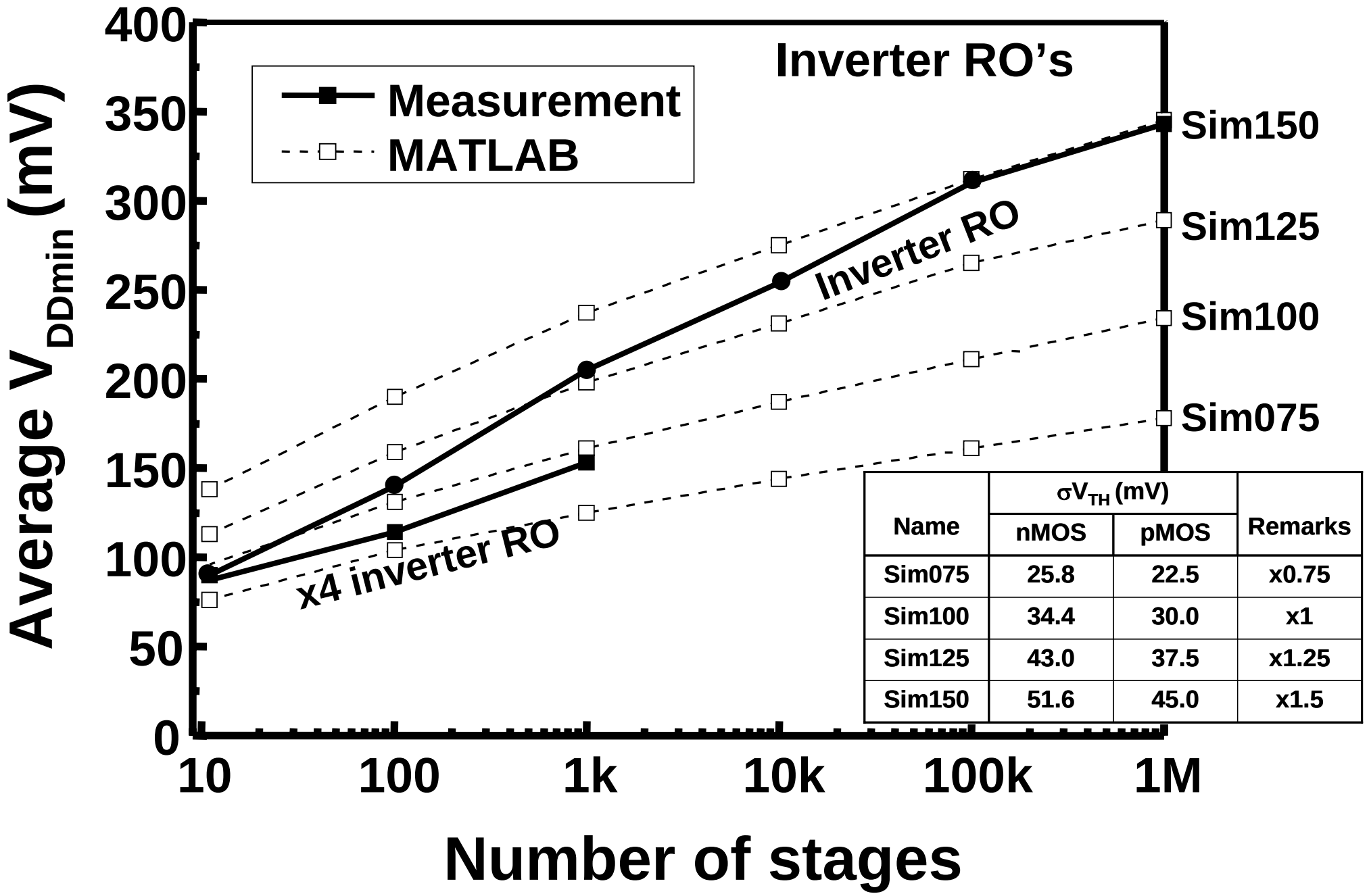


- The die-to-die V_{DDmin} variations are not systematic but random.

Summary of Measured V_{DDmin}



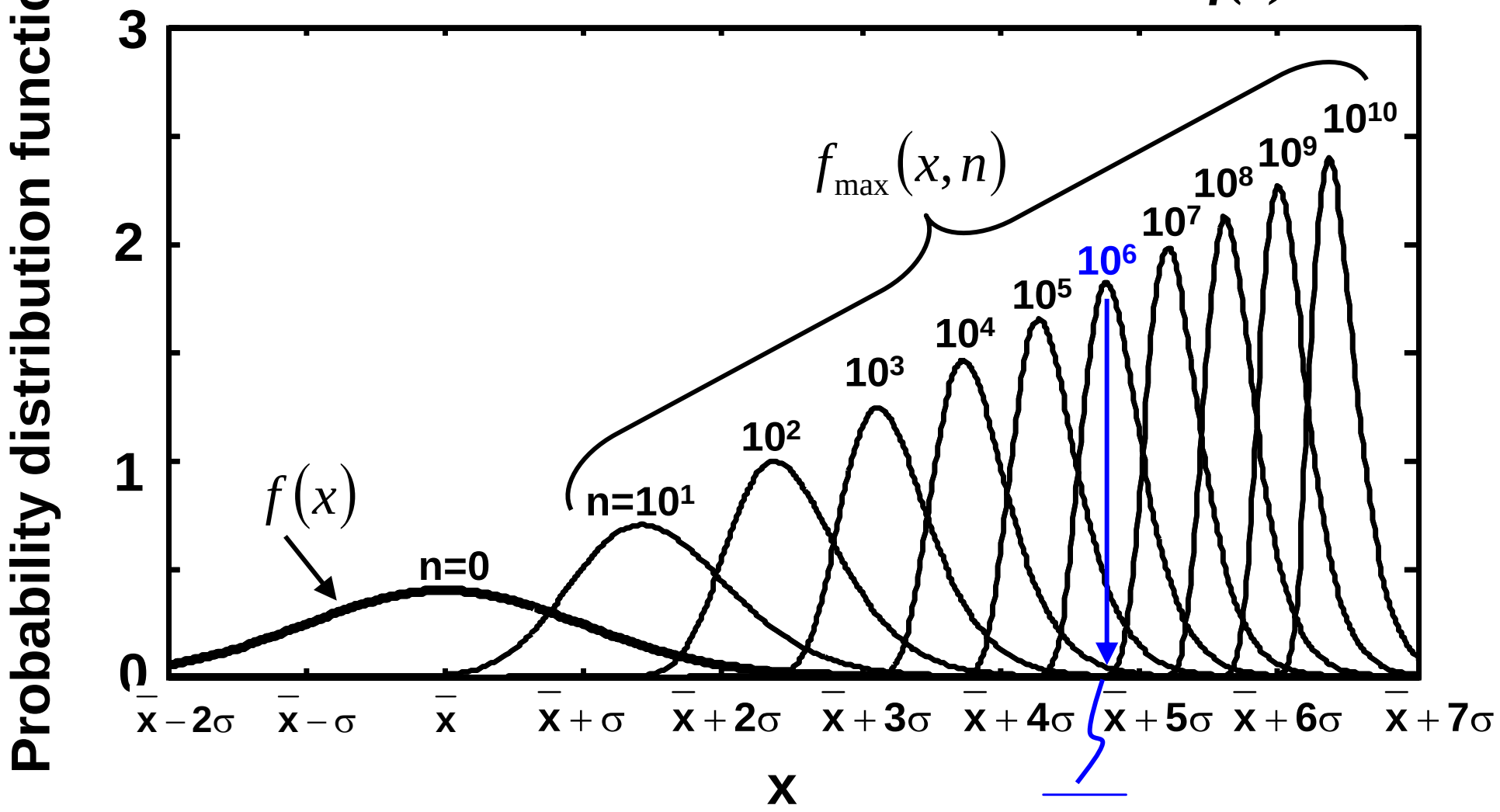
Comparison of Measured and Calculated V_{DDmin}



Name	σV_{TH} (mV)		Remarks
	nMOS	pMOS	
Sim075	25.8	22.5	x0.75
Sim100	34.4	30.0	x1
Sim125	43.0	37.5	x1.25
Sim150	51.6	45.0	x1.5

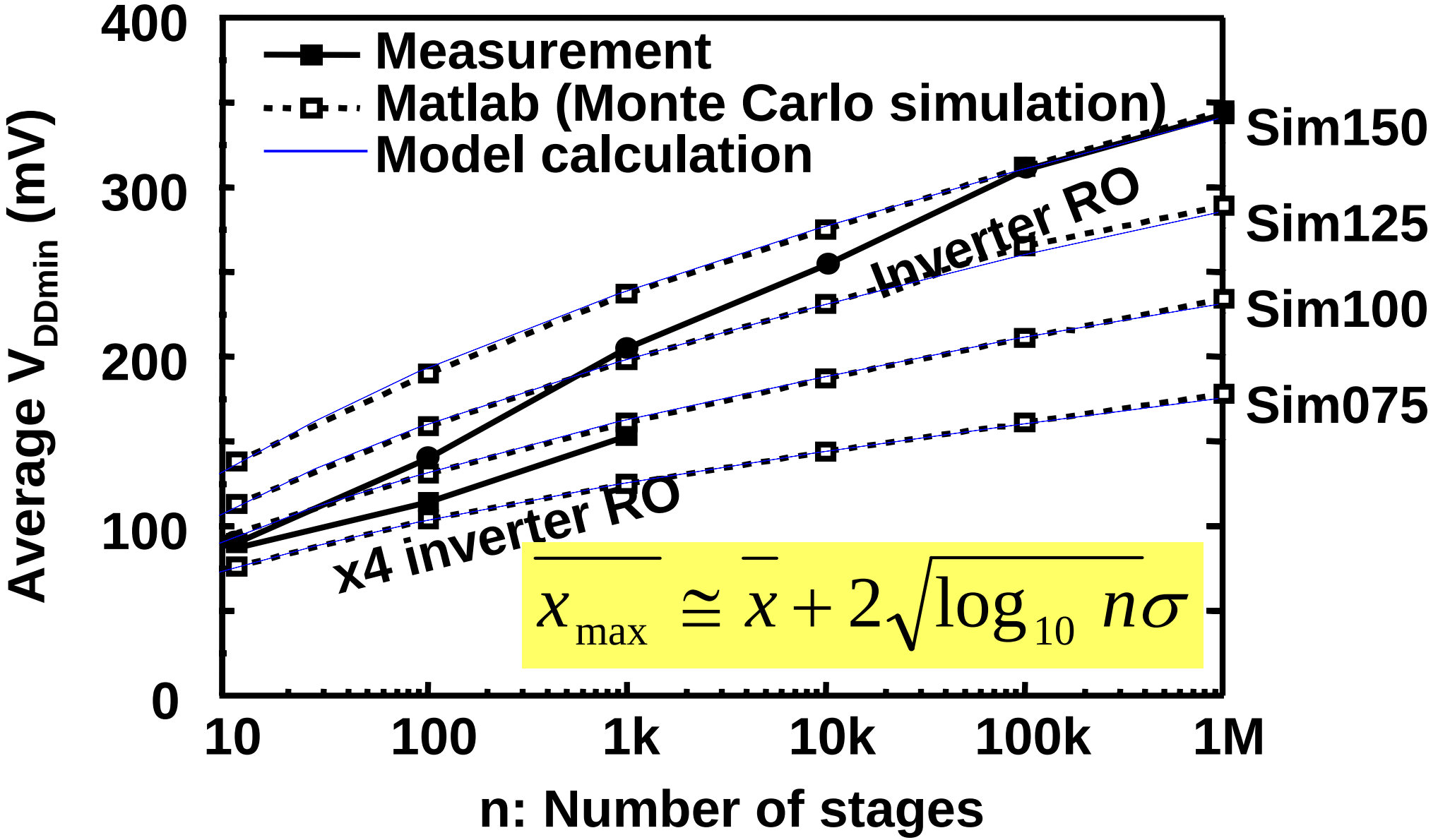
Reason Why Average V_{DDmin} Increases with # of RO Stages

The largest value distributions $f_{max}(x,n)$ of n samples which have Gaussian distribution $f(x)$



$$\overline{x_{\max}} \cong \bar{x} + 2\sqrt{\log_{10} n}\sigma$$

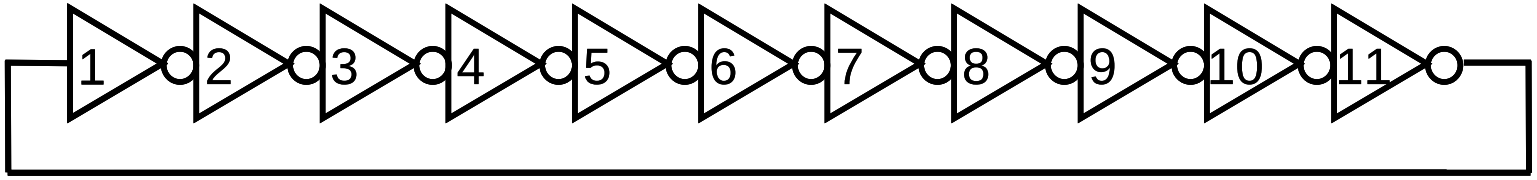
Comparison of Monte Carlo and Model



- The equation intuitively explains the reason why the average V_{DDmin} increases with the number of RO stages.

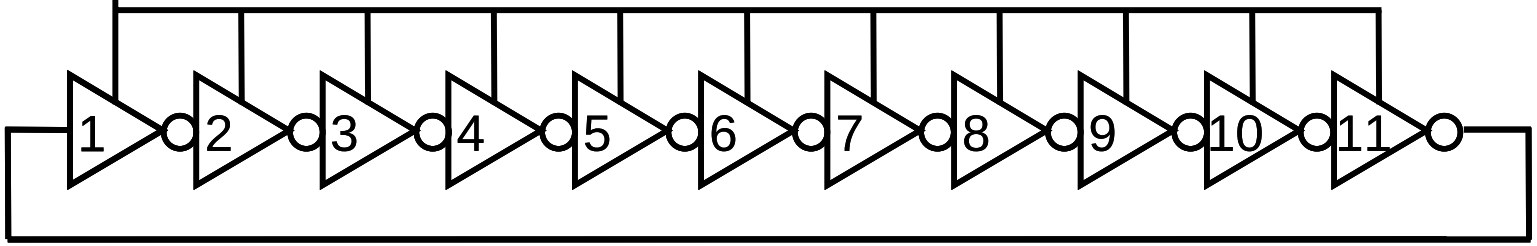
Adaptive Body Bias Control to Reduce V_{DDmin}

Simulated



V_{DDmin}=89 mV (Initial)

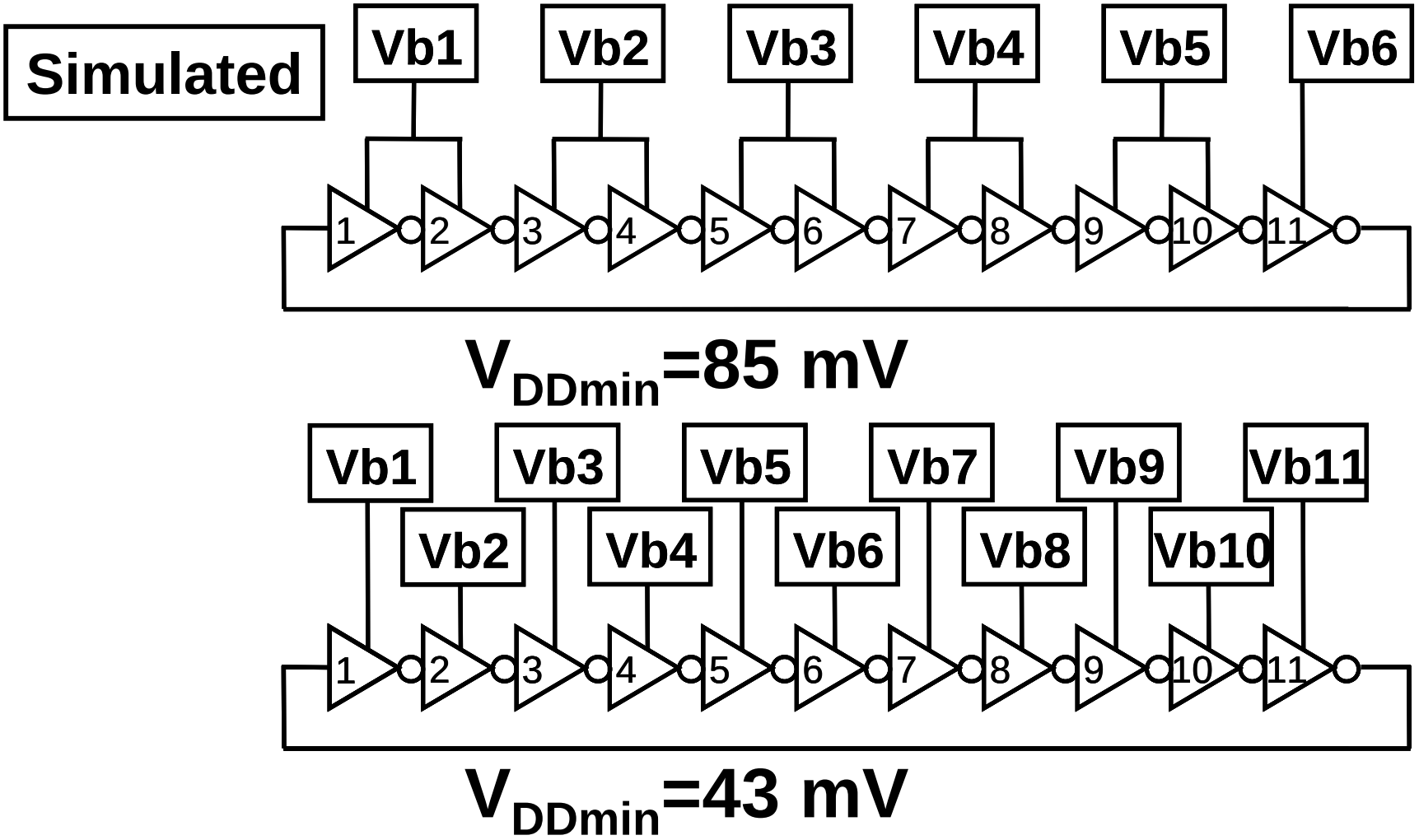
Body bias control



V_{DDmin}=87 mV

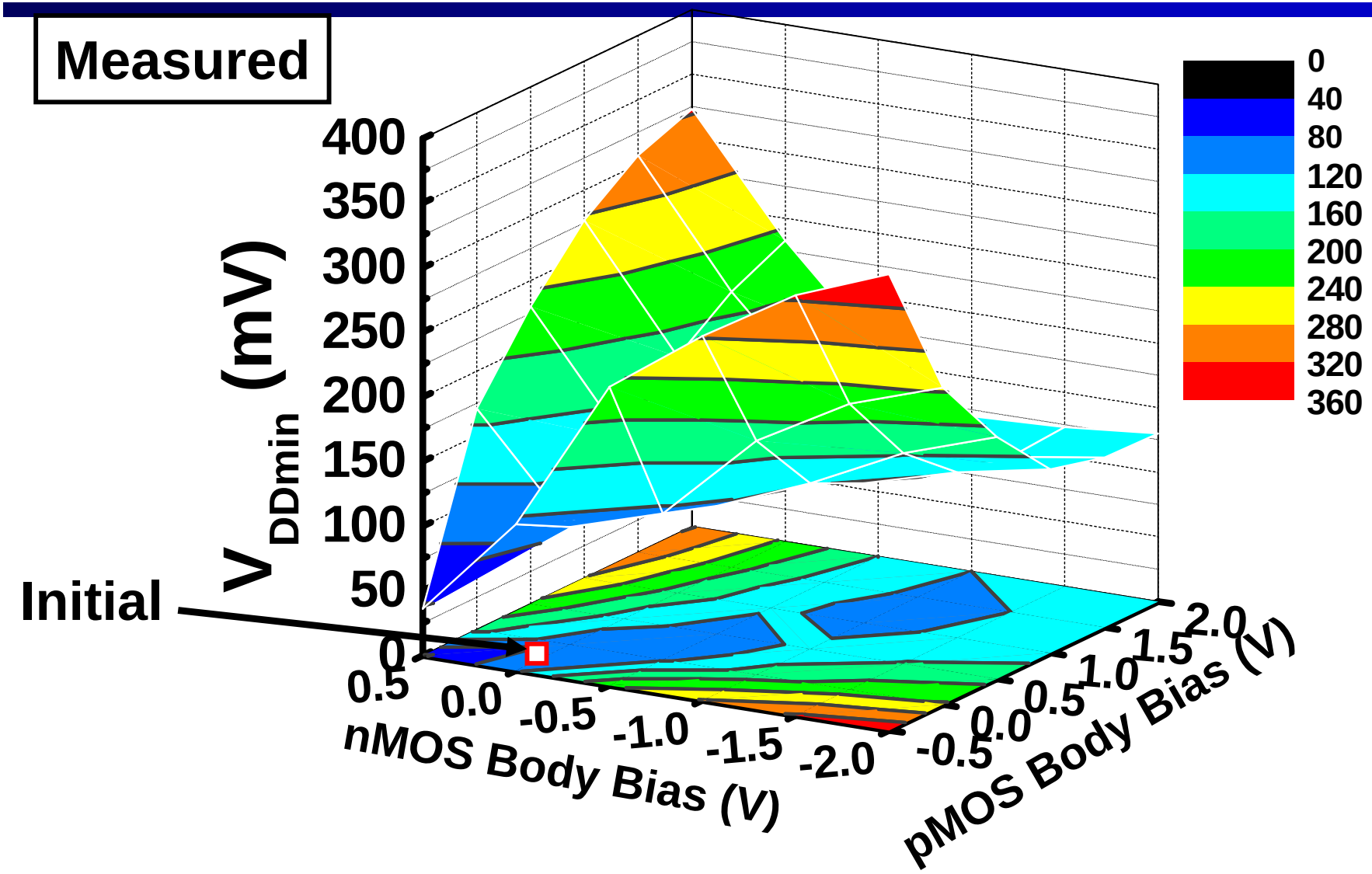
- **The body bias of pMOS is adaptively controlled to minimize V_{DDmin} and the body bias of nMOS is fixed.**

Fine-Grain Adaptive Body Bias Control to Reduce V_{DDmin}



- When inverter-by-inverter body bias is applied, V_{DDmin} is drastically reduced to 43mV. But it is impractical.

V_{DDmin} Dependence on Body Bias of Both nMOS and pMOS



- Common body bias control allows to reduce V_{DDmin} by only 4mV.

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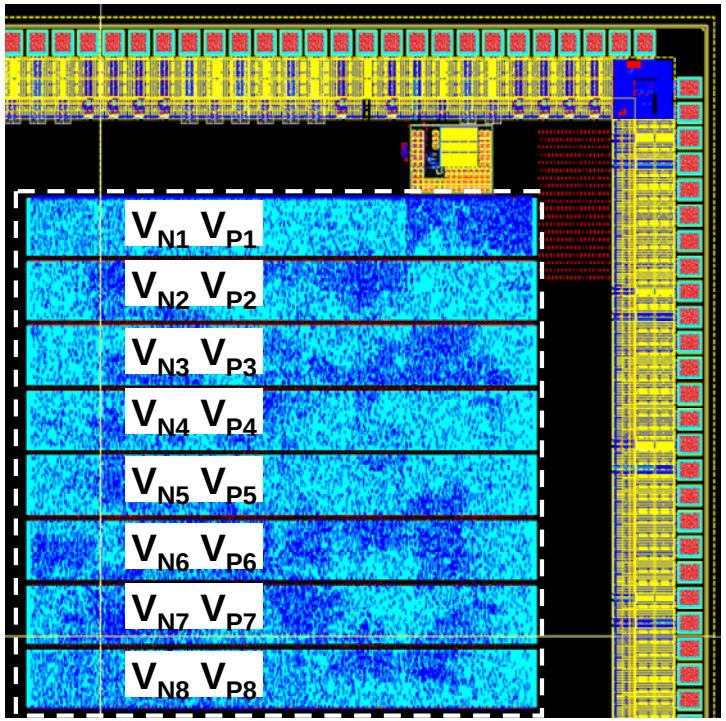
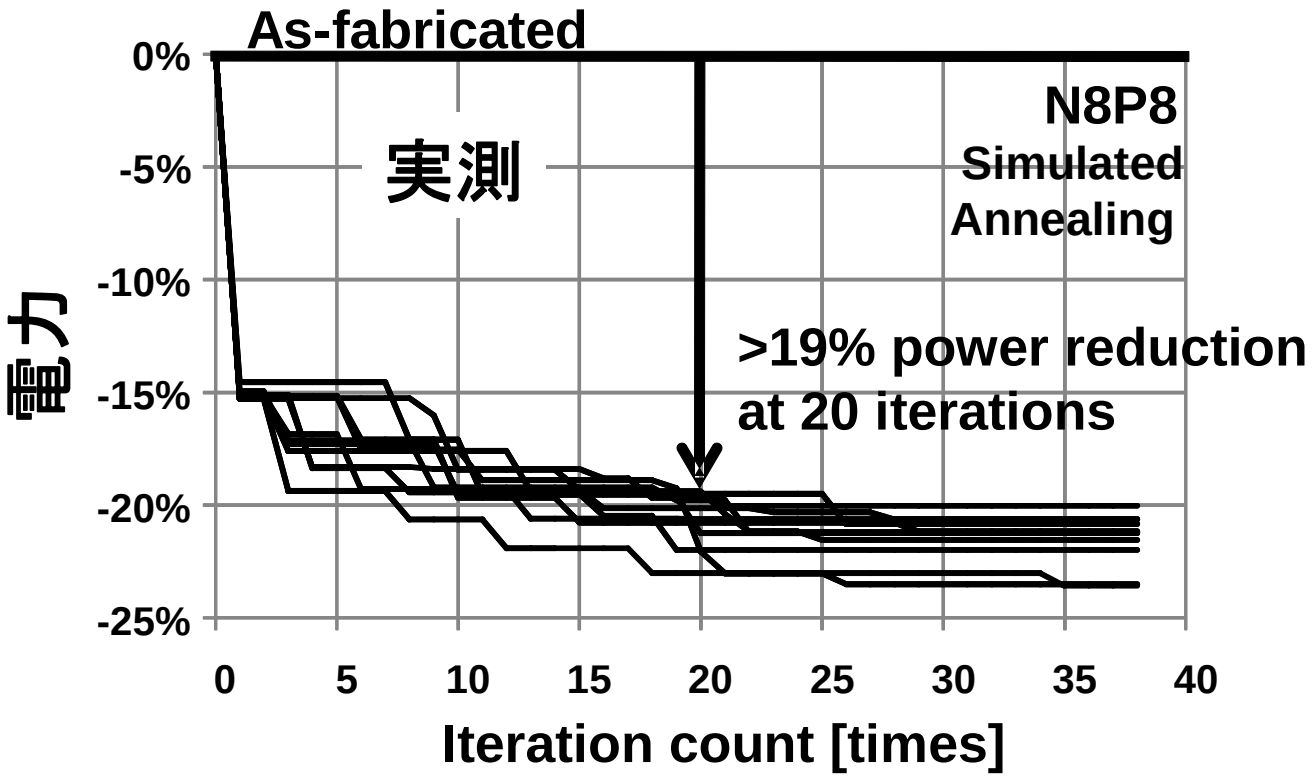
細粒度基板バイアス制御による低電力化



機能	64bit DES CODEC
プロセス	1V, 90nm CMOS

1つの機能ブロックを8領域に等分割



基板バイアス16変数の最適化

- 基板バイアスのグローバル最適化により電力を19%以上削減
- post-fabrication tuningにより設計ばらつきを補正

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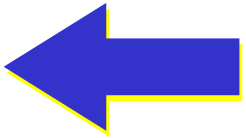
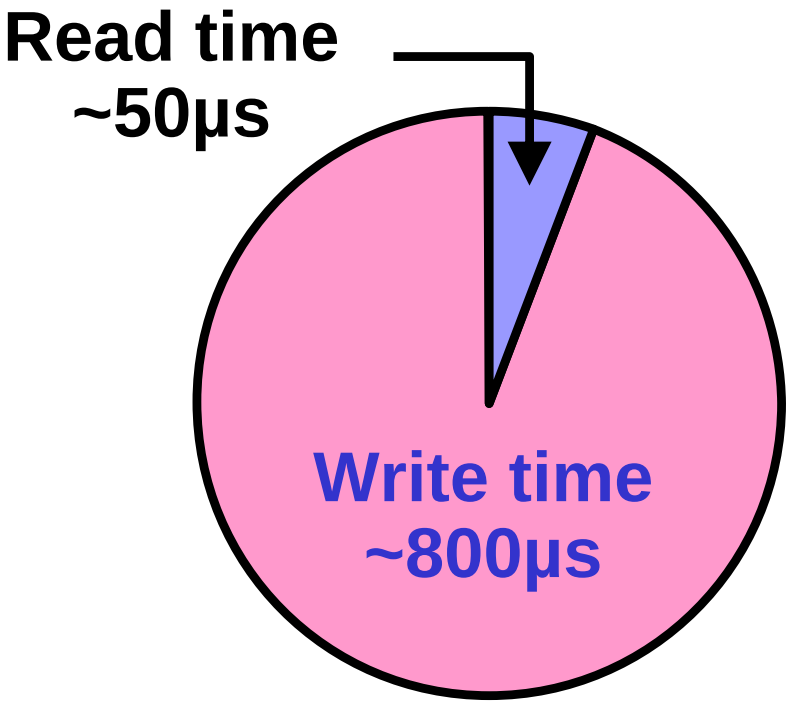
- 3次元SSDのNANDフラッシュ向け昇圧回路による低電力化 

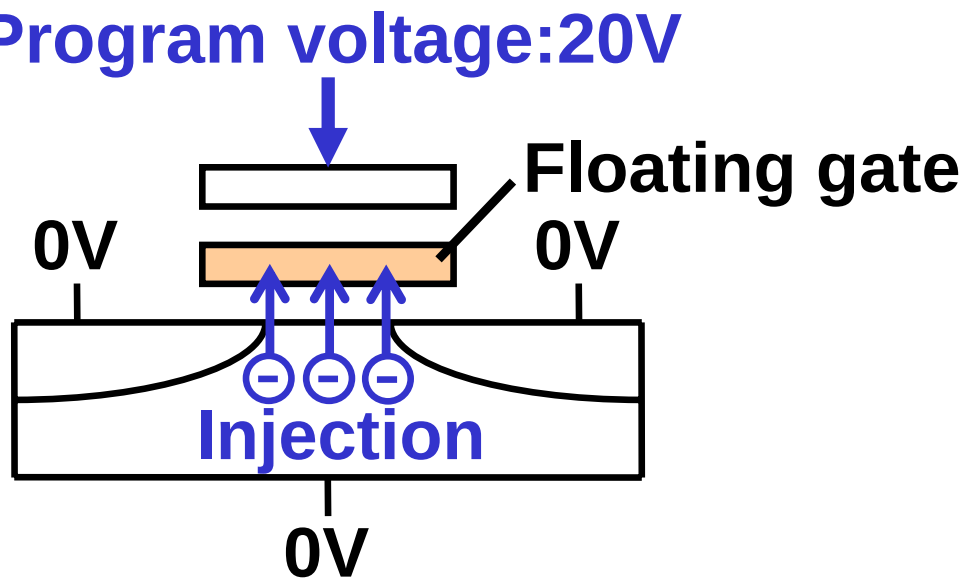
(SSD: Solid State Drive)

Importance of 20V generator in NAND

☹ Write time is dominant over read time.
➔Write 8 to 16 chips simultaneously.

☹ 20V or higher program voltage for write
➔Energy during write should be reduced.





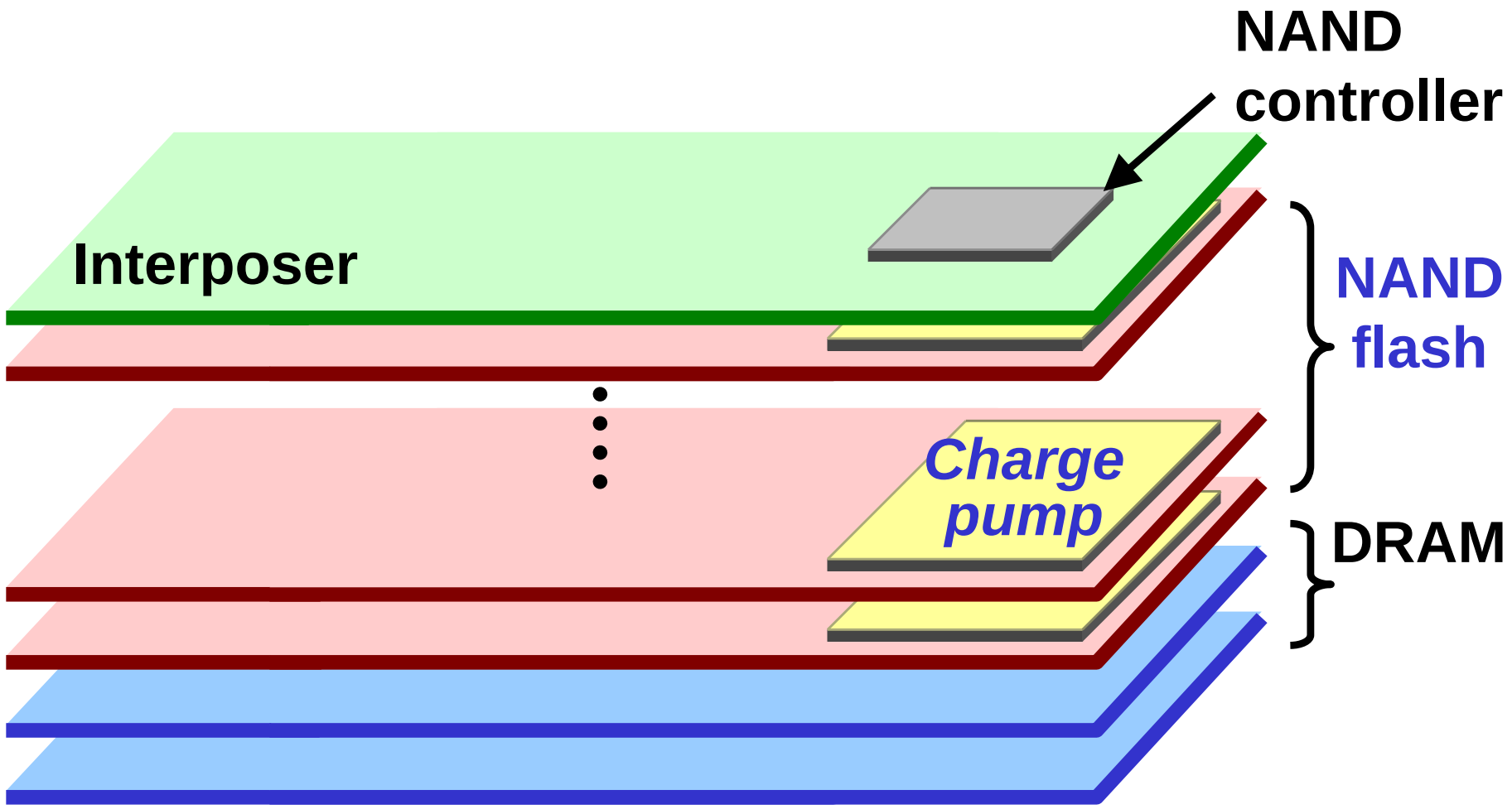
Write operation of NAND flash

High-speed low-power 20V generator is required.

Conventional SSD with charge pump

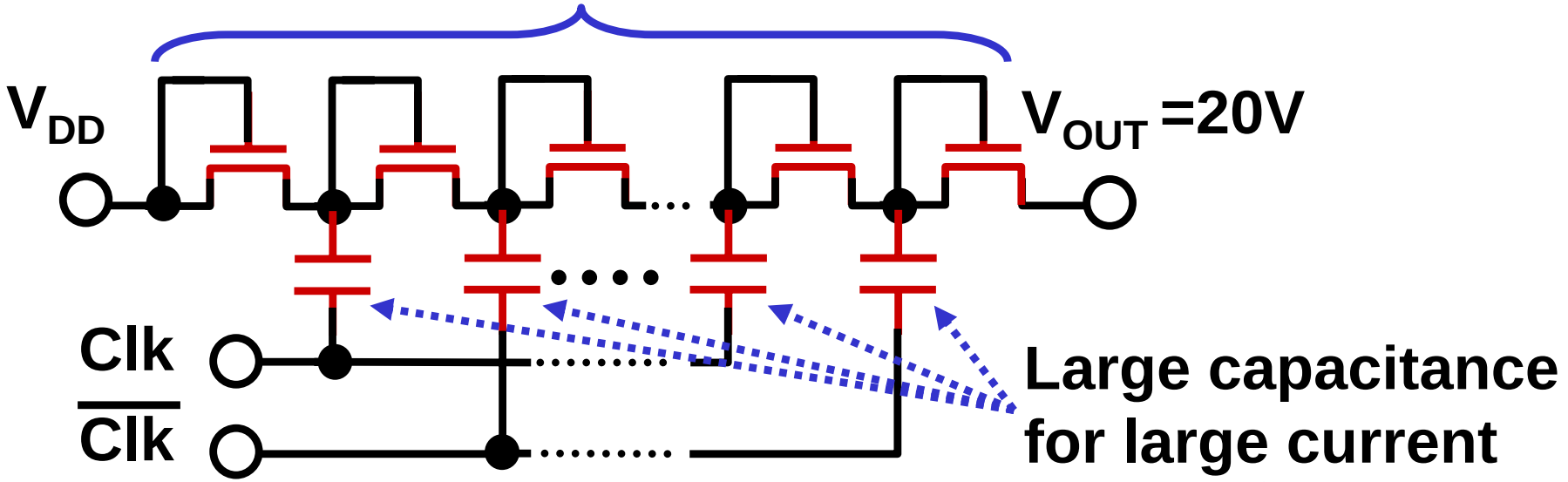
Each NAND flash has charge pump for 20V.

☹ 5 to 10% area of NAND flash chip!

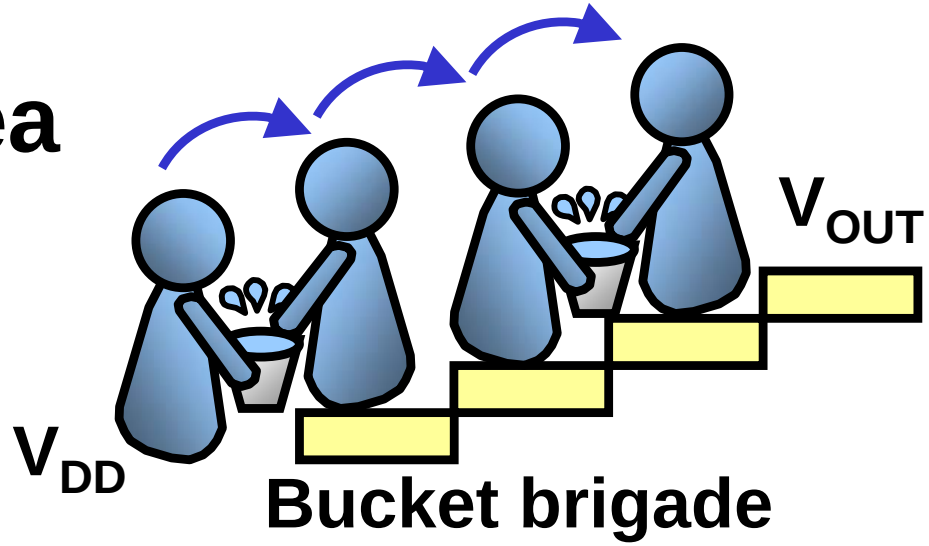


Issues on charge pump

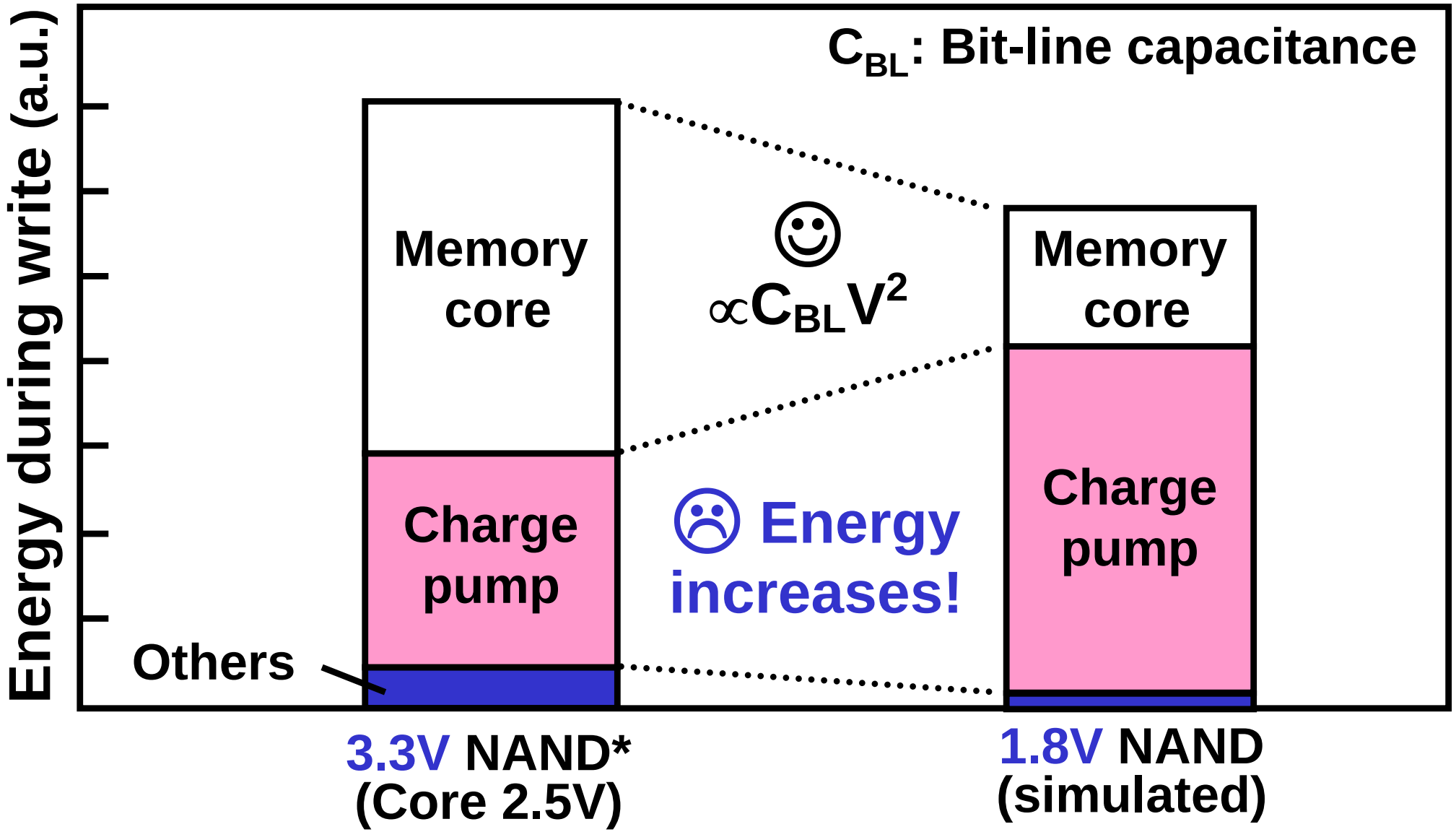
Serial MOS diodes lose energy.
Large number of stages for low V_{DD}



☹ **Large capacitance area**
☹ **Energy loss**



Voltage scalability of charge pump

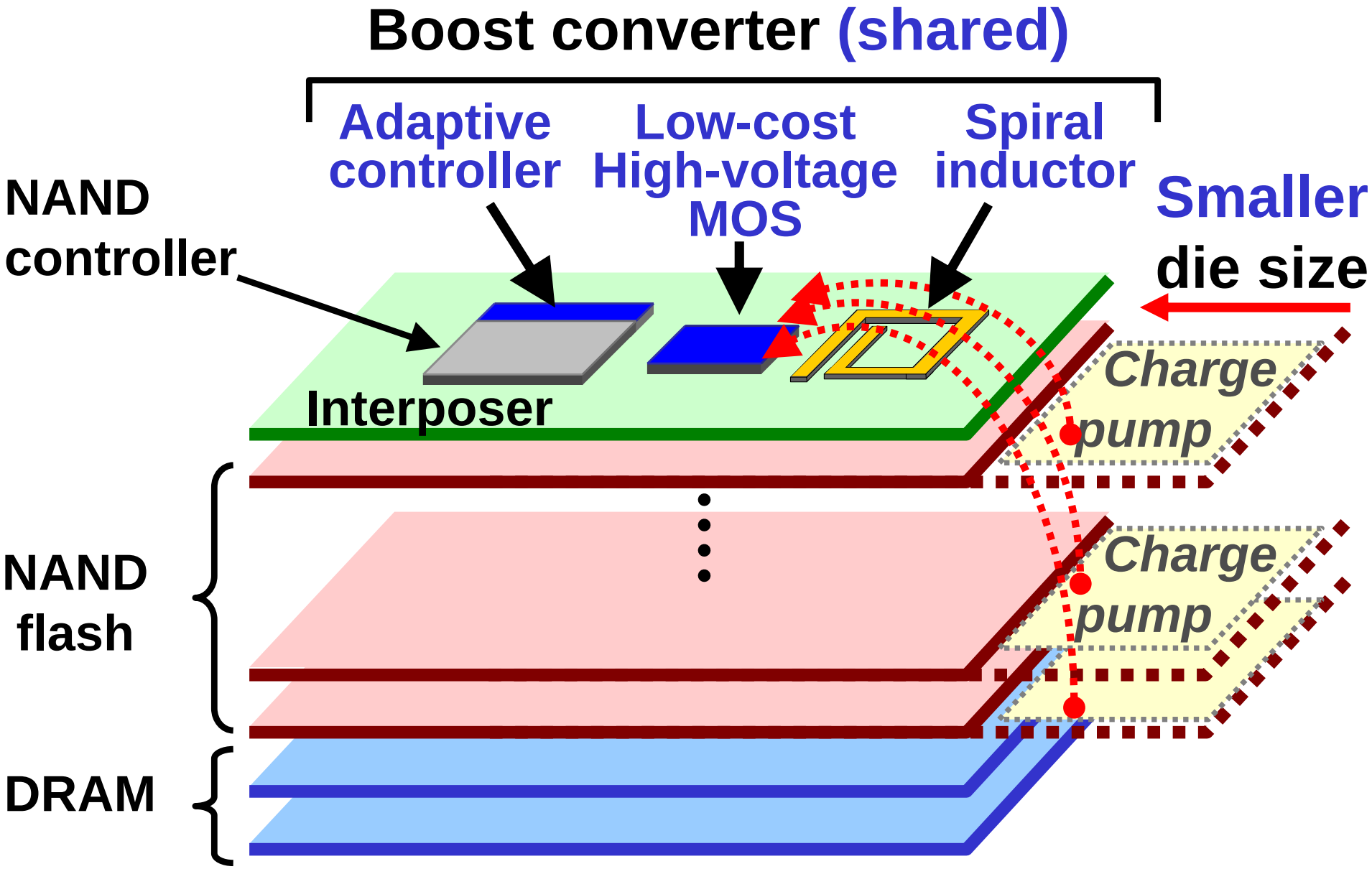


Energy by charge pump increases!

*K. Takeuchi, et al., ISSCC 2006

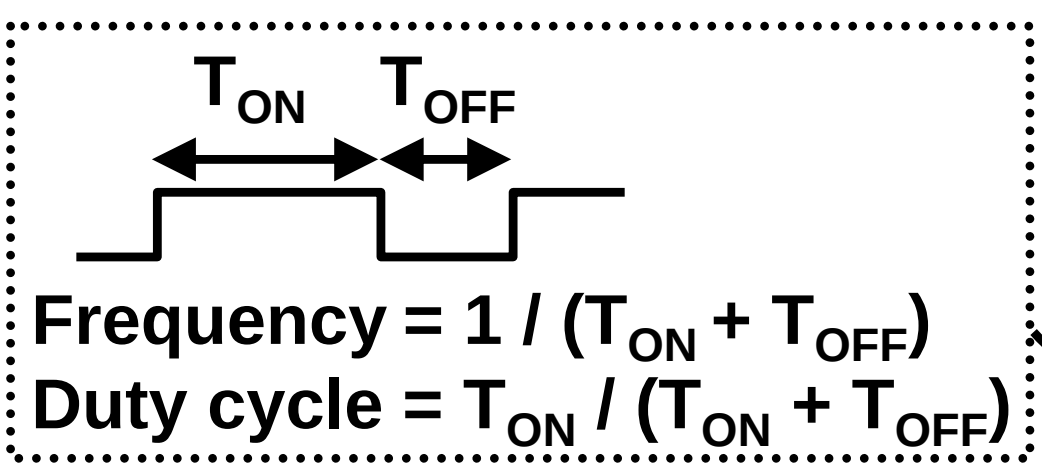
Proposed 3D-SSD with boost converter

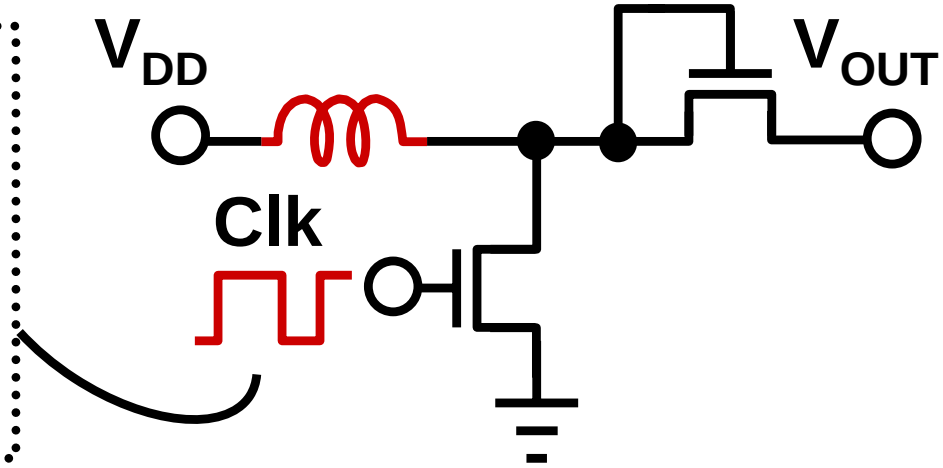
☺ Realizing low power and low cost



Advantages of Boost converters

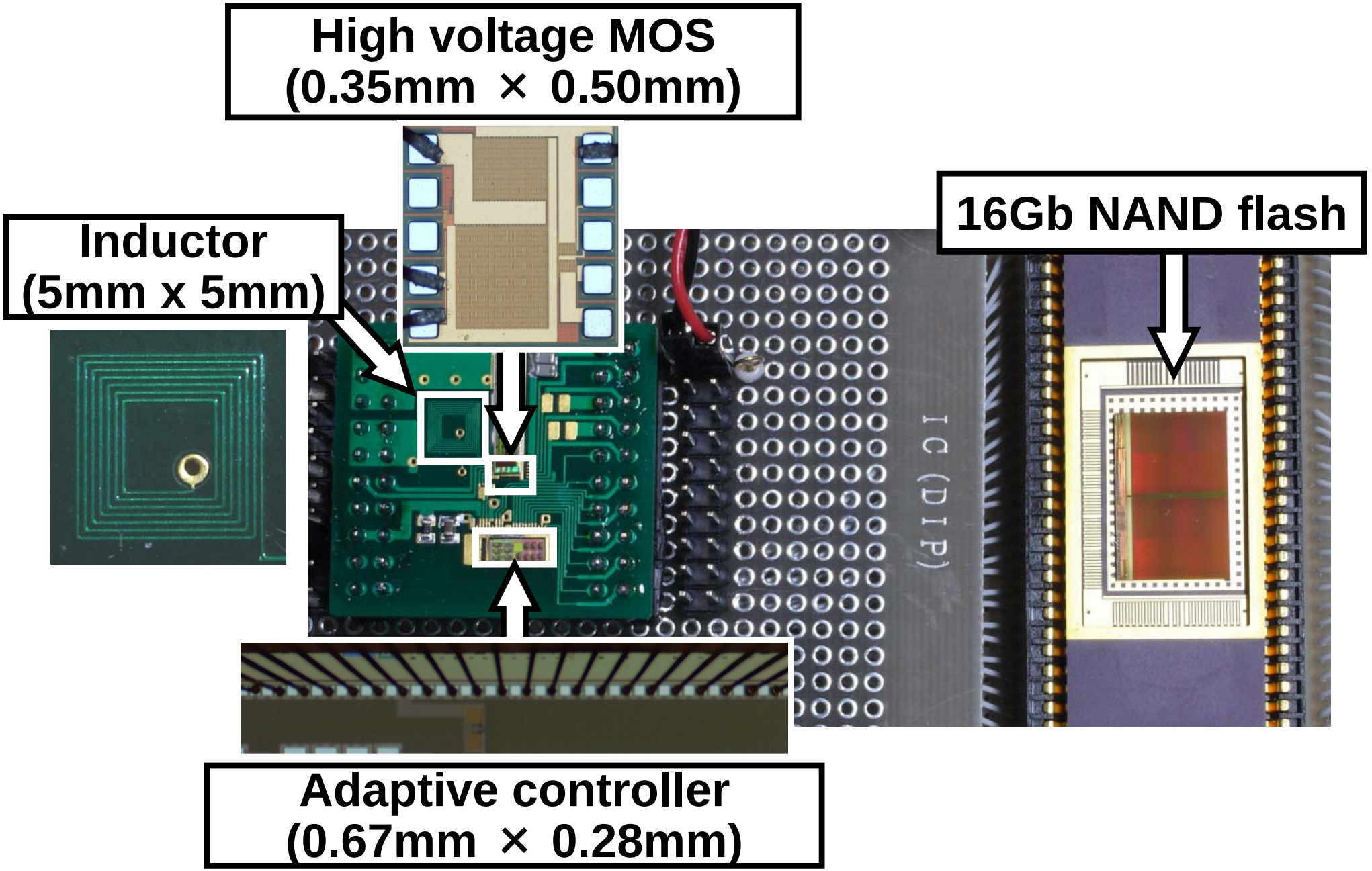
Frequency, duty cycle ➔ Conversion ratio (V_{OUT}/V_{DD})
Inductance ➔ Output current



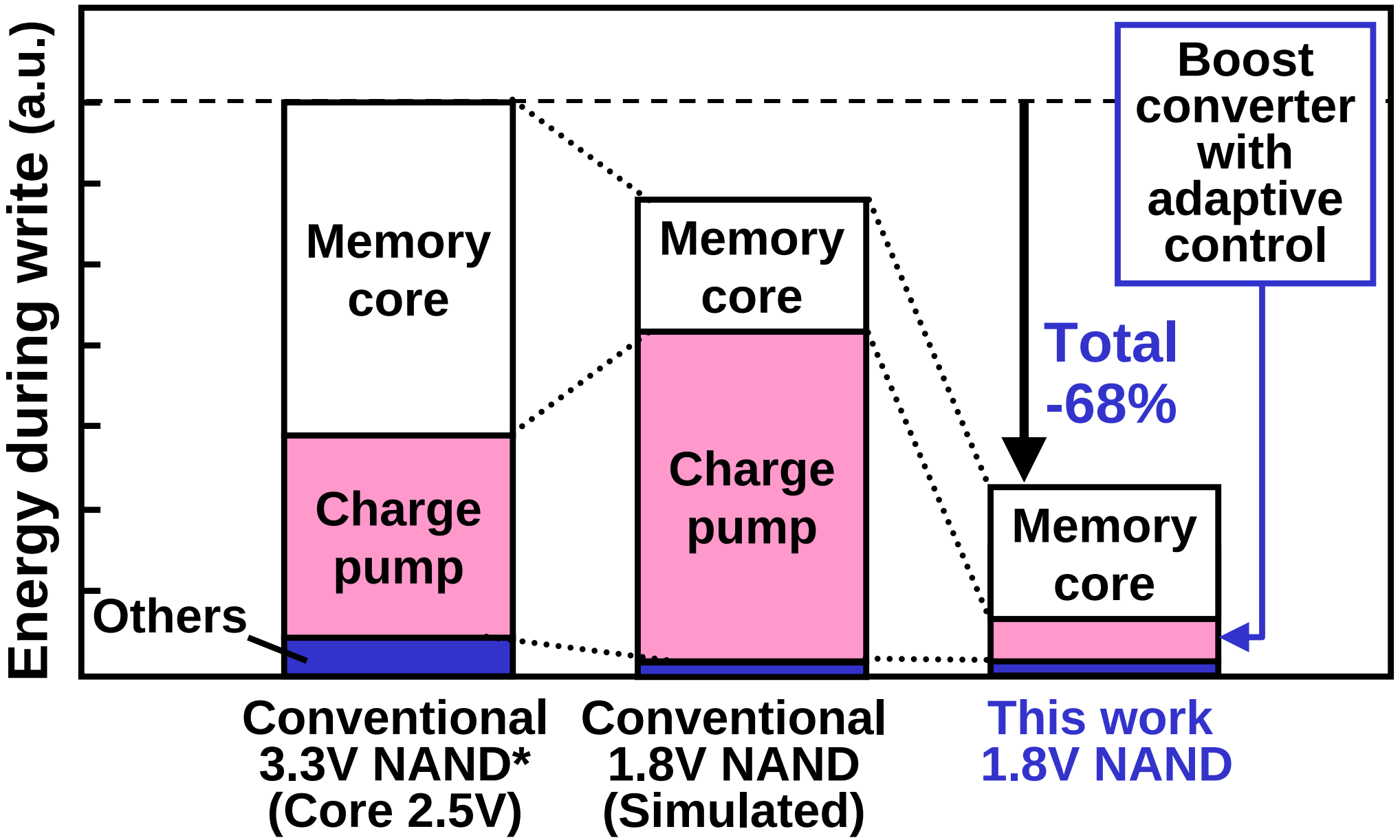


- ☺ High conversion ratio, large output current
- ☺ High efficiency
- ☺ Small chip area
- ☹ Off-chip inductor

Boost converter & NAND Co-operation



Comparison of energy during write



*K. Takeuchi, et al., ISSCC 2006.

Summary of key features

	This work (Measured)	Charge Pump (Simulated)
Transient energy (0➔15V)	30nJ (12%)	253nJ (100%)
Rising time (0➔15V)	0.92μs (27%)	3.45μs (100%)
Chip area (HV-MOS)	0.175mm^2 (15%)	1.19mm^2 (100%)
Technology (High voltage MOS)	20V CMOS process	--------
Chip area (Adaptive controller)	0.188mm^2	--------
Technology (Adaptive controller)	1.8V 0.18μm standard CMOS	--------
Supply voltage	1.8V	1.8V

まとめ

◆低電力設計技術の3つのキーワード
→(1)低電圧、(2)細粒度制御、(3)3次元

◆チップ内製造ばらつきはランダム(90nm CMOS, 4mm)
→細粒度制御では対処不能
→一方、設計ばらつきは細粒度制御で対処可能

◆リングオシレータの段数を11段から1M段にすると、
V_{DDmin}は90mVから 343mVに増加
→大規模ロジックの低電圧化は困難
→革新的な回路技術が必要

◆ 3次元による低電力化の例　→SSD

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