7.3 User Customizable Logic Paper (UCLP) with Organic Sea-of-Transmission-Gates (SOTG) Architecture and Ink-Jet Printed Interconnects

Koichi Ishida[1], Naoki Masunaga[1], Ryo Takahashi[1], Tsuyoshi Sekitani[1], Shigeki Shino[2], Ute Zschieschang[3], Hagen Klauk[3], Makoto Takamiya[1], Takao Someya[1], Takayasu Sakurai[1]

[1]University of Tokyo, Tokyo, Japan
[2]Mitsubishi Paper Mills, Kyoto, Japan
[3]Max Planck Institute for Solid-State Research, Stuttgart, Germany

With recent advances in printable large-area electronics [1, 2], it is not a fantasy anymore to print macroscopic-level organic ICs by ink-jet printers. To prototype the organic circuits for the higher integration level, we propose User Customizable Logic Paper (UCLP). The UCLP can be easily customized by the user and operated in a speed for educational purposes that one can see how the circuit operates with one's naked eyes. With an ordinary ink-jet printer, one can utilize UCLP to make one's own circuit by printing customized interconnects on the prefabricated array of organic transistors. This paper demonstrates the feasibility and in-field customizability of UCLP with Sea-of Transmission-Gates (SOTG) of organic CMOS transistors. This type of technology will provide ways to add programmability for ICs used in large-area electronics such as smart flexible displays, power transmission sheets, and electronic skin for robots.

Figure 7.3.1(a) shows the UCLP, in which a sheet of paper containing an array of vias and an organic SOTG film are stacked. Organic transistors are prefabricated and the in-field customizability is provided by the printed interconnects. Conventional printed interconnects require high-temperature (130-150ºC) sintering, which damages organic transistors. We develop the conductive Ag nanoparticle ink to solve this problem. The Ag ink is printed on the paper with the pre-coated nanoconductive base to form the conductive interconnects under room temperature. Figure 7.3.1(b) shows the interconnect printing process on UCLP by a commercial ink-jet printer. The design rule of interconnects is 200μm. The thickness is 10μm and the measured sheet resistance is 0.4Ω/square. The via holes 200μm in diameter are prefabricated in UCLP by punching the paper to form connections among SOTG cells. The measured via resistance is 2.7Ω/via. Figure 7.3.1(c) shows the experimental setup of the UCLP for educational purposes. The photograph has been shown to give an example and that the UCLP in Fig. 7.3.1(c) was not operated. Such experiences in designing and printing interconnects of custom ICs on UCLP and performing the experiment on macroscopic ICs operating at visible speed will help learners to understand the operations of the ICs.

Figure 7.3.2(a) shows the cross section of UCLP that consists of an SOTG and a rewiring layer on paper. The 2V organic CMOS transistors are fabricated on polyimide film [3, 4]. Materials for nMOS and pMOS are $F_{16}CuPc$ and pentacene, respectively [3]. Figure 7.3.2(b) shows the 8×8 SOTG cell array and the details of a single SOTG cell. The sizes of the 8×8 SOTG cell array and the single SOTG cell are 73mm square and 6mm square, respectively. The design rule of the SOTG is 20μm. SOTG is a type of pass transistor logic and each cell has 6 transistors. The output (OUT) is connected to either PSW or NSW depending on the input (IN). Each SOTG cell has four pads for ink-jet printed interconnects. V_{DD} and V_{SS} are shared by every SOTG cell. The large pad pitch of 3mm is a design challenge for UCLP to increase the integration density. The 3mm pitch is determined from (1) the error (=0.3mm) in feeding the paper in the printer, (2) the design rule (L/S=200μm) of the printed interconnect, and (3) the number of interconnects (=4) between the pads. To solve the problem, an area-efficient SOTG is proposed instead of the conventional Gate Array (G/A).

Figure 7.3.3 shows several examples of logic gate implementation with SOTG cells. An inverter requires one logic cell, as shown in Fig. 7.3.3(a). At first glance, the SOTG architecture will consume a large number of transistors, but it will not be critical for the UCLP. In terms of saving on rewiring cost or area, the SOTG makes it easy to customize the UCLP. In fact, either a buffer or a two-input multiplexer can be implemented with one cell, as shown in Figs. 3(b) and 3(c). An XOR gate consists of a two-input multiplexer and an inverter, which are connected in the way as shown in the bold line in Fig. 7.3.3(d). Not only the XOR gate, but also any two-input logical operation can be realized with only two SOTG cells [5]. Furthermore, a D-flip flop can be implemented with four cells and six interconnects, in addition to the power supply connection to both V_{DD} and V_{SS}, as shown Fig. 7.3.3(e).

Figure 7.3.4 shows logic cells of the conventional G/A and the SOTG. Under the condition of a via spacing rule of 3mm for printed interconnects on paper, a typical G/A cell occupies an area of 81mm^2 because there are nine vias in each cell, as shown in Fig. 7.3.4(a). On the other hand, the logic cell of SOTG has only a 36mm^2 area although the number of transistors in an SOTG cell is more than that in G/A. Figure 7.3.4(b) indicates the number of transistors in various logic functions. The number of transistors in the SOTG tends to be more than that in the G/A except in a few functions such as a multiplexer and a latch. In contrast, the required area for implementing logic functions in the SOTG are less than those in the G/A in each function shown in Fig. 7.3.4(c). The results indicate the SOTG can reduce the area of cells by 11% (INV and NAND) to 85% (MUX) for the UCLP, compared with a typical G/A architecture.

To evaluate signal attenuation of the printed interconnects, the open drain pMOS LED driver with three printed interconnects shown in Fig. 7.3.5(a) is measured. Figure 7.3.5(b) shows the measured waveform in the case with conventional metallic interconnects for reference. The output swing is around 2.0V with 2.5V V_{DD}. Figure 7.3.5(c) shows the output waveform from the printed interconnects on the paper. Although the output swing is slightly degraded by the printed interconnects, it is acceptable because the driver can still provide capability to drive low-power LEDs and logic gates of the SOTG.

Figure 7.3.6(a) shows the schematics of the setup for a two-input multiplexer using the SOTG cell. Square waves of 200mHz are applied to the select signal, S, and square waves of 800mHz are applied to an input terminal, A. Another input terminal, B is connected to V_{SS}. Figure 7.3.6(b) shows measured waveforms. The result confirms that the organic CMOS transmission gates can successfully conduct both high and low signals, and therefore, the feasibility of the SOTG architecture is verified by measurement.

In order to measure the propagation delay of the SOTG logic cell, a ring oscillator using three organic SOTG cells and an organic CMOS output buffer are fabricated on a silicon substrate. Figure 7.3.7(a) shows its schematic and Fig. 7.3.7(b) shows the chip photograph. The oscillator operates from 2.0 to 3.0V V_{DD} and its measured frequency is 2.84Hz at V_{DD} of 3V, which equals to 0.12s propagation delay of each cell. It is appropriate for educational purposes since the LED can flash at a visible speed.

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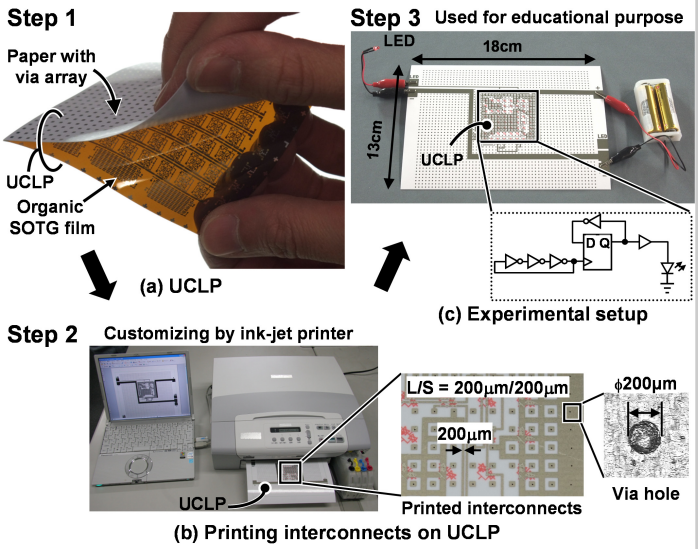


Figure 7.3.1: User Customized Logic Paper (UCLP).

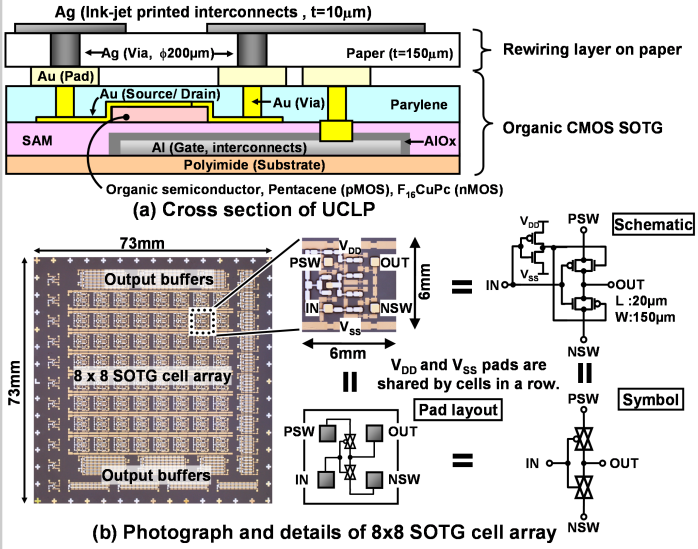


Figure 7.3.2: Cross section of UCLP and derails of SOTG.

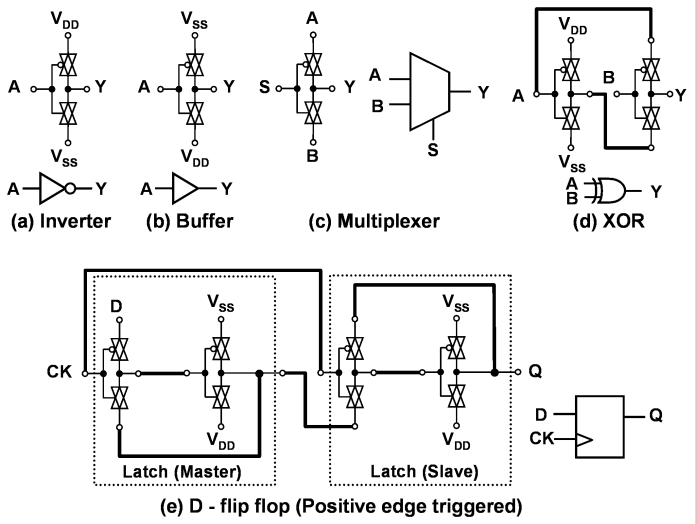


Figure 7.3.3: Examples of logic implementation with SOTG.

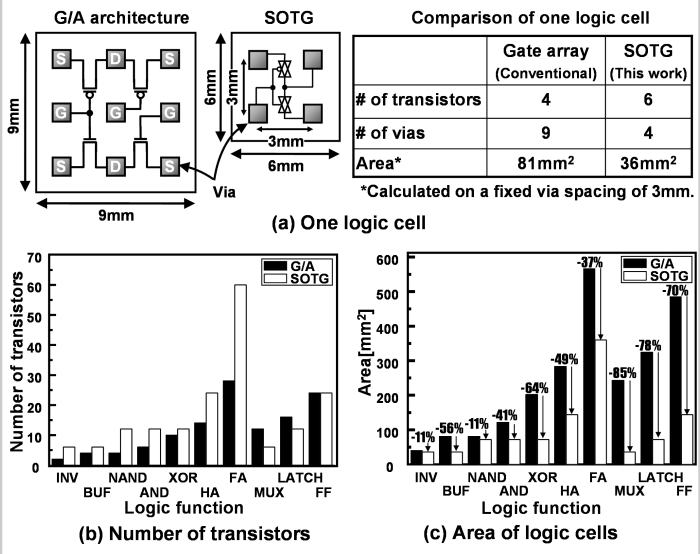


Figure 7.3.4: Gate array architecture and SOTG.

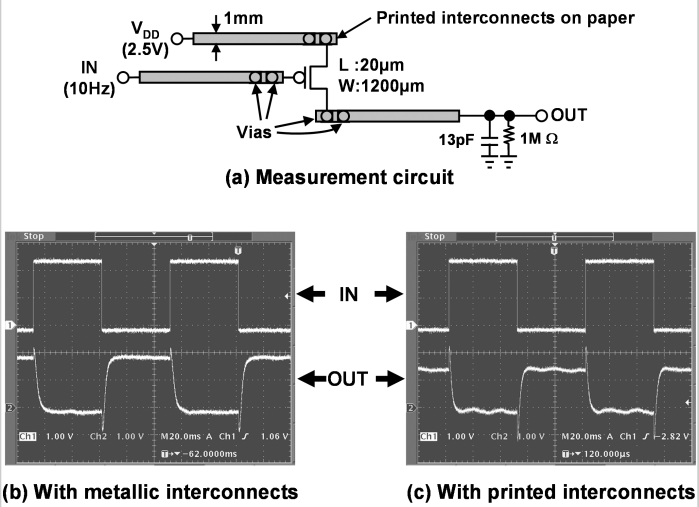


Figure 7.3.5: Measured waveforms of organic transistor.

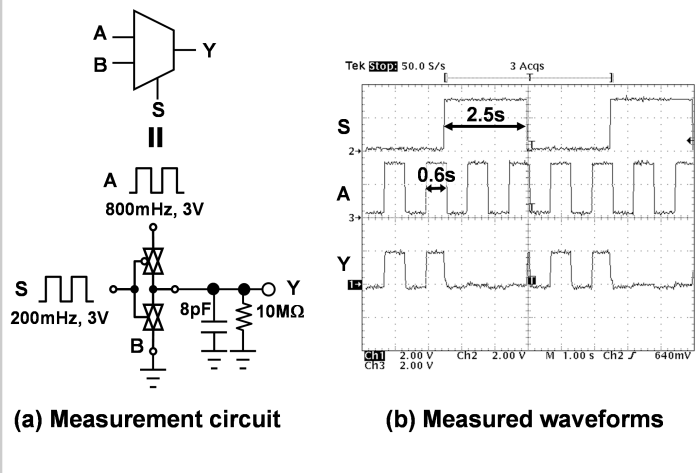
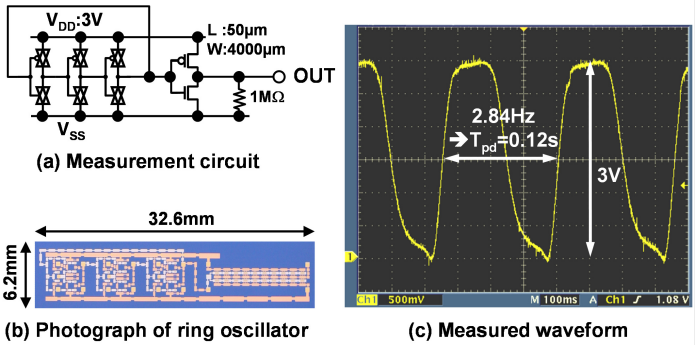


Figure 7.3.6: Measured waveforms of two-input multiplexer.



(a) Measurement circuit

(b) Photograph of ring oscillator

(c) Measured waveform

Figure 7.3.7: Photograph and measured waveform of SOTG ring oscillator.

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