0.18-V Input Charge Pump with Forward Body Biasing in Startup Circuit using 65nm CMOS

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***Abstract*- In this paper, a 0.18-V input three-stage charge pump circuit applying forward body bias is proposed. In the developed charge pump, all the MOSFETs are forward body biased by using the inter-stage/output voltages. By applying the proposed charge pump as the startup in the boost converter, the lower kick-up input voltage of the boost converter can be achieved. To verify the circuit characteristics, four test circuits have been implemented by using 65nm CMOS process. The measured available output current of the proposed charge pump under 0.18-V input voltage can be improved more than 150%. In addition, the boost converter can successfully been boosted from 0.18-V input to the 0.74-V output under 6mA output current. The proposed circuit is suitable for extremely low voltage applications such as harvesting energy sources.**

I. INTRODUCTION

Recently, there has been an increasing demand for portable energy sources harvesting the energy from the surrounding environment to implement the self-powering and long lasting portable electronic devices. However, the output voltage provided from harvesting energy source is usually low and requires to be converted to a higher supply voltage by using the up-conversion power management circuits. In advanced CMOS technology, even the threshold voltage of the MOSFET has been scaled to lower than 400mV, operating the circuit under 0.5V with high performances is still a tough task.

Until now, several low input voltage boost converter systems have been reported [1]-[4]. These converters applied the startup mechanisms such as providing an additional high voltage battery [1] or a mechanical vibration switch [2] to kick-up the boost converter. The others use SOI process [3] or standard CMOS process [4] to implement the low voltage startup circuit to kick-up from low input voltage. To avoid additional components, realizing a low-voltage startup circuit by using CMOS technology is necessary.

In this paper, an ultra low input voltage charge pump circuit is proposed and fabricated using 65nm standard CMOS technology. The proposed circuit is implemented by using three-stage charge pump circuit based on voltage doubler structure. It applies forward body bias to every MOSFETs by feedback the voltage from the ground, inter-stage and the output voltages. From the measurement results, the proposed charge pump circuit can provide more than 150% output current comparing to the conventional ones in 0.18-V input voltage. It is suitable to implement as a part of startup circuit for low voltage operation.

To verify the characteristics of charge pump circuit, we implemented the boost converter together with the startup circuit utilizing the charge pump circuit to generate the DC voltage for clock generator. The measurement results show that the boost converter can successfully been boosted from 0.18-V input to the 0.74-V output. When the output voltage of the boost converter is boosted up to 0.65 V, it is sufficient to drive the feedback circuit of the boost converter by using its output voltage [1].

This paper is organized as follows. In Section II, the topology of the proposed three-stage charge pump circuit with forward body bias is described. The boost converters integrated with the startup circuit are presented in Section III. The experimental results are shown in Section IV. Finally, conclusion will be drawn in Section IV.

II. PROPOSED CHARGE PUMP CIRCUIT

Historically, most of the charge-pump circuits are based on the Dickson type charge pumps [5] as shown in Fig.1. The diode connected MOSFET makes the switch function as a diode and the output current degrades violently at low supply voltages. For low voltage applications, the circuit structure of the proposed charge pump circuit is based on the voltage doubler [6], which is shown in Fig. 2. It is realized by using a cross coupled switches driven by output of phase clocks.

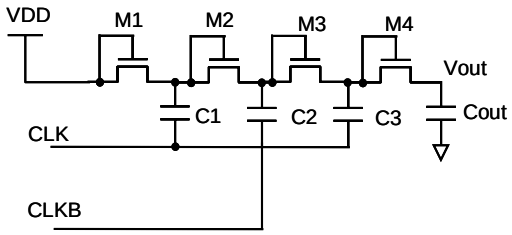

Fig.1. The circuit schematic of the 3-stage Dickson charge pump circuit.

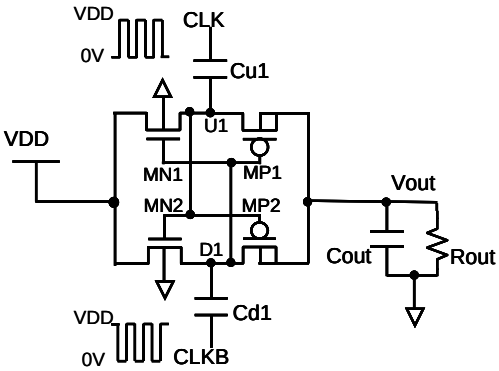

Fig.2. The circuit schematic of the conventional voltage doubler.

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When the CLK is high, the MN2 and MP1 turns on and the node D1 is charged to VDD. When the CLK changes from high to low, the MN1/MP2 turns on and the node U1 is charged to VDD. The node D1 is driven by the capacitor Cd1 and boost from VDD to 2VDD while charging the node Vout at the same time. On the next half cycle, the node D1 becomes to VDD and the node U1 is also pumped to 2VDD which is also charged to node Vout. As a result, the node Vout can always been charged to 2VDD.

The 3-stage charge pump circuit based on the conventional voltage doubler is shown in Fig. 3. Since the deep n-well is available in this process, the body of the nMOSFET is connected to the source terminal to avoid the body effect. The operation of the inter-stage output voltages Vo1 and the Vo2 are described as follows. When the CLK is high, the MOSFETs MP1/MN4 turn on and the Vo1 is charged to 2VDD from the node U1 to D2. On the other half cycle, the MP2/MN3 turn on and the Vo1 is also charged to 2VDD. The node Vo2 is operated likewise and can be pumped to 3VDD. As a result, each of the inter-stage voltage can be pumped to a fixed DC value.

The targeted input voltage of the charge pump circuits is 0.18V, where the MOSFET is operating under the cut-off region and is charged by leakage current. In addition, the large on-resistance of the MOSFETs cause voltage drops and decrease the output voltage, especially when the load requires larger current. To alleviate this problem, we proposed the charge pump circuit which applies the forward bias to each MOSFET, as shown in Fig. 4. Since the source terminal of each MOSFET is pumped to different voltage, the three-stage charge pump circuit requires six different voltages to provide the forward bias. However, it is very difficult to generate six different voltages.

In the proposed circuit, each body of nMOSFET is biased to the next stage output (i.e. 2nd stage nMOSFETs are biased from 3rd output voltage Vout) and each body of pMOSFET is biased to the input voltage of previous stage t(i.e. 2nd stage pMOSFETs are biased from 1st input voltage VDD). In case of pMOSFETs in the first stage, since there is not any previous stage, the bodies of the pMOSFETs are connected to ground. In case of nMOSFETs in the third stage, we added an additional stage with less than 1.5% area overhead to provide the forward bias.

In the proposed circuit, all of the forward biases are provided by the self-pumped voltage or the ground by only adding an additional charge pump stage. This stage is implemented by using two small capacitor and MOSFETs with less than 1.5% area overhead since it is only used to provide the forward bias.

The proposed charge pump circuit degrades the threshold voltage of the MOSFET to improve the low-voltage characteristics. Comparing to the conventional charge pump circuit, the proposed one can remain high output voltage even the output current increase. It is particularly worthy noting that this improvement becomes much more significantly when the circuit is operating under low input voltage.

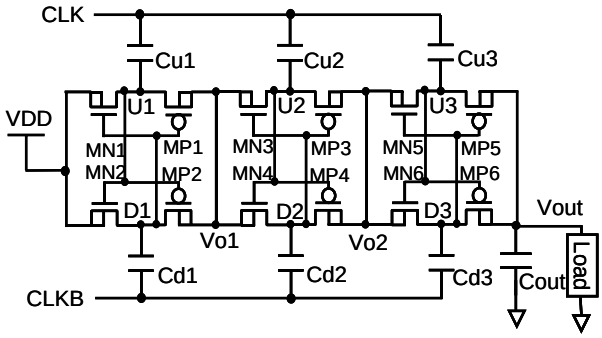

Fig.3. 3-stage charge pump circuit without forward body bias

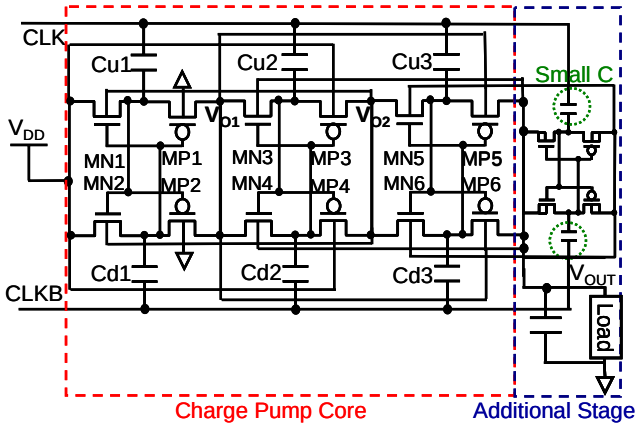

Fig.4. Proposed 3-stage charge pump circuit with forward body bias

III. LOW STARTUP VOLTAGE BOOST CONVERTER

To kick-up the boost converter from low input voltage, it is required to drive the power MOSFET with high duty cycle for charging the output capacitance. If the boost converter is required to boost from 0.18V input to 0.7-V output, the clock amplitude should be larger than 0.5-V which is higher than threshold voltage of the MOSFET. In addition, the duty cycle of 80% is also required. One of the available methods to generate such a clock signal is applying the DC-DC converter to up-conversion the 0.18-V input voltage to the 0.5-V output. Delivering this output power to the clock generator can generate the 80% duty 0.5-V V_{P-P} clock signals. The Fig.5 shows the system diagram of the proposed boost converter. It consists from a charge pump circuit, a clock generator, and a boost converter. In order to generate the 0.5-V output voltage under relative large output current, the charge pump applies the three-stage charge pump circuit which is described in previous section. The proposed charge pump circuit is driven by the 0.18-V supply voltage and 0.18-V clock signal. In addition, the input voltage of the boost converter is also provided from the input power supply.

Fig. 6 shows the detail circuit schematics of the boost converter and the clock generator. The clock generator consists from the ring oscillator, 80% duty cycle generator and buffer chains to drive the power switches of the boost converter.

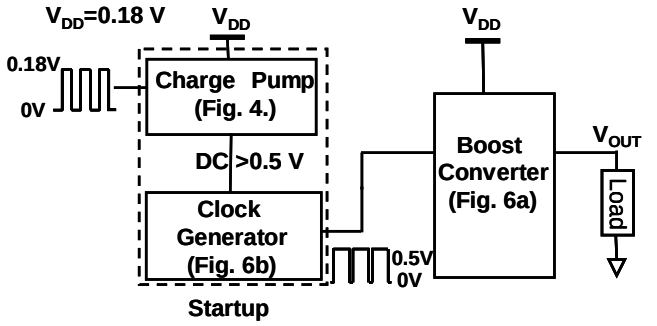

Fig.5. Block diagram of the boost converter applying proposed charge-pump type startup circuit

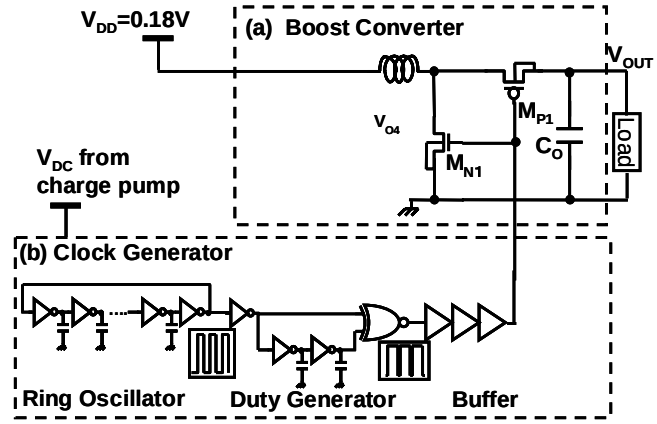

Fig.6. Circuit schematics of the (a) boost converter and (b) clock generator

The most critical part of the startup circuit is the low voltage charge pump circuit. Due to the high threshold voltage comparing to input, it is difficult to extract the enough current. Moreover, since the available output current of the charge pump circuit is proportional to the pumping capacitances, the capacitance area of the pumping capacitors can be reduced for fixed output current. Applying this architecture, the boost converter can be triggered from 0.18-V input voltage and the output voltage can be up-converted. When the output voltage of the boost converter is boosted to higher than 650 mV [3], the control circuitry can be driven by the output of the boost converter and the startup circuit including the charge pump can be stopped. Therefore, the power consumption caused by the startup circuit is ignorable and will not affect the operation efficiency of the boost converter.

IV. EXPERIMENTAL RESULT

In this work, a test chip has been designed and fabricated using 65nm standard CMOS technology. It includes a 3-stage conventional charge pump circuit based on voltage doubler, a proposed 3-stage charge pump circuit, a boost converter integrated with startup circuit utilizing a conventional charge pumps and a boost converter integrated with proposed startup circuit. The chip microphotograph of the test chip is shown in Fig. 7 and the proposed charge pump circuit is shown in Fig. 8.

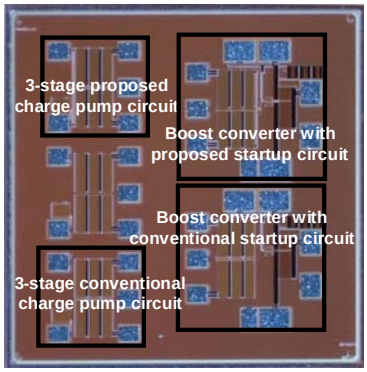

Fig.7. Photographs of the charge pump circuits and the boost converters integrated with the startup circuits.

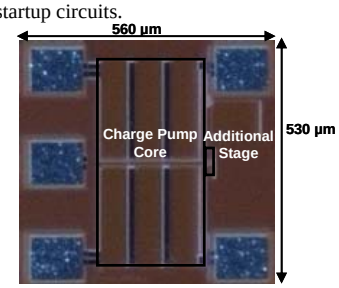

Fig.8. Photographs of the proposed charge pump circuits with applying a small additional stage. (Area overhead is less than 1.5%)

In the charge pump circuit, each pumping capacitor of the charge pump core and the additional stage is 12.3pF and 0.4pF, respectively and the clock frequency is 10 MHz. The total area overhead of the additional stage is less than 1.5%.

The measured output voltages of conventional and proposed charge pump circuit with 0.18-V input voltage is shown in Fig. 9. As can be seen, the proposed charge pump circuit has better pumping performance especially when the output current increases. Fig. 10 compares the measured output current of the conventional and proposed charge pump circuit with 0.5-V output voltage as supply voltage increases. The output current improves 150% when the input voltage is 0.18V. The improvement becomes more significantly as the input voltage is lower. Although applying forward bias requires considering the latch-up issues, the proposed circuit does not latch-up during the measurement.

The measurement results of the boost converter integrated with the conventional or proposed charge pump circuit are shown in Fig. 11. The boost converter integrated with the proposed charge pump circuit can boost the 0.18-V input voltage to 0.74-V output with 6-mA output current while the conventional one cannot boost the output voltage.

The comparison of the power management circuits for energy harvesting applications are shown in Table I. The boost converter in [1] and [2] can startup from extremely low input voltage. However, they require external high supply voltage or a mechanical switch. The startup circuit in [3] and [4] are implemented by using the CMOS technology. However, the startup voltage is still very high. The proposed circuit provides a solution to startup the boost converter from very low input voltage without using the external high voltage or mechanical switches.

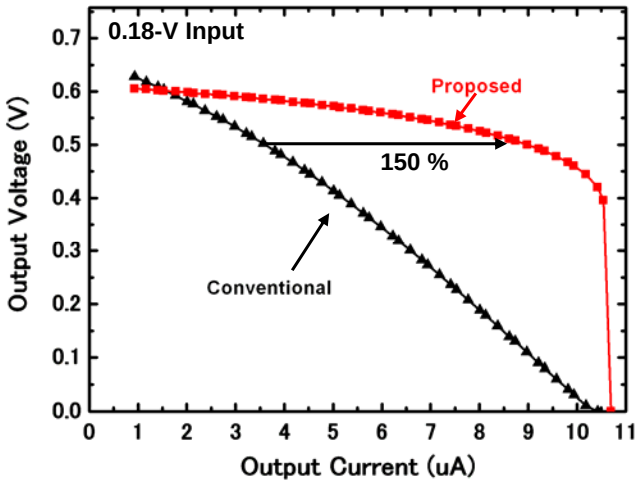

Fig.9. Measured output voltages of the proposed and conventional charge pump circuit with 0.18-V power supply.

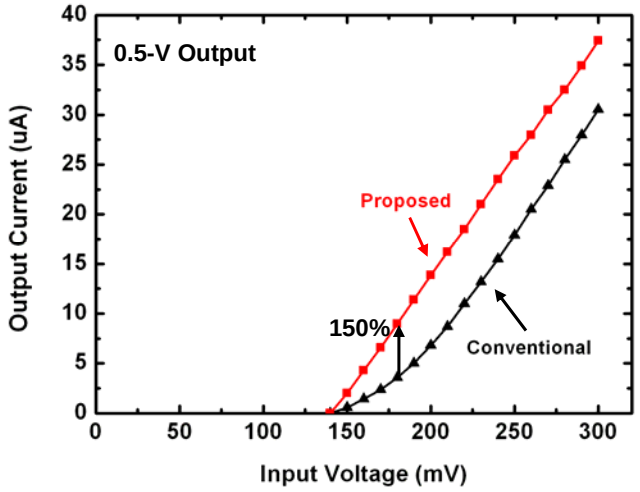

Fig.10. Measured output current of the proposed and conventional charge pump circuits with 0.5-V output voltage as supply voltage increases.

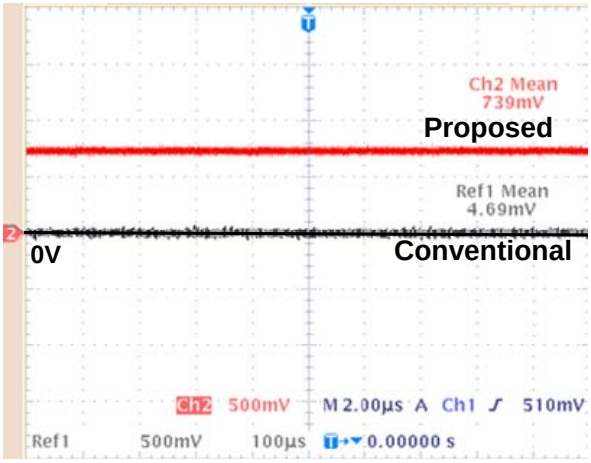

Fig.11. Measured output voltage of the boost converter with startup circuit under 0.18-V power supply and 6-mA output current.

TABLE I
COMPARISON OF RECENTLY PUBLISHED BOOST CONVERTERS APPLYING STARTUP MECHANISM

Reference	[1]	[2]	[3]	[4]	This Work
Process	130nm CMOS	350nm CMOS	350nm SOI BCD	600nm CMOS	65nm CMOS
Min. Input Voltage	0.02V	0.02V	0.36V	1V	0.18V
Output Voltage	1V	1.8V	3.6V	1.5V	0.74V
Note	External voltage (0.65V) is required	Mechanical switch is required	Separate start-up IC Is required	1-chip integration	1-chip integration

V. CONCLUSION

To kick up the boost converter in low operation voltage, the charge pump circuit with forward body biasing is proposed. Because of applying the appropriate forward bias to each MOSFET, the pumping efficiency can be improved than conventional charge pump without applying forward bias. The experiment results show that the proposed charge pump can improve the output current more than 150% with 1.5% area overhead. The boost converter connected with the proposed charge pump can kick up the 0.18-V input to 0.74-V output while the conventional one only provides 4.7mV output. With the higher pumping ability and the lower kick-up voltage, the proposed charge pump circuit is more suitable for energy harvesting applications which only provide low voltages.

ACKNOWLEDGMENTS

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