A 1-V Input, 0.2-V to 0.47-V Output Switched-Capacitor DC-DC Converter with Pulse Density and Width Modulation (PDWM) for 57% Ripple Reduction

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***Abstract*—To effectively reduce output ripple of switched-capacitor DC-DC converters which generate variable output voltages, a novel feedback control scheme is presented. The proposed scheme uses pulse density and width modulation (PDWM) to reduce the output ripple with low output voltage. The prototype chip was implemented using 65nm CMOS process. The switched-capacitor DC-DC converter has 0.2-V to 0.47-V output voltage and delivers 0.25-mA to 10-mA output current from a 1-V input supply with a peak efficiency of 87%. Compared with the conventional pulse density modulation (PDM), the proposed switched-capacitor DC-DC converter with PDWM reduces the output ripple by 57% in the low output voltage region with the efficiency penalty of 2%.**

I. INTRODUCTION

For emerging ultra-low power SoCs which utilize near-threshold or sub-threshold supply voltages and draw less than 10mA of current [1-2], a switched-capacitor (SC) DC-DC converter is a viable choice for its tunable output voltage and the probability of on-chip full integration [3]. However, the previously reported SC DC-DC converters [3-6] often overlook the effect of output ripple on the sub-threshold digital circuits.

With the trend of the power supply voltage (V_{DD}) scaling, power supply ripple is extremely detrimental to their digital building blocks. This is because the delay of logic circuits is influenced by V_{DD} in an exponential way in the sub-threshold region. The net result is that a very small amount of injected ripple can cause a very large delay uncertainty. Fig. 1 clearly shows such impact of power supply ripples (V_{Ripple}) on the frequency of an FO4-per-stage ring oscillator. The central frequency f_{center} is obtained at V_{DD} = 200 mV. The upper and lower bounds of the frequency, i.e., f_{max} and f_{min}, are obtained at V_{DD} = 200mV + V_{Ripple}/2 and V_{DD} = 200mV - V_{Ripple}/2, respectively. Note that in Fig. 1, f_{max} and f_{min} are normalized to f_{center}. As seen, an 80 mV ripple can result in a more than 200% delay uncertainty.

In the super-threshold region, the ripple of the DC-DC converter and ground-bounce noise (also referred to as Ldi/dt noise) are two major sources of power supply noise at digital blocks. As V_{DD} scales to the sub-threshold region, the transient current of digital blocks also scales rapidly, in this way mitigating the ground-bounce noise. However, the problem of the ripple of the DC-DC converter remains and it even goes severer with the decreasing output voltage.

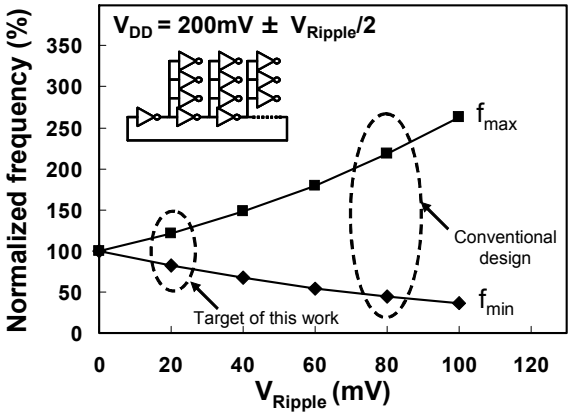

Fig. 1. Normalized ring oscillator frequency at different power supply ripples and the target of this work.

Motivated by the above concerns, it is of great importance to look for solutions which can reduce the output ripple of switched-capacitor DC-DC converter which supplies variable output voltages to the sub-threshold digital circuits. Interleaving techniques can also be employed for lower ripples [7], however, this method comes with the cost of increased component count and complicated timing control. Therefore, exploring a more effective control scheme to reduce output ripple of switched-capacitor DC-DC converter with the variable output voltages for sub-threshold digital circuits is the focus of this study.

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II. Proposed PDWM Control Scheme of SC DC-DC Converter

Fig. 2 shows the architecture of the SC DC-DC converter with conventional pulse density modulation (PDM). The core of the system is a switch matrix which contains the charge-transfer capacitors and the charge-transfer switches. A PDM based control scheme is used to regulate the output voltage to the desired value with a suitable clock density. The PDM works as follows: a comparator clocked by the clock (CK) is used to compare V_{OUT} and V_{REF}. When the output voltage V_{OUT} is above V_{REF}, the output of comparator, CK_{pulse} is set to 0, which means switching signals ϕ_{CK} and ϕ_{CKB} are paused. When V_{OUT} falls below V_{REF}, the comparator triggers a pulse on CK_{pulse}, which will be transported to ϕ_{CK} and ϕ_{CKB}, thus charges up the output load capacitor. The non-overlap clock generator is used to prevent any overlap between ϕ_{CK} and ϕ_{CKB}. The clock buffers are employed to provide drive ability to the switches in the switch matrix.

With the PDM control scheme, pulse densities of ϕ_{CK} and ϕ_{CKB} are effectively adjusted. The switches are switched less frequently as I_{OUT} decreases, thereby reducing the switching losses and the power consumed by control circuit. With the PDM control scheme, this converter is able to achieve a high power efficiency with a wide output current range.

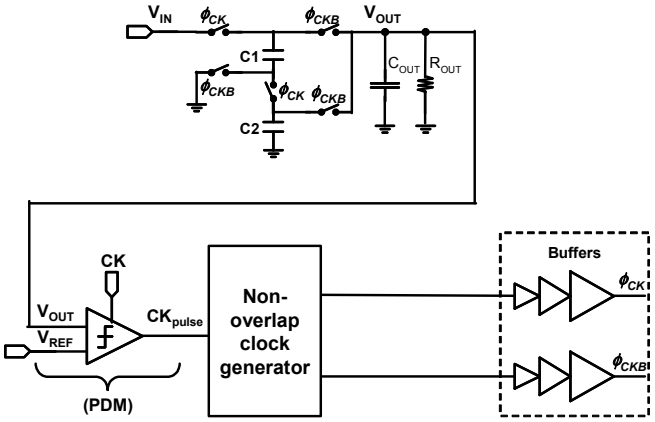


Fig. 2. Schematic of conventional method with only PDM.

However, the conventional PDM architecture suffers from the problem of large ripple at low output voltage region. Fig. 3 shows the proposed architecture which employs both PDM and pulse width modulation (PWM) in the control scheme. In the proposed scheme, a pulse width control block and a look up table (LUT) are introduced to the control circuit. Only one of the switches connected to V_{IN} is controlled by a modulated pulse signal ϕ_{PW}, because by controlling the pulse width of this switch, the power transferred from V_{IN} to the capacitors at every circle can be precisely controlled. The pulse width of ϕ_{PW} is modulated by the pulse width control block. A 4-bit control signal is read from a LUT to determine the pulse width for ϕ_{PW}, according to different I_{OUT} and V_{OUT}.

Figs. 4 (a) and (b) show the waveform of conventional method with different V_{REF}'s, and Figs. 4 (c) and (d) show proposed method. By comparing Figs. 4 (a) and (b), it is observed that lower V_{REF} causes bigger ripple, because V_{OUT}

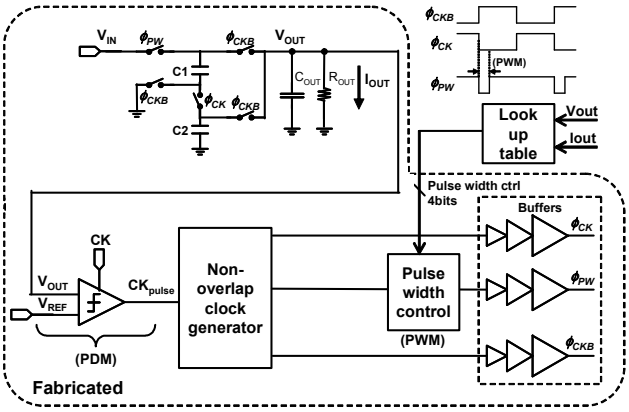


Fig. 3. Schematic of proposed method with PDWM.

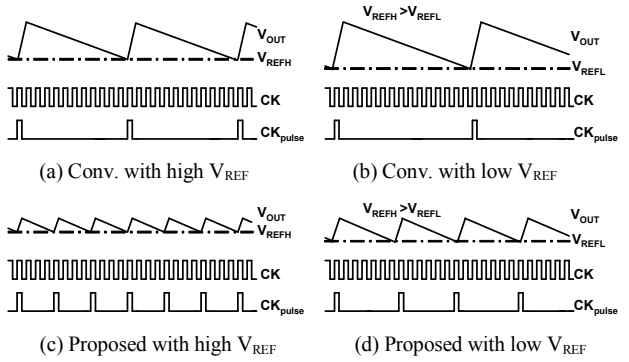


Fig. 4. Waveforms of conventional and proposed method. (a) conventional PDM with high V_{REF}, (b) conventional PDM with low V_{REF}, (c) proposed PDWM with high V_{REF}, (b) proposed PDWM with low V_{REF}.

is charged to a $V_{IN}/2$ at every pulse of CK_{pulse}. This implies that the ripple problem goes severer with the decreasing V_{REF}. On the other hand, as shown Figs. 4 (c) and (d), proposed PDWM has a much lower ripple due to the PWM control. Because variable pulse width can be applied to drive ϕ_{PW}, shown in Fig. 3, V_{OUT} is now able to be charged to a lower value than in Figs. 4 (a) and (b), thus reduce the ripple significantly.

Fig. 5 shows the pulse width control circuit of propose DC-DC converter. The pulse width is controlled by a delay generator, with a 4-bit digital input signal. Post-layout simulation results show that the pulse width control circuit generates an output with pulse width from 2.7ns to 32.8ns, with 2.1-ns step.

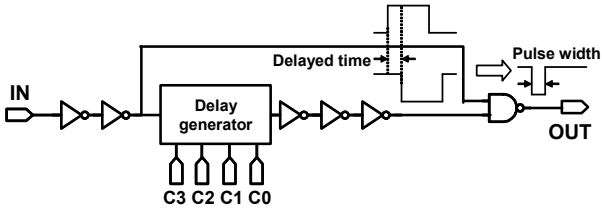


Fig. 5. 4-bit pulse width control circuit.

III. Measurement Results and Discussion

The proposed SC DC-DC converter is fabricated with 65nm CMOS process, except for the LUT as shown in Fig. 3. Capacitors C_1, C_2, and C_{OUT} shown in Fig. 3 are implemented using off-chip ceramic capacitors with values of 4.7nF, 4.7nF, and 47nF, respectively. Fig. 6 shows the chip micro-photograph and the layout. The active area of the DC-DC converter is 0.074mm^2.

Fig. 7 shows the measured dependence of the power efficiency on the output current at 0.47-V output voltage. The DC-DC converter delivers 0.25mA to 10mA output current from a 1V input supply, with an efficiency higher than 82%, and a peak value of 87%.

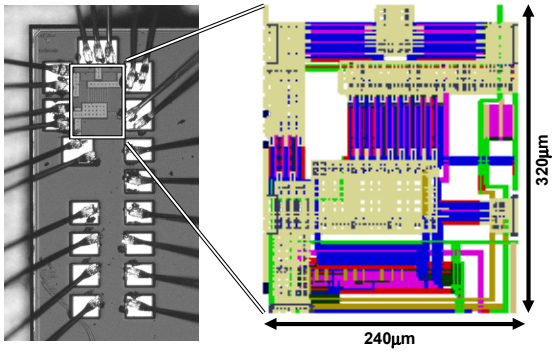


Fig. 6. Chip microphotograph and layout.

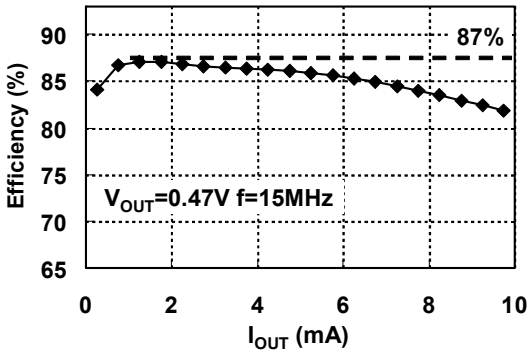
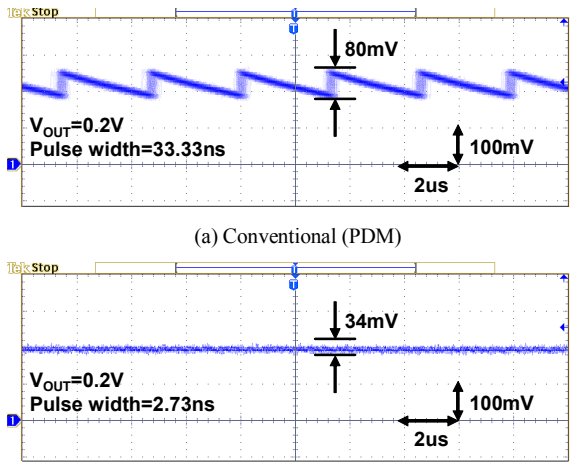


Fig. 7. Measured efficiency v.s. output current with proposed PDWM.

Fig. 8 shows the measured transient waveform of V_{OUT} of both conventional and proposed DC-DC converters with 0.2-V output voltage and 1-mA output current. Significant ripple reduction is achieved by the propose DC-DC converter.

Fig. 9 shows the measured output ripple with different pulse width. The conventional PDM with a 15MHz clock (equals to 33.3ns pulse width) is shown in the right of the graph. As seen, compared with the conventional PDM, the proposed PDWM greatly suppresses the output ripple, especially with low output voltage region, because the pulse width of PDM is too wide for transporting required power to the output. Fig. 10 shows the same measured ripple of Fig. 9, with regarding to power efficiency. The degradation of efficiency with lower output voltage is due to the series resistance of output switches, which can be alleviated by sizing the output switches at different output voltage. As shown in Fig. 10, the ripple is reduced by narrowing the pulse



(a) Conventional (PDM)

(b) Proposed (PDWM)

Fig. 8. Measured transient waveform of V_{OUT} of conventional DC-DC converter and proposed DC-DC converter.

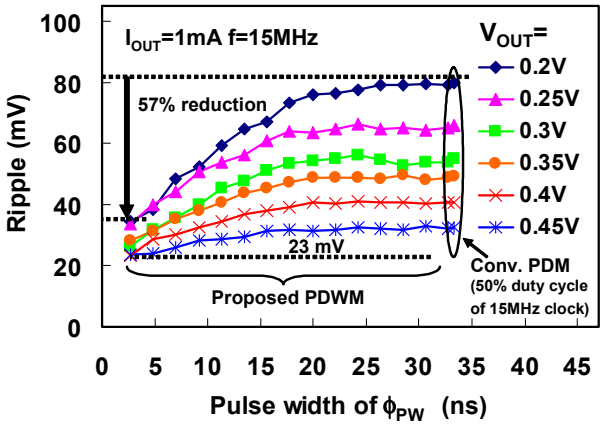


Fig. 9. Measured ripple v.s. pulse width with various V_{OUT}.

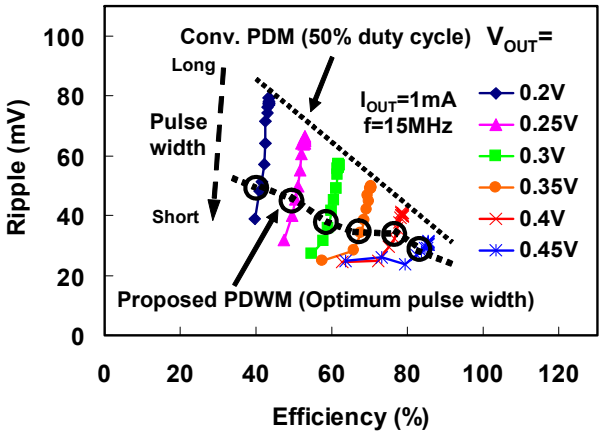


Fig. 10. Measured ripple v.s. power efficiency with various V_{OUT}.

width, at the cost of slightly degraded power efficiency. That is because narrowing the pulse width also increases the pulse density, thus increases the power consumption slightly. Therefore, a group of practical optimum choice on pulse width was defined by allowing a 2% degradation on power efficiency as shown in Fig. 10.

The measured optimum pulse width for different I_{OUT} and V_{OUT} is shown in Fig. 11. As observed, the optimum pulse width tends to increase with increasing I_{OUT} and V_{OUT}, because there is a larger need of power delivered by the switch matrix, thus demanding a wider pulse on the switch. The selected pulse width information is then stored in the LUT. Therefore, for different I_{OUT} and V_{OUT}, the SC DC-DC converter will be configured to the optimum output ripple and power efficiency.

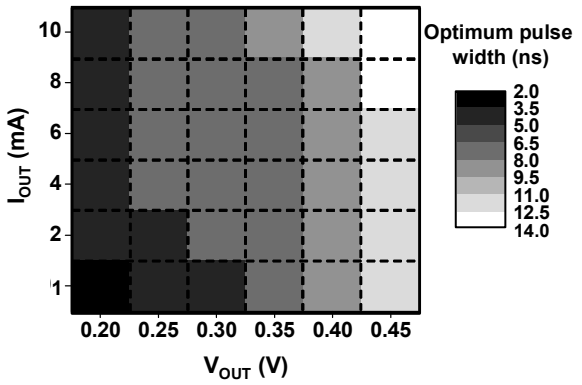


Fig. 11. Contour of optimum pulse width with regarding to I_{OUT} and V_{OUT}.

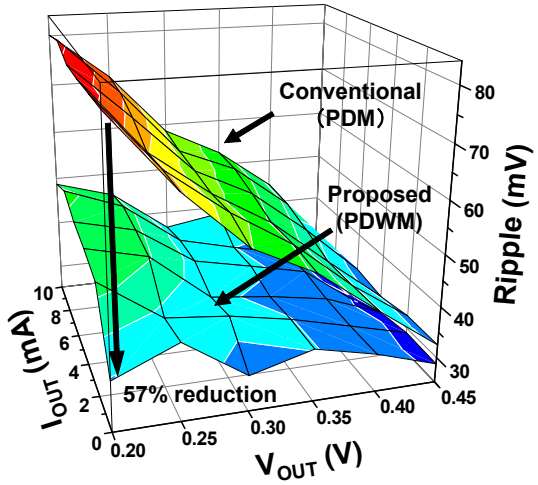


Fig. 12. Measured ripple of conventional and proposed DC-DC converters with regarding to I_{OUT} and V_{OUT}.

TABLE I. PERFORMANCE SUMMARY OF THE PROPOSED CONVERTER

Process	**1.2V 65-nm CMOS**
Active area	**0.074 mm^2**
Clock frequency	**15MHz**
Input voltage	**1V**
Output voltage	**0.2~0.48V**
Output current	**0.25~10mA**
Max efficiency	**87%**
Min output ripple	**23mV**

Fig. 12 shows the measured output ripple of conventional and proposed PDWM DC-DC converters with regarding to I_{OUT} and V_{OUT}. Significant reduction of the output ripple is observed in the whole range of I_{OUT} and V_{OUT}. Moreover, the output ripple is more effectively reduced in low output voltage region (to a peak of 57%). Recall that ripple has a larger impact on digital circuits at a lower voltage, the proposed DC-DC converter provides a promising solution for sub-threshold digital circuits. The performance the proposed PDWM SC DC-DC converter is summarized in Table I.

IV. CONCLUSION

A SC DC-DC converter with PDWM control scheme for high power efficiency and low output ripple is proposed and implemented using 65nm CMOS process. A control scheme using both PDM and PWM is introduced to enable a high efficiency with wide output current range, and suppress the output ripple with low output voltage, respectively. The proposed SC DC-DC converter has 0.2-V to 0.47-V output voltage and delivers 0.25-mA to 10-mA output current from a 1-V input supply with a peak efficiency of 87%. Compared with the conventional PDM, the proposed SC DC-DC converter with PDWM reduces the output ripple by 57% in the low output voltage region with the efficiency penalty of 2%.

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