0.6V Voltage Doubler and Clocked Comparator for Correlation-based Impulse Radio UWB Receiver in 65nm CMOS

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***Abstract*—This paper presents a 0.6-V voltage doubler and a 0.6-V clocked comparator in 65nm CMOS. For the multi-phase sampling application, such as charge-domain correlator for impulse UWB receivers or analog-to-digital converter, the proposed voltage doubler can reduce the power consumption and the chip area by half compared to the conventional one. The non-overlapping complementary clock generator used in the conventional voltage doubler can be eliminated by simply swapping the input clock order in the voltage doubler. The proposed 0.6-V clocked comparator can operate at 100-MHz clock with the proposed voltage booster.**

I. INTRODUCTION

The market and the need to develop efficient electronic equipment have pushed the industry to design circuits with very low power supply voltage, and also often constrained to low power consumption. This work targets to develop a 0.6V voltage doubler and a 0.6V clocked comparator for the multi-phase sampling application, such as correlation-based ultra-wideband (UWB) receiver or analog-to-digital converter (ADC).

As an application example, the proposed voltage doubler and the clocked comparator are used for the impulse UWB receiver. Impulse UWB refers to a radio technology for transmitting information by means of extremely short duration pulses without radio frequency modulation. Ideal targets for impulse UWB system are low power, low cost, high data rates, and extremely low interference, which makes it an attractive option for ad hoc and sensor network where groups of wireless terminals are located in a limited area and communicate in an infrastructure-free fashion without any central coordinating unit or base-station.

Conventional impulse UWB transceivers usually require 1.2V supply voltage or above [1-3]. However, in the single solar cell powered ad hoc and sensor network, the maximum available supply voltage is less than 0.6V. Figure 1 shows the application of the proposed circuits in the impulse UWB receiver. To verify the performance of the proposed 0.6V voltage doubler and the 0.6V clocked comparator, the 1.2V sampling clock generator and the synchronization control circuits are also implemented in the same chip.

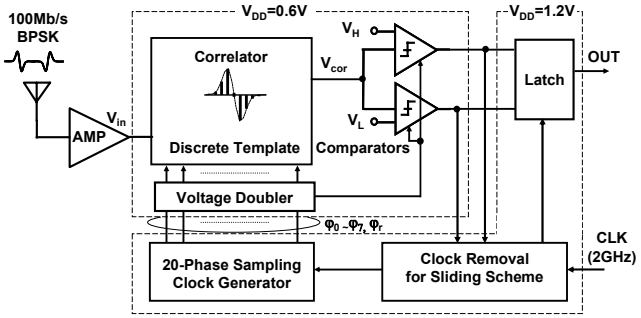

Figure 1. Block diagram of inpulse radio UWB receiver. 0.6-V voltage doubler supplies boosted voltage to charge-domain correlator and comparator.

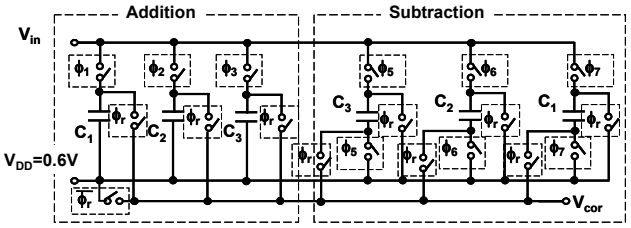

Figure 2. Charge-domain sampling correlator.

Section II presents the circuit implementations of the voltage doubler. The 0.6V voltage comparator is described in Section III. Experimental results are presented in Section IV and Section V concludes the paper.

II. VOLTAGE DOUBLER

Figure 2 shows the circuit schematic of the charge-domain sampling correlator used in the UWB receiver [2]. The sampling correlator circuits make use of two basic building

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blocks, namely the capacitor and the switch. Lowering the supply voltage of the correlator has implications on the operation of some building blocks. The functional property of a capacitor, namely its capacitance, is in fact independent of the supply voltage. The most problematic issue in low voltage sampling correlator design is the switch driving problem. One effective way to cope with the low supply is to apply voltage multiplication. This technique uses circuits which convert the voltage from the available supply to another one. The conversion factor is larger than unity and the up-converted voltage is a multiple of the available supply voltage.

A. Conventional Voltage Doubler

Various circuits have been proposed and used in literature to implement voltage multiplication. Originally monolithic voltage multipliers stem from non-volatile memory circuits where a relatively high potential is needed to write or erase information [4]. A conventional voltage doubler from DRAM applications is found in [5] and shown in Fig.3 (a). The key feature of this voltage doubler is to use feedback technique to obtain a boosted voltage of $2V_{DD}$ even at low operating voltage. When one clock is high, the bootstrapped voltage is high enough to turn on the other NMOS, which charges the other capacitor to V_{DD}. In the next phase the roles are exchanged. This feedback technique can eliminate a voltage loss due to a threshold voltage of MOSFET.

The required clock signals used in the conventional voltage doubler can be generated by the non-overlapping complementary clock generator show in Fig.3 (b). This circuit takes a clock signal and generates a two-phase non-overlapping clock. The amount of separation is set by the delay through the NAND gate and the two inverters on the NAND gate output. When driving a large capacitance, where the rise time of the signals can be significant, a large number of inverters are required as part of the delay which will dominate the power consumption of the voltage doubler.

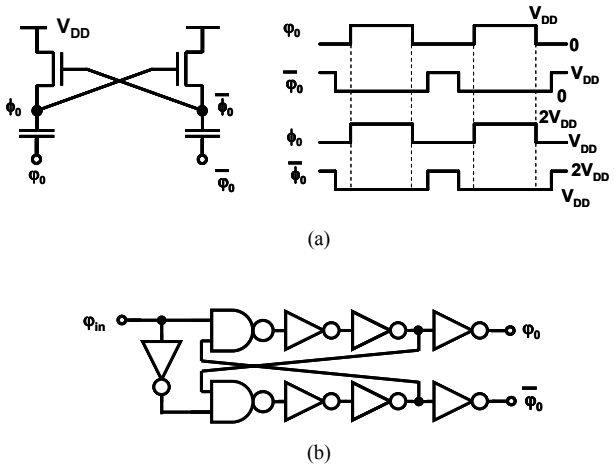


Figure 3. Conventional voltage doubler [5]. (a) Circuit schematic and waveforms. (b) Non-overlapping complementary clock generator.

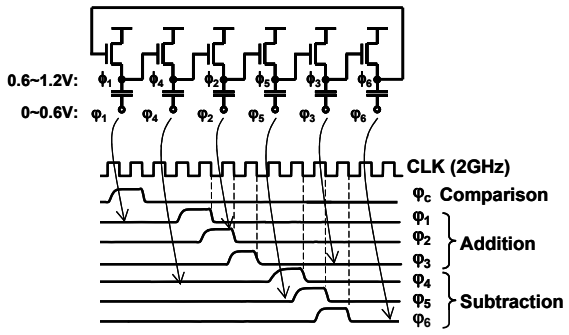


Figure 4. Simplified circuit schematic of the proposed voltage doubler for the sampling correlator.

B. Proposed Voltage Doubler

In the sampling correlator, the complementary clock signals are not required. If the conventional voltage doublers are directly used to generate the 20-phase sampling clocks for the correlator in Fig.1, half of chip area and power dissipation of the voltage doublers will be wasted due to the complementary clock signals. To overcome this problem, the proposed voltage doubler for the multi-phase sampling correlator is shown in Fig.4. The non-overlapping requirement on the adjacent input signals can be satisfied by simply swapping the clocks φ_1, φ_2, φ_3, φ_4, φ_5, φ_6 to φ_1, φ_4, φ_2, φ_5, φ_3, φ_6, thus eliminating the non-overlapping complementary clock generator.

III. CLOCKED COMPARATOR

Comparators are used for synchronization control and data decision in the proposed UWB receiver as shown in Fig. 1. For 0.6-V supply voltage, it doesn't suffice to force an existing circuit to operate at 100-MHz clock. It requires the development of dedicated circuits.

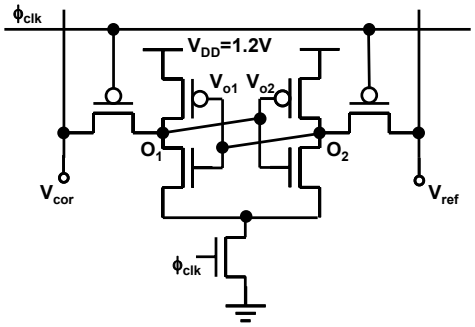
A. Conventional Clocked Comparator

Fig. 5 shows the circuit schematic and the simulated waveforms of the conventional clocked comparator [6] at 1.2-V power supply voltage. The reset is done to the meta-stable state and the regeneration is satisfied by two MOS inverters in positive feedback configuration. When clock is low, the drains of the two inverters (O_1, O_2) are charged to V_{cor} or V_{ref} (creating an imbalance). When clock goes high, the imbalance causes the circuit latch high or low depending on the state of the inputs. The conventional clocked comparator operates with 100-MHz clock at 1.2-V power supply voltage, while it fails to operate at 0.6-V power supply voltage.

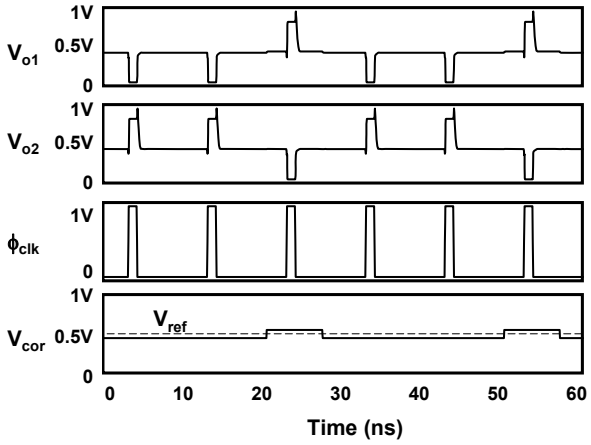
B. Proposed Clocked Comparator

To make the conventional clocked comparator operate at 100MHz with 0.6V supply voltage, in the proposed comparator, supply voltage is doubled from 0.6V to 1.2V when clock goes high. Figure 6 shows the complete circuit schematic of the proposed voltage doubler for both the sampling correlator and the clocked comparator where ϕ_1, ϕ_2, ..., ϕ_6 are used for the sampling clock of the correlator

and ϕ_{cmp} is used for the supply voltage of the comparator. Figure 7 shows the circuit schematic and the simulated waveforms of the proposed comparator. The proposed clocked comparator operates with 100-MHz clock at 0.6-V power supply voltage. When ϕ_{clk} is low, the circuit outputs are not valid logic signals but rather, ideally, track the input signals. This form of the latch has the advantage of lower power dissipation because no current is flowing when the latch is in reset mode.



(a)



(b)

Figure 5. Conventional clocked comparator [6]. (a) Circuit schematic. (b) Waveforms.

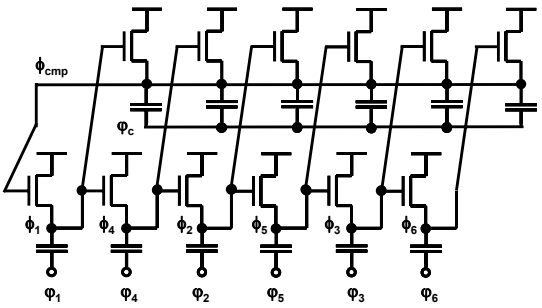
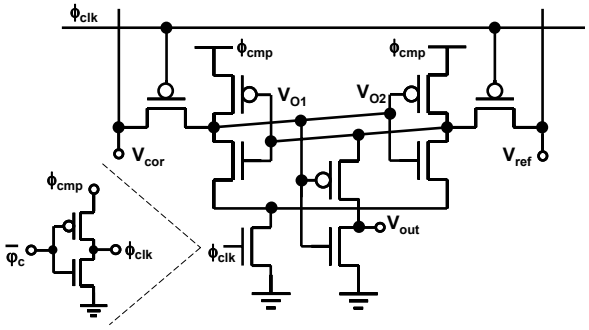
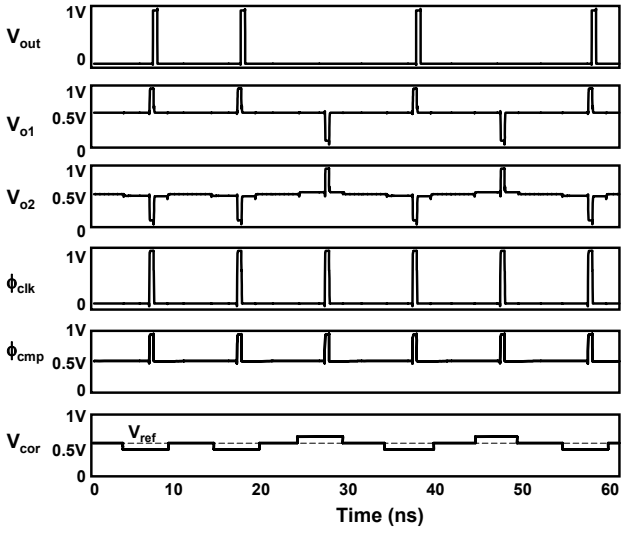


Figure 6. Complete circuit schematic of the proposed voltage doubler for both the sampling correlator and the clocked comparator.



(a)



(b)

Figure 7. Proposed clocked comparator. (a) Circuit schematic. (b) Waveforms.

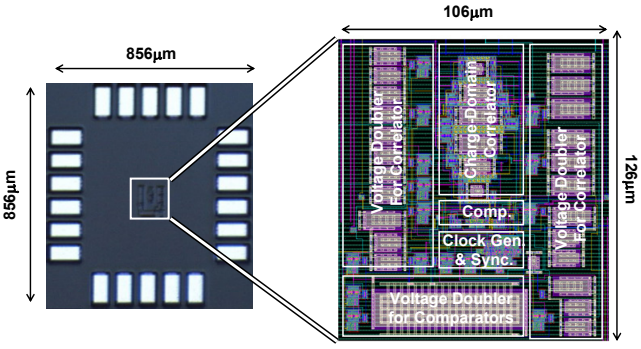
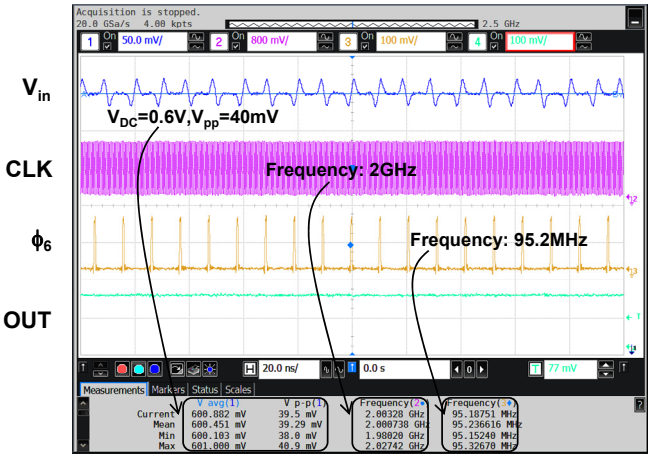


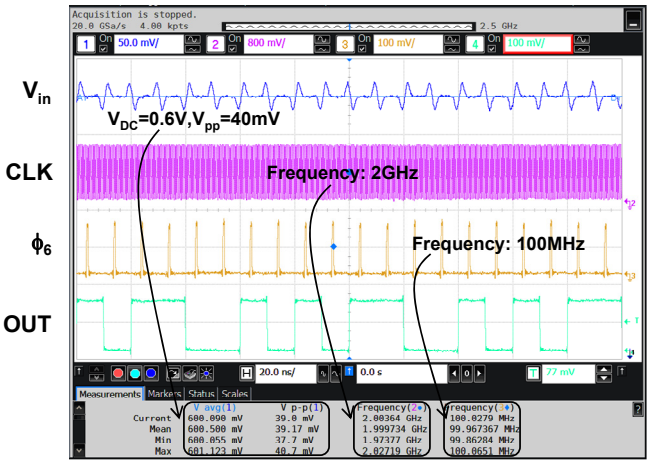
Figure 8. Chip micrograph and layout of UWB receiver.

IV. Measurement Results

The proposed UWB receiver without the front-end amplifier was designed and fabricated in 1.2V 65nm CMOS process. The chip micrograph and layout are shown in Fig. 8. To verify the performance of the proposed 0.6V voltage doubler and the 0.6V clocked comparator, the 1.2V level



(a)



(b)

Figure 9. Measurement results of UWB receiver. (a) Sliding scheme for timing alignment. (b) Measured waveforms in synchronization.

TABLE I. RECEIVER PERFORMANCE SUMMARY AND COMPARISON

		[2]	This Work
CMOS Technology		180nm	65nm
Supply Voltage		1.8V	0.6V,1.2V
Data Rate		100Mb/s	100Mb/s
Clock Frequency		2GHz	2GHz
Power	Correlator & Comparators	0.75mW @1.8V	0.05mW @0.6V
	Clock Gen. & Sync Control	0.53mW @1.8V	0.34mW @1.2V
	Total	1.28mW	0.39mW
Energy per bit		12.8pJ/bit	3.9pJ/bit
Core Area		5561 μm² (w/o Volt. Doubler)	13356 μm² (with Volt. Doubler)

outputs of the clock generator are down-shifted to 0.6V for the input in Fig. 1. Fig. 9 (a) shows the measured waveforms before synchronization is achieved, where V_{in} is the incoming UWB pulse, CLK is the 2GHz input clock, ϕ_6 is the sixth sampling clock and OUT is the output data. The same sliding scheme-based synchronization mechanism as [1] is used. Before synchronization is achieved, due to the clock-swallow sliding scheme, for every incoming UWB pulse one input clock is swallowed and the period of the sampling clock generator output is increased to 10.5ns which corresponds to the frequency 95.2MHz. Fig. 9 (b) shows the measured waveforms when synchronization is achieved. Because the sliding scheme for timing alignment is inactivated, the frequency of the sampling clock returns to 100MHz and the UWB receiver receives 100-Mbps data correctly.

The receiver performance is summarized in Table I. Compared to the conventional 1.8V UWB receiver [2], the total power consumption is reduced by three times. The power consumption of the correlator and the comparators is reduced by 93% (from 0.75mW to 0.05mW) by reducing the power supply voltage from 1.8V to 0.6V.

V. CONCLUSIONS

A 0.6-V voltage doubler and a 0.6-V clocked comparator are presented in 65nm CMOS. Compared to the conventional voltage doubler, the proposed doubler can reduce the required capacitance area by half and eliminate the non-overlapping complementary clock generator. The proposed 0.6-V clocked comparator can operate at 100-MHz clock with the proposed voltage booster. Compared to the conventional UWB receiver [2], the power consumption of the correlator and the comparators is reduced by 93% by reducing the power supply voltage from 1.8V to 0.6V.

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