3D Stacked Buck Converter with 15µm Thick Spiral Inductor on Silicon Interposer for Fine-Grain Power-Supply Voltage Control in SiP's

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***Abstract*-This paper proposes a 3D stacked buck converter with a 15µm thick spiral inductor on a silicon Interposer, which is suitable for fine-grain power-supply voltage control in SiP's. Our newly developed silicon interposer technology realizes a fine-pitch design rule (Line/Space=20µm/20µm, via hole diameter =30um) at the metal thickness of 15µm as well as conventional interposers with 5µm metal thickness. The measurement result shows that the 15µm thick inductor improves the power efficiency of the buck converter by 12% at the output current of 100mA compared with that by the conventional 5-µm thick inductor.**

I. Introduction

Space-domain fine-grain voltage engineering is a promising method for low-power high-performance VLSI circuit design with advanced CMOS technologies [1]. To realize fine-grain V_{DD} implementation, distributed power supplies with on-chip buck converters are required as shown in Fig. 1.

Conventional buck converters employ either off-chip discrete inductors or on-chip inductors. Off-chip inductors have low parasitic resistance. However, interconnects between LSI and the inductor tend to be long, and therefore, its parasitic capacitance and resistance are issues for the fine-grain power supply voltage (V_{DD}) implementation. On the other hand, on-chip inductors have high parasitic resistance and occupy area of expensive LSI chip. A high-efficiency buck converter using on-chip inductor has been proposed [2]. However, three metal layers from the top are used for the on-chip inductor to reduce its parasitic resistance. It is not reasonable to waste several metal layers for on-chip inductors for the distributed power supplies.

Another candidate in which inductors are implemented is a silicon interposer technology. Its design rule is similar to that of typical pad layouts on silicon VLSI chip. In addition, recently developed $SrTiO_3$ thin film decoupling capacitors in silicon interposer [3] can be used as an output filter of a buck converter. Silicon interposer, therefore, has possibility to add both inductors and capacitors to on-chip distributed buck converters with reasonable parasitic capacitance and resistance. Therefore, we propose a 3D stacked buck converter using a 15µm thick spiral inductor on a newly developed silicon interposer for fine-grain power-supply voltage control in SiP's as shown in Fig. 2.

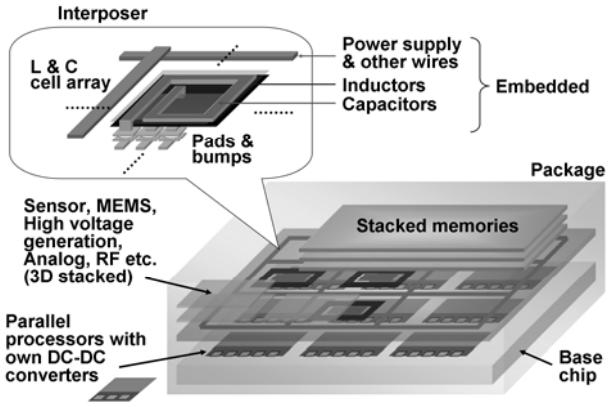

Fig. 1. Distributed power supply for the fine grain V_{DD} in SiP's.

We introduce the structure of the proposed 3D stacked buck converter and details of the silicon interposer with 15µm thick metal layers in Section II. Experimental results are described and discussed In Section III. And finally the conclusions are given in Section IV.

II. Proposed 3D Stacked Buck Converter

A. Structure of the 3D Stacked Buck Converter

Fig. 2 shows the proposed 3D stacked buck converter with a spiral inductor on a silicon interposer. The buck converter consists of a CMOS LSI circuit and a silicon interposer. The CMOS LSI includes active components such as a PWM controller, a CMOS switch, and a driver. Passive components of the buck converter, a spiral inductor and a metal-insulator-metal (MIM) capacitor, are implemented on the silicon interposer. The CMOS LSI circuit and the silicon

interposer are stacked and connected by metal bumps with a small parasitic capacitance and resistance.

In order to improve power efficiency of buck converter, parasitic resistance of a spiral inductor, R_i in Fig. 2 should be reduced. Since the parasitic resistance is inversely proportional to the thickness of the metal layers, 15μm thick metal layers are adopted while conventional silicon interposers typically employ around 5μm metal thickness. The inductance, L_i and parasitic resistance, R_i of a spiral inductor as shown in Fig. 3 can be estimated analytically by following formulas [4]

$$L_i \approx \frac{\mu_0 n^2 d_{avg} c_1}{2}\left[\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right], \quad (1)$$

$$d_{avg} = \frac{d_{out} + d_{in}}{2}, \quad (2)$$

$$\rho \equiv \frac{d_{out} - d_{in}}{d_{out} + d_{in}}, \quad (3)$$

Where C_1=1.27, C_2=2.07, C_3=0.18, C_4=0.13, n is number of turns.

Power loss by inductor, P_{IND} is given by

$$P_{IND} = \frac{V_{IN} D(1-D)}{2fL_i / R_i I_R}\left(I_L^2 + \frac{I_R^2}{3}\right), \quad (4)$$

where V_{IN} is input voltage, D is duty ratio, *f* is switching frequency, I_R is the ripple current, and I_L is the load current [5]. The ratio of L_i / R_i which is determined by the thickness and design rules of metal lyers, and is the most important metrics to discuss inductor performance. Fig. 4 shows the ratio of L_i / R_i dependence of power efficiency of buck converter at D=0.4, V_{OUT}=0.1V, P_{OUT}=0.4W calculated by using equations in [5]. As the ratio of L_i / R_i increases, the power efficiency increase. Therefore it is important that increasing metal thickness (t=15μm) and realizing fine pitch design rule (L/S=20/20μm) at the same time to realize high L_i / R_i ratio.

B. Silicon Interposer with 15μm Thick Metal Layers

To obtain higher inductance performance, our newly developed silicon interposer technology realizes a fine-pitch design rule (Line/Space=20μm/20μm, via hole diameter =30μm) at the metal thickness of15μm as well as conventional interposers with 5μm metal thickness.

Fig. 5 shows the cross-section of the proposed silicon interposer. MIM capacitors ($Ru/SrTiO_3/Ru$ thin film capacitors) [3] are formed on the silicon substrate. The capacitance density is around 12nF/mm^2. 15μm thick metal layers are formed with electroplated copper on the MIM

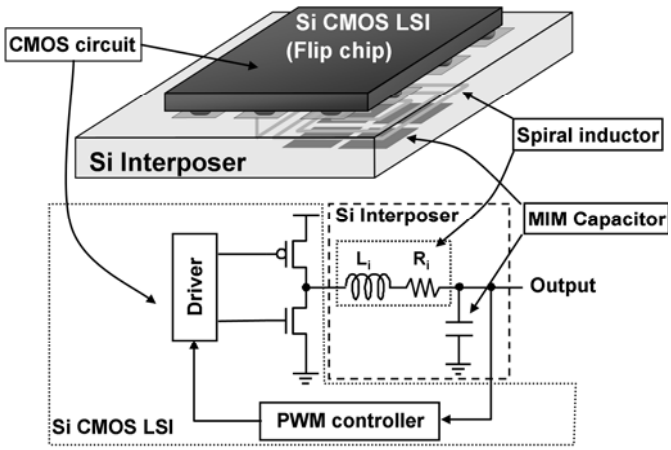

Fig. 2. Proposed 3D stacked buck converter with a spiral inductor on silicon

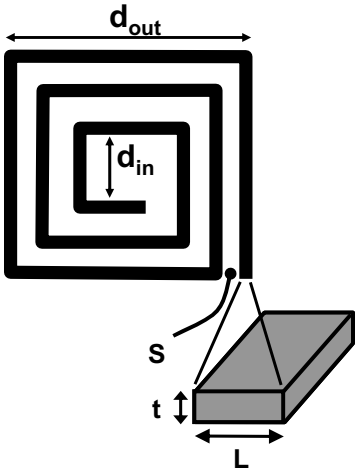

Fig. 3. Planar spiral inductor and formulas to estimate L_i and R_i.

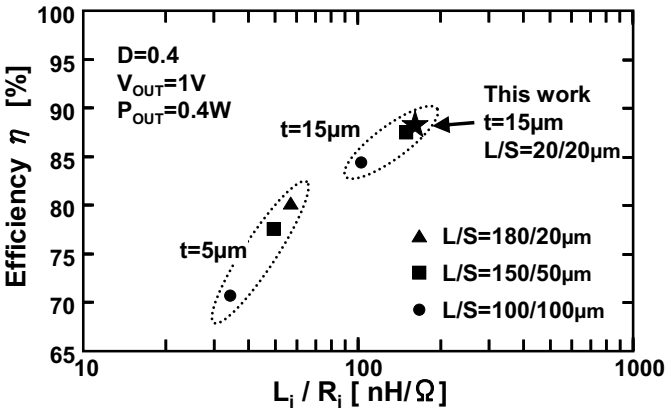

Fig. 4. The ratio of L_i / R_i dependence of power efficiency of buck converter at D=0.4, V_{OUT}=0.1V, P_{OUT}=0.4W.

capacitors. Totally three metal layers including pad metal are available. By increasing metal thickness, photosensitive resin thickness should be thicker. In this work, the thickness between two metal layers is around 20μm The fact makes it difficult to form cavities because of degradation of sensitivity and under exposing at the bottom of the resin as shown in Fig. 6. To solve these problems in photolithography process, a newly developed chemically amplified, positive photosensitive resin is used for the proposed silicon interposer. Fig. 7. shows photograph of the proposed interposer.

III. Measurement Results and Discussion

To demonstrate the effectiveness of the 15μm thick spiral inductor, a test CMOS LSI chip and interposers are fabricated. Fig. 8 shows photographs of the CMOS LSI chip and the silicon interposer. A CMOS switch, which is a main component of the buck converter, is implemented in a 0.18-μm CMOS process. For the comparison of the performance degradation by the parasitic resistance of the spiral inductor, R_i, we fabricated both 5 and 15μm metal thickness interposers. We designed a 2000 × 2000-μm^2, 6-turn, square spiral inductor. The calculated inductance and RS are 80nH and 0.6Ω with 15μm thickness, respectively. The MIM capacitor is implemented underneath the spiral inductor. The measured Buck converter circuit is also shown in Fig.2. 36-MHz, non-overlap clocks are applied to the switch and V_{OUT} is monitored by an active current source, I_{OUT}. V_{IN} and V_{OUT} are 1.8V and 1.0V, respectively.

Fig. 9 shows measured power efficiency vs. I_{OUT} of the buck converters. The peak power efficiency of the 15μm thick inductor achieves 77% at I_{OUT} of 70mA, while that of the 5μm thick inductor is only 66% at I_{OUT} of 60mA. As the increase of I_{OUT}, the difference of the efficiency tends to increase because the power consumption by R_i is dominant. As the result, the newly developed 15μm thick inductor improves the power efficiency by 12% at I_{OUT} of 100mA compared with that of the conventional 5μm thick inductor.

IV. Conclusions

A 3D stacked buck converter with a 15μm thick spiral inductor on a silicon Interposer has been proposed. Our newly developed silicon interposer technology realizes a fine-pitch design rule at the metal thickness of 15μm as well as conventional interposers with 5μm metal thickness. The measurement result shows that the 15μm thick inductor improves the power efficiency of the buck converter by 12% at the output current of 100mA compared with that by the conventional 5μm thick inductor. The buck converter realizes fine-grain power-supply voltage control in SiP's.

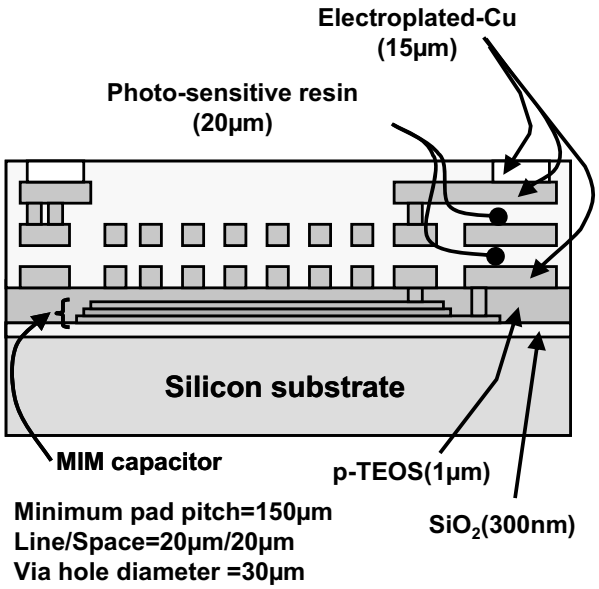

Fig. 5. Cross-section of the proposed silicon interposer with 15-μm thick metal layers.

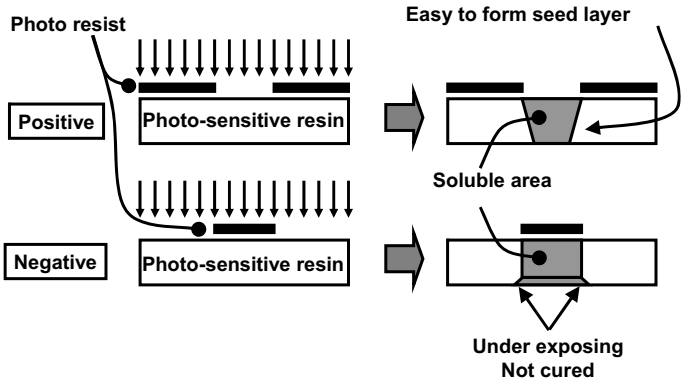

Fig. 6. Photolithography process issue with 20μm thick photo-sensitive resin.

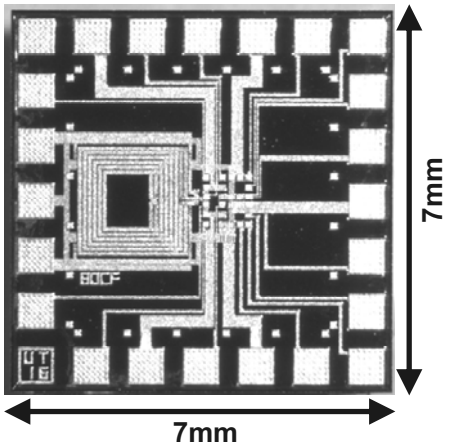

Fig. 7. Photograph of the proposed silicon interposer with 15-μm thick metal layers.

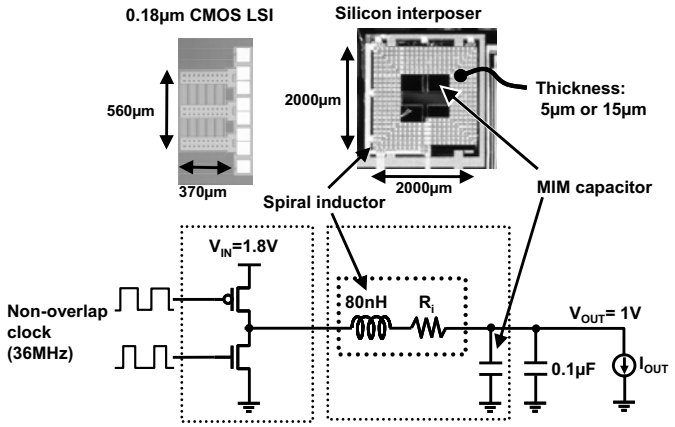

Fig. 8. Photographs of the CMOS LSI chip and the silicon interposer and measurement circuit.

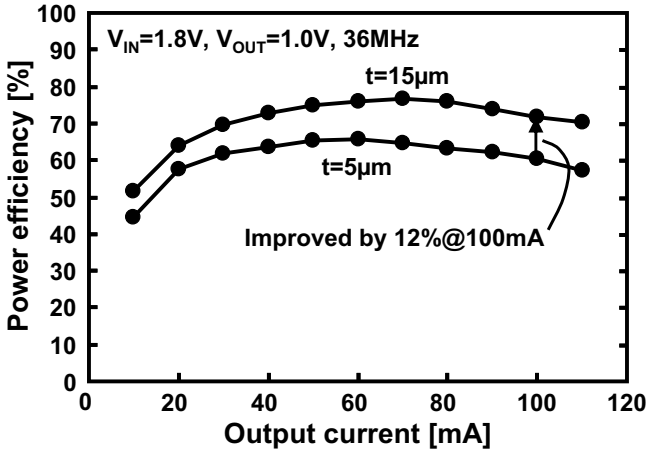

Fig. 9. Measured power efficiency vs. I_{OUT} of the buck converters.

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