Large Area Electronics with Organic Transistors and Novel Interconnects: EMI Measurement Sheet with Stretchable Interconnects and User Customizable Logic Paper (UCLP) with Ink-Jet Printed Interconnects

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ABSTRACT

Large area electronics, which takes advantage of the flexibility and the low cost per area, is a good application of the organic FETs. In this paper, some examples of large area electronics using organic transistors including an EMI measurement sheet and a User Customizable Logic Paper (UCLP) are shown.

1. INTRODUCTION

Organic electronics is attracting a lot of attention for large-area pervasive electronics applications, because organic transistors can be fabricated with printing technologies on arbitrary substrates, enabling both high-throughput and low-cost production. In this paper, some examples of large area electronics using organic transistors including an EMI measurement sheet and a User Customizable Logic Paper (UCLP) are shown.

2. LARGE AREA ELECTRONICS WITH ORGANIC TRANSISTORS

Large area electronics, which takes advantage of the flexibility and the low cost per area, is a good application of the organic FETs (OFET's). Fig. 1 shows the relation between conventional IT applications based on silicon VLSI and human interface applications using large area electronics. The IT applications such as computers and communications are supported by the conventional silicon VLSI's, because silicon MOSFETs are fast and the cost per transistor (=cost per function) is low. In contrast, human interface applications such as ambient intelligence can well be supported by large area electronics with OFET's, because OFET's are flexible and the cost per area is low. Thus silicon VLSI and OFET's are not competing technologies but more complement each other. By combining silicon VLSI's and OFET's, large area electronics has the potential to expand both the application field and the market size of electronic industry. Therefore, the development of the large area electronics which sophisticatedly combines silicon VLSI's and OFET's is very important.

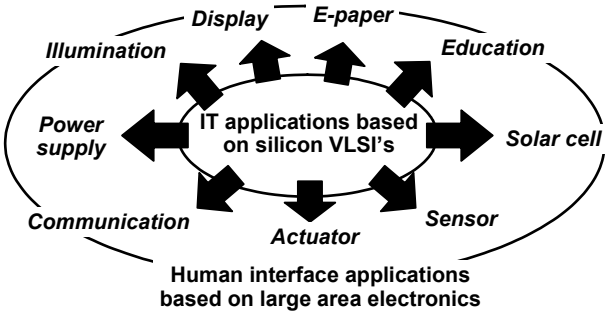

Fig. 1. Relation between conventional IT applications based on silicon VLSI and human interface applications using large area electronics.

3. EMI MEASUREMENT SHEET WITH STRETCHABLE INTERCONNECTS

3.1 EMI Measurement Sheet

Fig. 2 shows an example of an intrasystem EMC issue in a mobile phone. EMI largely depends on the circuit board layout. Localizing either an EMI source or a critical wiring is difficult by simulation. EMI measurement is, therefore, important for the development of electronic systems. However, there is no method of measuring EMI on the surface of 3D structures. In a conventional method, a pencil-like magnetic field probe with X-Y scanning equipment and spectrum analyzers are used for the EMI measurement [1]. In the method, the surface of the electronic device should be scanned repeatedly with the probe. However, the scanning equipment can only move in a flat plane. In another conventional

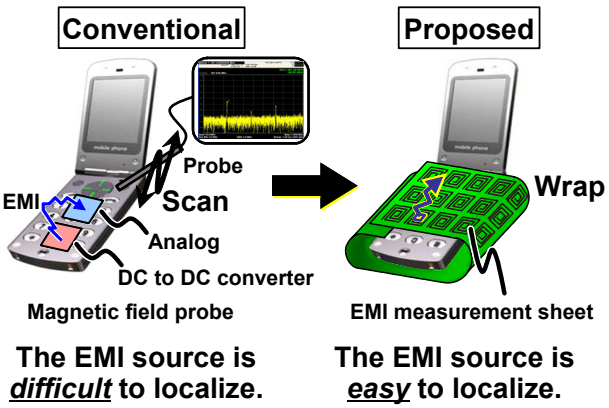

Fig. 2. Intrasystem EMC issue in a mobile phone.

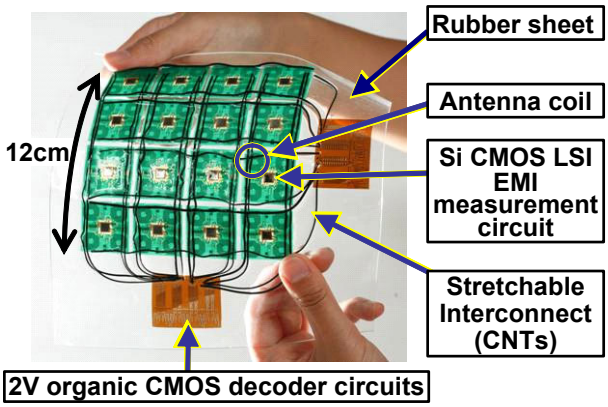

Fig. 3. Stretchable EMI measurement sheet.

method, a measurement system with an integrated array of magnetic field loop antennas is used [2]. Although the method captures the distribution of a magnetic field, it is not applicable to 3D structures since the antenna array is implemented on a flat and rigid printed circuit board.

To solve this problem, an EMI measurement sheet [3-5] was proposed, which enables the measurement of EMI distribution on the surface of 3D structures by wrapping the devices with a sheet like "furoshiki ". Once EMI noise is roughly localized with the measurement sheet, one can easily scan EMI noise using the probe method for precise localization or better quantification of the EM field. The sheet can measure not only a magnetic field but also an electric field suitably changing its antenna connection [5].

Fig. 3 shows a prototype of the stretchable EMI measurement sheet. Each printed circuit board (PCB) includes 2×2 antenna coils and a silicon EMI measurement LSI. The sheet consists of 4×4 PCB's, and therefore, 8×8 antennas are located in 12×12cm^2 area. The antennas and LSI's are controlled using 2V organic CMOS decoder and selector. Each module is electrically connected with a stretchable interconnect made of carbon nanotubes (CNT's). The overall system is sealed with a rubber sheet made of silicone elastomer. The sheet is, therefore, flexible and stretchable. The sheet detects the total power of an electric field in the band up to 700MHz and that of a magnetic field up to 1GHz. The minimum

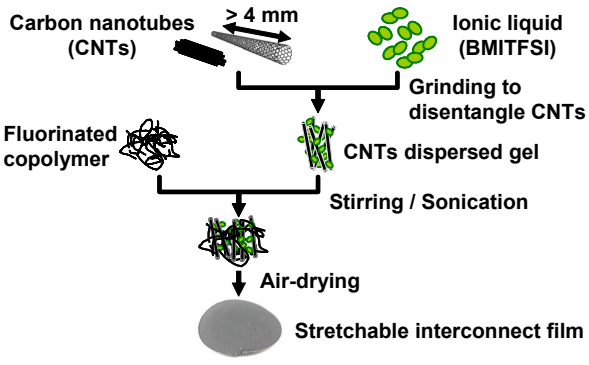

Fig. 4. Process flow of the stretchable interconnects.

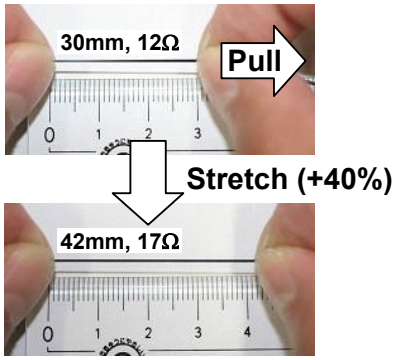

Fig. 5. Demonstration of stretchable interconnect.

detectable power of the electric and magnetic fields are -60 and -70dBm, respectively.

3.2 Stretchable Interconnects with CNT's

The conductive material for the stretchable interconnects is CNT's. CNT's are an inherently stretchable material with a very low resistivity of 0.02 μΩcm [6], however, CNT's should be disentangled prior to being combined with a rubberlike material. The process flow of the stretchable interconnects is shown in Fig. 4. Single-walled CNT's are used as a conductive material. An ionic liquid (1-butyl-3-methyl imidazoliumbis (trifluoromethanesulfonyl) imide, BMITFSI [6]) and CNT's are combined and ground to disentangle the CNT's. A rubberlike material, fluorinated copolymer, and CNT dispersed in gel are combined and stirred by sonication. The stretchable interconnects film is formed by air-drying. Fig. 5 demonstrates its stretchability. The flexible interconnects can be stretched by 40% thanks to the sliding CNT's embedded in the rubberlike material, fluorinated copolymer.

4. UCLP WITH INK-JET PRINTED INTERCONNECTS

4.1 User Customizable Logic Paper (UCLP)

UCLP is proposed for both prototyping of larger-area electronics and educational applications [7]. In particular, as shown in Fig. 6, learners can study and experience the operation of integrated circuits by fabricating custom integrated circuits, using at-home ink-jet printers to print conducting interconnects on paper that contains prefabricated arrays of organic transistors. The feasibility of UCLP is demonstrated with the newly proposed Sea-of Transmission-Gates (SOTG) of organic CMOS transistors, providing field customizability through the use of the printable electronics technology. UCLP is applicable to a wide range of products of printable electronics including flexible displays and electronic paper, as well as for educational purposes. This technology provides a new means to add programmability for integrated circuits used in large-area electronics.

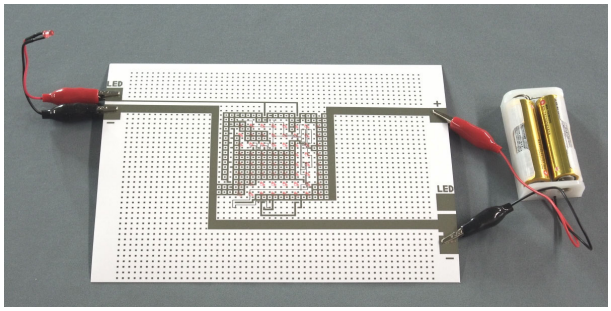

Fig. 6. User Customizable Logic Paper (UCLP) for educational purpose. Learners can study and experience operation of integrated circuits by fabricating custom integrated circuits, using at-home ink-jet printers to print conducting interconnects on paper that contains prefabricated arrays of organic transistors.

Fig. 7 shows a prototype of UCLP [7]. In UCLP, paper that contains an array of vias and an organic SOTG film are stacked. Although it would be ideal to fabricate the whole UCLP including the organic transistors using ink-jet printers, this proves to be very difficult since both high temperature (130-150ºC) and an organic solvent are required to fabricate the organic transistors. Since high temperatures and organic solvents cannot be handled by ink-jet printers, in UCLP the organic transistors are prefabricated and the field customizability is provided by the printed interconnects.

Fig. 8 shows the cross section of UCLP. The 2-V organic CMOS transistors [8] are fabricated on polyimide film. Organic semiconductors for nMOS and pMOS are F16CuPc and pentacene, respectively [8]. Self-assembled mono-layers (SAM) realize 2-V organic transistors, which are covered with a protective layer of parylene. Connection pads to the paper are formed with gold on top of this protective layer. The interconnects are ink-jet printed onto the paper by users.

4.2 Ink-Jet Printed Interconnects

A number of ink-jet printed interconnects technologies

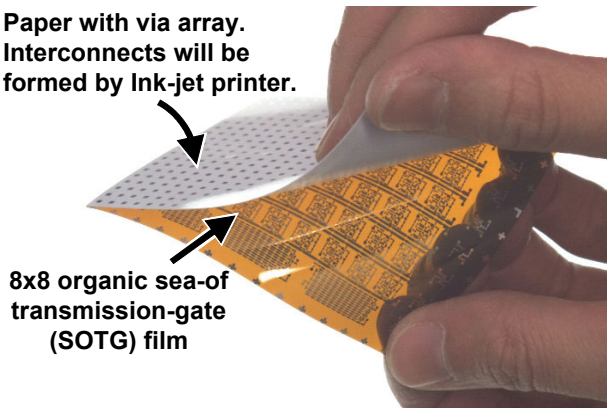

Fig. 7. Prototype of UCLP.

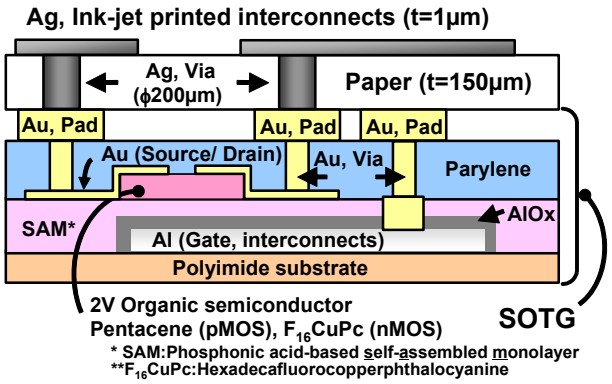

Fig. 8. Cross section of UCLP.

have been developed to date. However, either a high temperature (130-150ºC) sintering or chemical process with organic solvent is required after the printing process, which causes damage to organic transistors. In contrast, our proposed ink-jet printing technology does not require such processes. The technology consists of pre-coated nanoconductive base and silver nanoparticle ink. The diameter of silver nanoparticles in the ink is typically 20nm. The ink chemically reacts with the pre-coated nanoconductive base on the paper at room temperature, that is, a sintering-free process, and does not cause damage to organic transistors.

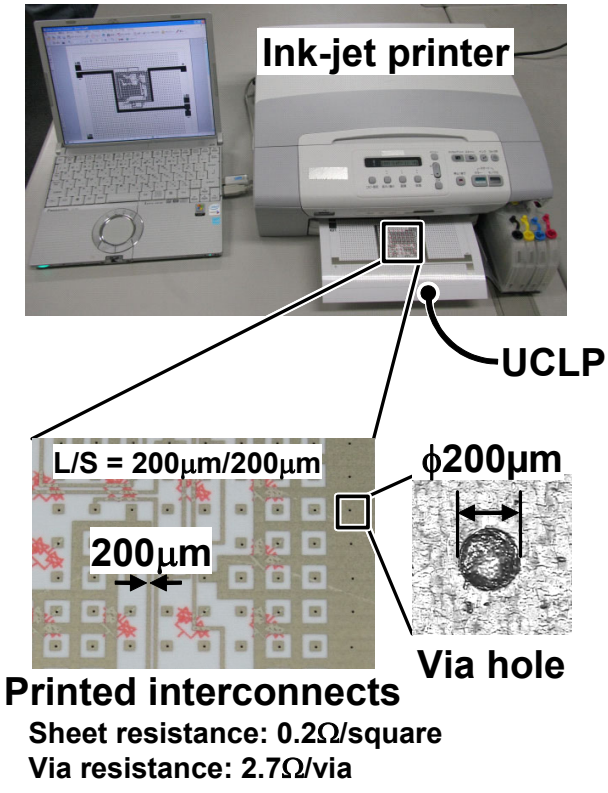

Fig. 9. Photograph of the printing process of the interconnects on UCLP using ink-jet printer, printed interconnects, and a via hole.

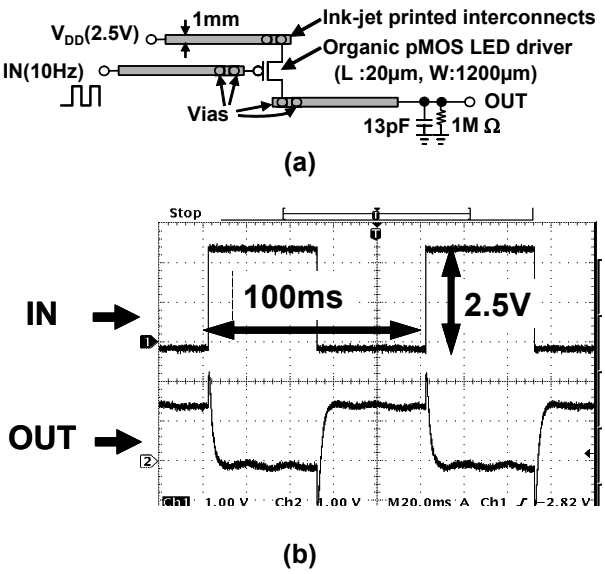

Fig. 10. Measured waveform of organic transistor through printed interconnects. (a) Measurement set-up. (b) Input and output waveforms.

Fig. 9 shows a photograph of the printing process of the interconnects on UCLP using an off-the-shelf ink-jet (piezo-jet) printer and photographs of printed interconnects and a via hole. The thickness of the Ag interconnect is 1μm (typ.) and the measured sheet resistance is 0.2Ω/square (typ.). The via holes of 200μm in diameter are prefabricated in UCLP by punching, in order to form a connection to the SOTG. The measured via resistance is 2.7Ω/via.

In order to evaluate signal attenuation due to the printed interconnects on the paper, the open drain pMOS LED driver with three printed interconnects shown in Fig. 10(a) is measured at 2.5-V power supply voltage (V_{DD}). Fig. 10(b) shows the output waveform from the proposed printed interconnects on the paper. Although the output swing is slightly degraded due to the printed interconnects, it is acceptable because the driver can the driver can still provide capability to drive low-power LED's and logic gates of the SOTG.

5. CONCLUSION

Some examples of large area electronics using organic transistors including the EMI measurement sheet with the stretchable interconnects and UCLP with the ink-jet printed interconnects are shown. By combining silicon VLSI's and OFET's, large area electronics has the potential to expand both the application field and the market size of electronic industry.

ACKNOWLEDGMENT

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