PAPER Special Section on Circuits and Design Techniques for Advanced Large Scale Integration

Inductor and TSV Design of 20-V Boost Converter for Low Power 3D Solid State Drive with NAND Flash Memories

Tadashi YASUFUKU[†a)], **Koichi ISHIDA**[†], *Members*, **Shinji MIYAMOTO**[††], **Hiroto NAKAI**[††], *Nonmembers*, **Makoto TAKAMIYA**[†], **Takayasu SAKURAI**[†], *and* **Ken TAKEUCHI**[†], *Members*

SUMMARY Two essential technologies for a 3D Solid State Drive (3D-SSD) with a boost converter are presented in this paper. The first topic is the spiral inductor design which determines the performance of the boost converter, and the second is the effect of TSV's on the boost converter. These techniques are very important in achieving a 3D-SSD with a boost converter. In the design of the inductor, the on-board inductor from 250 nH to 320 nH is the best design feature that meets all requirements, including high output voltage above 20 V, fast rise time, low energy consumption, and area smaller than 25 mm^2. The use of a boost converter with the proposed inductor leads to a reduction of the energy consumption during the write operation of the proposed 1.8-V 3D-SSD by 68% compared with the conventional 3.3-V 3D-SSD with the charge pump. The feasibility of 3D-SSD's with Through Silicon Vias (TSV's) connections is also discussed. In order to maintain the advantages of the boost converter over the charge pump, the reduction of the parasitic resistance of TSV's is very important.

key words: *SSD, boost converter, charge pump, inductor design, TSV's*

1. Introduction

One of the serious design issues of Solid State Drive (SSD) is the increasing power consumption. Figure 1 shows the device architecture of a conventional SSD. A typical SSD consists of more than 16 NAND flash memories, DRAM's and a NAND controller. In SSD, each NAND flash chip has a charge pump circuit to generate the program voltage of 20 V. Figure 2 shows a schematic and issues concerning the charge pump that generates the program voltage (V_{OUT}). The charge pump prevents area reduction, V_{DD} scaling, and fast write operation of the NAND flash memory [1]. For example, 5 to 10% of the area of each NAND flash chip is occupied by the charge pump owing to its large capacitance, which raises the cost of SSD. Figure 3 shows the energy consumption of NAND flash memories during a write operation at V_{DD} of 3.3 V [2] and 1.8 V (simulated). When V_{DD} is decreased from 3.3 V to 1.8 V, even though the energy of the memory core decreases, the total energy decreases by only 18%, because the energy of the charge pump increases. Therefore, an alternative high-voltage generation circuit is strongly required to reduce the area, the power, and the write time of the NAND flash memory.

Figure 4 shows the 3D-integrated SSD proposed in [3]. The NAND flash memories, DRAM's, the NAND controller, and a boost converter are integrated in SiP. Through silicon vias (TSV's) are assumed to provide the connection between the boost converter and each NAND chip. Figure 5 shows a schematic diagram of the boost converter, which consists of two high-voltage nMOS transistors and an in-

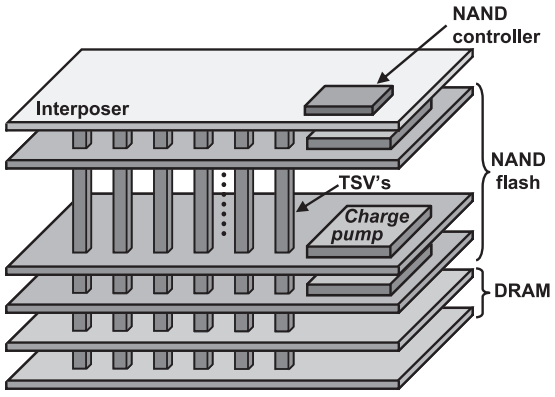


Fig. 1 Conventional SSD with charge pump.

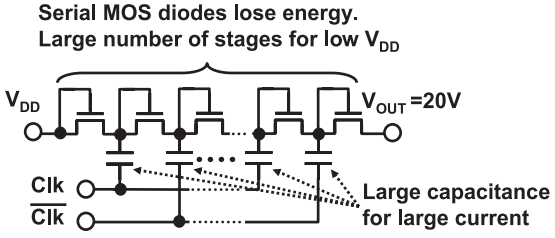


Fig. 2 Schematic and issues of the charge pump.

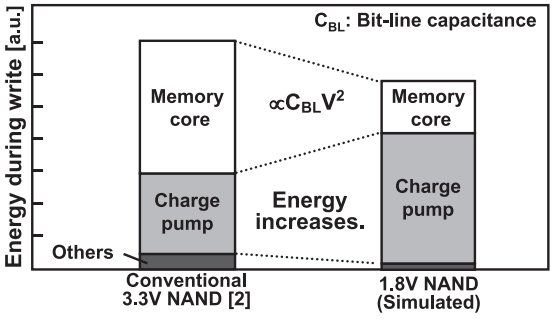


Fig. 3 Energy consumption of NAND flash memories during write operation at V_{DD} of 3.3 V and 1.8 V.

Manuscript received July 10, 2009.
Manuscript revised October 2, 2009.

[†]The authors are with The University of Tokyo, Tokyo, 153-8505 Japan.
[††]The authors are with Toshiba Corporation, Yokohama-shi, 247-8610 Japan.
a) E-mail: tdsh@iis.u-tokyo.ac.jp

DOI: 10.1587/transele.E93.C.317

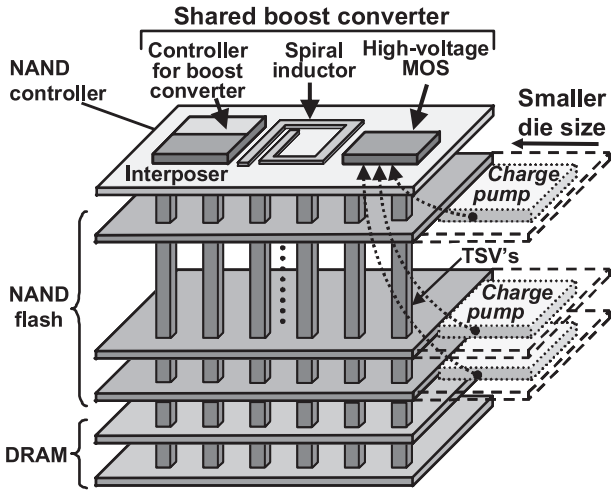


Fig. 4 Proposed 3D-SSD with boost converter.

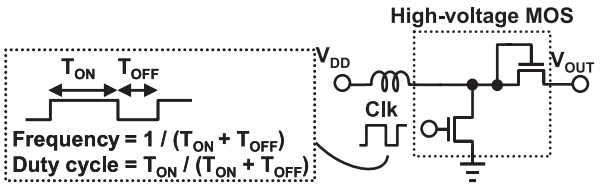


Fig. 5 Circuit diagram of boost converter.

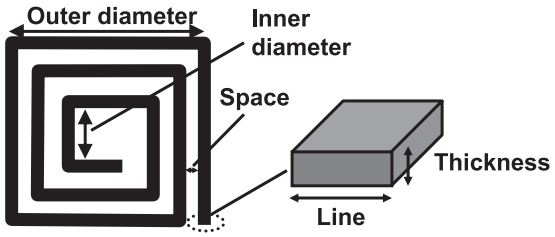


Fig. 6 Design parameters of inductor.

ductor. In the proposed 3D SSD, both low power and fast write-operation are achieved, because both the voltage conversion efficiency and the output current drivability of the boost converter are higher than those of the charge pump. The die area of the NAND flash memory is also reduced, because the charge pumps on each flash memory are merged into the boost converter on an interposer.

In the proposed 3D-SSD, the design of the inductor and TSV's is very important, because it greatly affects the performance of the boost converter, such as the output voltage of the boost converter, the rise time from an initial voltage to a target voltage (V_{OUT}), and the energy consumption during the boost. Therefore, the inductor design of the boost converter and the effect of TSV's on the boost converter are discussed [4], [5].

In Sect. 2, the spiral inductor design, based on SPICE circuit simulation, for the boost converter is presented. In this section, three types of inductors are compared, an on-chip inductor (L), an on-interposer inductor, and an on-board inductor, and the feasibility and design of those inductors are discussed. Section 3 concerns the measurement result of the fabricated boost converter with the spiral inductor optimized in Sect. 2. The boost converter with the designed inductor has a large advantage over the conventional charge pump. In Sect. 4, the effect of TSV's on the boost converter is presented. The parasitic resistance of TSV's degrades the performance of the boost converter. Cu TSV's and doped poly-Si TSV's are compared. A conclusion is drawn in Sect. 5.

2. Spiral Inductor Design for Boost Converter

In this section, the spiral inductor design of the boost converter for the 3D-SSD is investigated. The spiral inductor design is not clear and has yet not been published, because the output load of the boost converter of the NAND flash memory is different from that of a widely used boost converter. Normally, the boost converter has a output resistive and operates in the continuous conduction mode. In contrast, the output load of the boost converter of the NAND flash memory is capacitive, and the boost converter operates in a discontinuous conduction mode. Hence, a spiral inductor design of the boost converter for the 3D-SSD with the NAND flash memories, using SPICE circuit simulation, is proposed.

Table 1 Parameters of three types of inductors.

	Line / Space	Thickness	Metal material
On-chip inductor	10μm / 10μm	2μm	Al
On-interposer inductor	25μm / 25μm	15μm	Cu
On-board inductor	100μm / 100μm	35μm	Cu

In order to implement the inductor in the 3D-SSD, three types of inductors, an on-chip inductor (L), an on-interposer inductor, and an on-board inductor, are compared. Figure 6 shows design parameters of the inductor. A square inductor is assumed. Table 1 shows the parameters of the three types of inductors used. An inductor, the line and space, and thickness of which are shown in this table, is defined as on-board, on-interposer, and on-chip inductor respectively. The parameter values given are typical for each type of inductor. The inductance of the inductors is calculated using Eqs. (1)–(4) [6].

$$L \approx \frac{\mu_0 n^2 d_{avg} c_1}{2}\left[\ln\left(\frac{c_2}{\rho}\right) + c_3\rho + c_4\rho^2\right] \tag{1}$$

$$d_{avg} = \frac{d_{out} + d_{in}}{2} \tag{2}$$

$$\rho \equiv \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{3}$$

$$c_1 = 1.27,\ c_2 = 2.07,\ c_3 = 0.18,\ c_4 = 0.13 \tag{4}$$

L represents the inductance, μ_0 the vacuum permeability, n the number of turns, d_{out} the outer diameter, d_{in} shows the inner diameter, and $c_1 - c_4$ are constants. $d_{\text{in}}/d_{\text{out}} = 1/3$ is assumed in this study to increase the quality factor of the

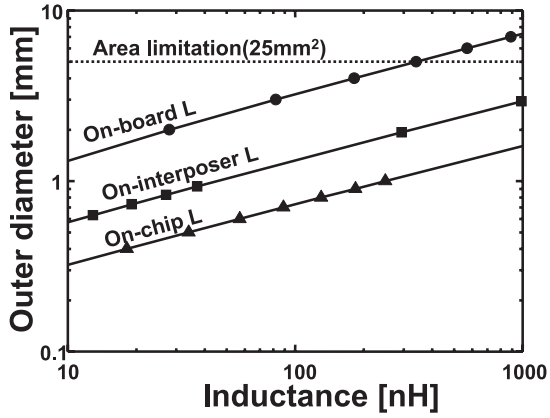


Fig. 7 Calculated inductance dependence of outer diameter of three types of inductors.

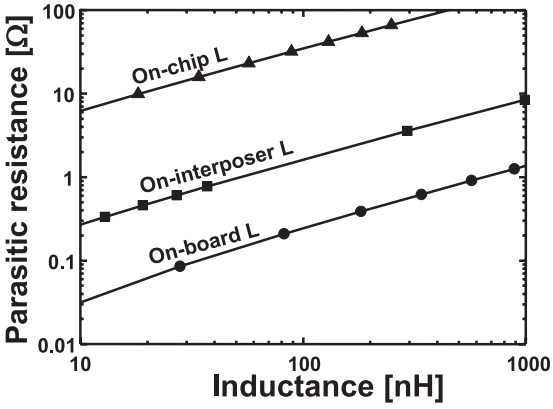


Fig. 8 Calculated inductance dependence of parasitic resistance of three types of inductors.

inductor. As the first step in the inductor design, the range of inductance is calculated with an area constraint.

Figure 7 shows the calculated inductance dependence of the outer diameter of the three types of inductors. The area limitation of 25 mm^2 for the inductor is assumed, because the die area of a typical flash memory is 150~200 mm^2 and 15% of that area can be used for the inductor. Figure 8 shows the inductance dependence of the parasitic resistance of the three types of inductors calculated from the total inductor length. The on-chip inductor has a small area and high parasitic resistance, because the line and space is narrow and the metal thickness is thin. In contrast, the on-board inductor has a large area and low parasitic resistance, because the line and space is wide and the metal thickness is thick. In the on-board inductor, 330 nH is the maximum inductance with the 25 mm^2-area constraint.

The various inductors shown in Figs. 7 and 8 are adopted in the boost converter and the best design of the inductor is investigated. Figure 9 shows the equivalent circuit of the simulated boost converter. The input voltage (V_{DD}) is 1.8 V and target output voltage (V_{OUT}) is 20 V. A NAND flash chip, as the output load of the boost converter, is emulated by the load resistance (1 MΩ) and capacitance

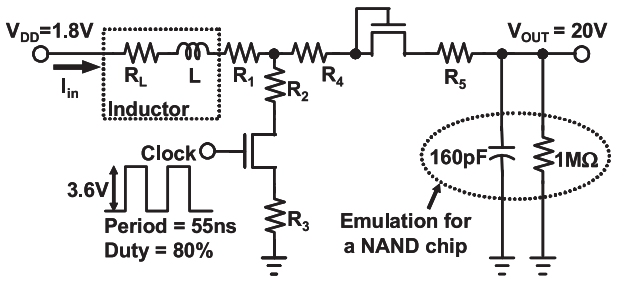


Fig. 9 Equivalent circuit of simulated boost converter described in Sect. 3.

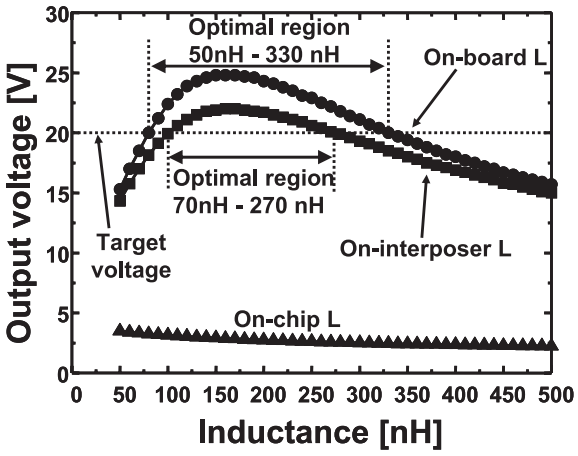


Fig. 10 Simulated dependence of output voltage on inductance in three types of inductors.

(160 pF). The parasitic resistance of the interconnects (R_1-R_5) and the inductor (R_L) is also included. The switching frequency (or period) and duty cycle are 18.2 MHz (55ns) and 80%, respectively, and the amplitude of the switching transistor is 3.6 V. Inductance dependence of key features of the boost converter, including the output voltage, the rise time, and the energy consumption, are simulated with the equivalent circuit.

Figure 10 shows the simulated dependence of the output voltage on the inductance in the three types of inductors. The boost converter with the on-chip inductor cannot boost the voltage above 4 V, because the parasitic resistance of the on-chip inductor is very high. In contrast, both the on-interposer and the on-board inductors can boost the voltage to above 20 V. In order to boost the output voltage to above 20 V, a 50 nH to 330 nH on-board inductor and a 70 nH to 270 nH on-interposer inductor are needed. Too high or too low an inductance cannot be used, because of the tradeoff between the inductance and the parasitic resistance. When the inductance is too low, the inductor cannot store enough energy to boost the voltage. When the inductance is too high, on the other hand, the inductor again cannot store enough energy because of the high parasitic resistance.

Figure 11 shows the simulated dependence of the rise time (t_{rise}) on the inductance in the two types of inductors. Figure 12 shows the simulated waveforms of the boost con-

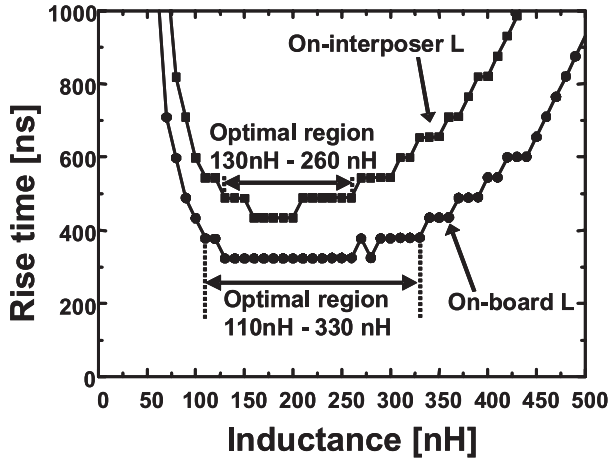


Fig. 11 Simulated dependence of rise time on inductance in two types of inductors.

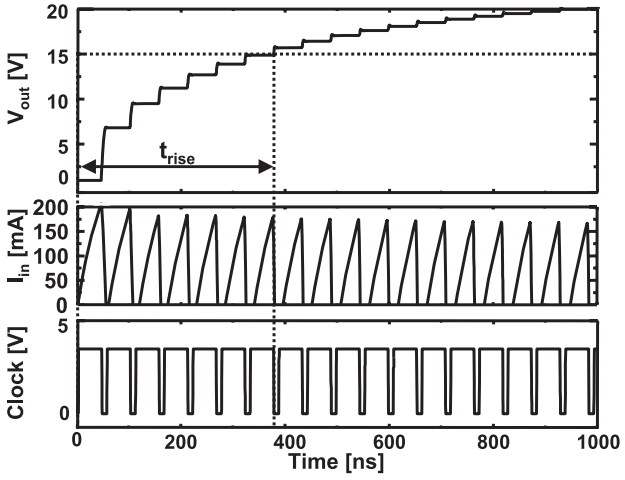


Fig. 12 Simulated waveforms of boost converter.

verter. $t_{\rm rise}$ is defined as the time needed to boost $V_{\rm out}$ from 0 V to 15 V, as shown in Fig. 12. The graph in Fig. 11 is not smooth, because $V_{\rm out}$ of 15 V is achieved by several pulses, as shown in Fig. 12. To realize short $t_{\rm rise}$, the range of inductance is limited from 130 nH to 260 nH for the on-interposer inductor, and 110 nH to 330 nH for the on-board inductor. The reason for the optimum inductance region is similar to the previous discussion.

Figure 13 shows the simulated inductance dependence of energy consumption ($E_{\rm loss}$) during boosting in the two types of inductors. $E_{\rm loss}$ is calculated from Eq. (5) using $V_{\rm DD}$, the input current ($I_{\rm in}$), and $t_{\rm rise}$ shown in Fig. 9.

$$E_{loss} = \int_0^{t_{rise}} V_{DD} \cdot I_{in} dt \tag{5}$$

When the on-interposer inductor is used, $E_{\rm loss}$ is minimum at around 400 nH. This optimal range, however, does not match the range shown in Figs. 10 and 11. In contrast, the inductance range from 250 nH to 320 nH is optimal with the on-board inductor. This is the best design choice for meeting all the requirements, including high output voltage,

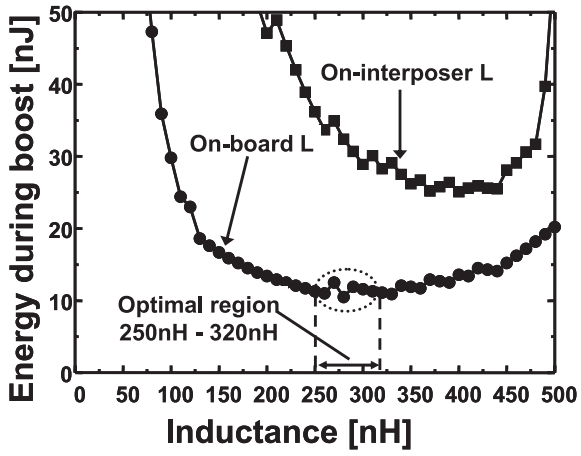


Fig. 13 Simulated inductance dependence of energy consumption during boosting in two types of inductors.

fast rise time, low energy consumption, and area limitation of 25 mm^2, because this range is also within the optimal region, as shown in Figs. 10 and 11. If a thicker metal is available in the on-interposer inductor, the boost converter with the on-interposer inductor will also achieve a similar performance to that with the on-board inductor. This is not impossible because only typical parameters are used in the calculation in this work.

3. Measurement of Boost Converter

To demonstrate the performance of the boost converter with the optimized inductor described in Sect. 2, the boost converter with a 270 nH on-board inductor, as shown Table 1, is fabricated and measured. Figure 14 shows the micrographs of the on-board spiral inductor and the fabricated boost converter LSI where the high voltage MOSFET's are integrated. The area of the inductor is 5 mm by 5 mm, and the area of the boost converter LSI is 0.35 mm by 0.50 mm. The measured parasitic resistance of the inductor is 1.05 Ω.

Table 2 summarizes the measured key features of the boost converter and the conventional charge pump for a typical NAND flash memory. The measured energy consumption for boosting to 15 V is 30 nJ and the rise time is 0.92 ns, which are 12% and 27% of those in the case of the charge pump. The area of the high voltage MOSFET's is 0.175 mm^2 which is 15% of that in the case of the charge pump. Figure 15 shows the energy consumption during the write operation for between the conventional 3D-SSD with the charge pump and the proposed 3D-SSD with the boost converter. When $V_{\rm DD}$ of the NAND decreases from 3.3 V to 1.8 V, the total energy consumed during writing of the NAND flash memory decreases by 68% compared with the conventional 3.3 V NAND, because the energy consumption of the high-voltage generator decreases by 88% compared with the charge pump. In the charge pump, the number of stages will increase when $V_{\rm DD}$ is lowered to 1.8 V, and therefore, energy loss by MOS diodes increases. In contrast, since the boost converter achieves the 20 V program

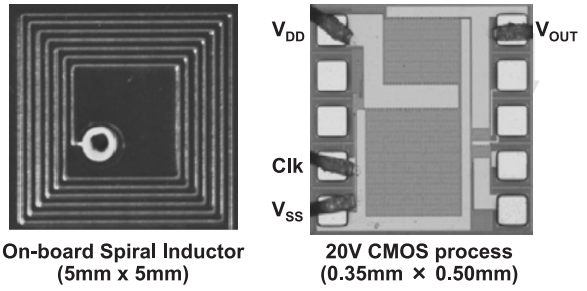


Fig. 14 Micrographs of on-board spiral inductor and fabricated boost converter LSI where high-voltage MOSFET's are integrated.

Table 2 Summary of key features of proposed boost converter and conventional charge pump.

	Proposed boost converter (Measured)	Conventional charge pump (Simulated)
Supply voltage	1.8V	←
Chip area	0.175mm² (15%)	1.19mm² (100%)
Rising time (0➔15V)	0.92μs (27%)	3.45μs (100%)
Energy during boost (0➔15V)	30nJ (12%)	253nJ (100%)

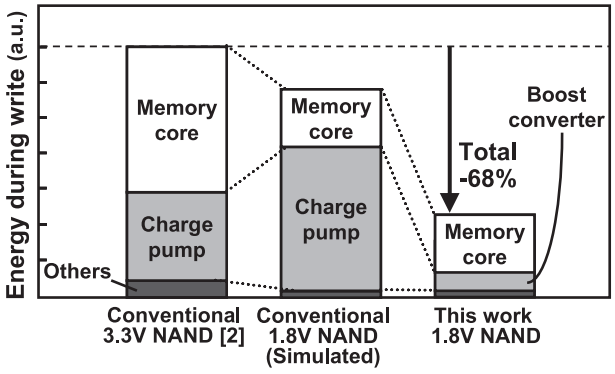


Fig. 15 Energy during write operation for conventional 3D-SSD with charge pump and proposed 3D-SSD with boost converter.

voltage with a single-stage circuit, the energy loss does not increase. In this way, the proposed spiral inductor design of the boost converter contributes to the low power and the fast write operation of the 3D-SSD.

4. Effect of TSV's on Performance of Boost Converter

The advantage of the boost converter over the charge pump was shown by the results of measurements in previous section. The feasibility of the 3D SSD with TSV connections, however, is not clear, because the measurement does not take into account the parasitic RLC's accompanying TSV's. In reality, when 3D-SSD's are implemented using TSV's, the parasitic RLC's may degrade the performance of the boost converter. The parasitic L and C of the TSV's can be neglected, because the parasitic L and C are under 0.03% and 1% [7] of the inductance of the inductor and the output load capacitance, respectively, in the boost converter. In

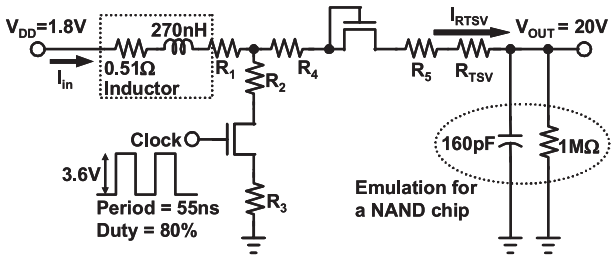


Fig. 16 Equivalent circuit of simulated boost converter described in Sect. 4.

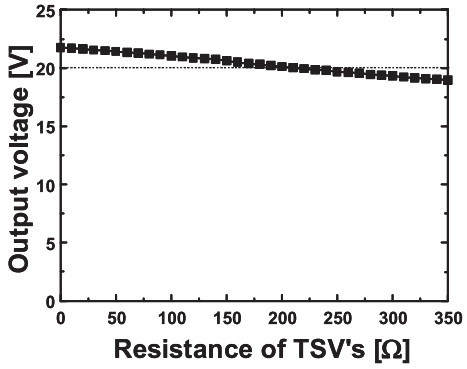


Fig. 17 Simulated dependence of output voltage of boost converter on resistance of TSV's.

contrast, the parasitic resistance of TSV's cannot be disregarded. Therefore, in this section, the impact of the parasitic resistance of TSV's on the performance of the boost converter (output voltage, rise time, energy consumption) is simulated.

Figure 16 shows the equivalent circuit of the simulated boost converter. The parasitic resistance of TSV's (R_{TSV}) is serially connected directly after R_5. The 270 nH inductor is used on the basis of the result presented in Sect. 3. The parasitic resistance of the inductor is 0.51 Ω. Other conditions such as clock frequency, duty cycle and input voltage are the same as those described in chapter 3. The resistance of a word-line is neglected in this work, which is the most pessimistic assumption in evaluating the effect of TSV resistance on the rise time. In an actual SSD, the word-line resistance increases the rise time of the program voltage and the TSV resistance has much less of an effect than in the simulation shown in Fig. 16.

R_{TSV} is governed by the TSV material and the number of stacked NAND chips. For example, the resistance of Cu TSV's with the diameter of 2 μm and the height of 5 μm is ~200 mΩ/via [8], while the resistance of the doped poly-Si TSV with the diameter of 28~46 μm and the height of 50 μm is 1.3~5.0 Ω/via [9]. In a 64-chip stacked SSD where a boost converter is connected to all the chips using only one TSV, the total resistance of the TSV's become 320 Ω (polysilicon TSV) and 12.8 Ω (copper TSV) so the simulated results are shown up to 350 Ω.

Figure 17 shows the simulated R_{TSV} dependence of the output voltage of the boost converter. Figure 18 shows the

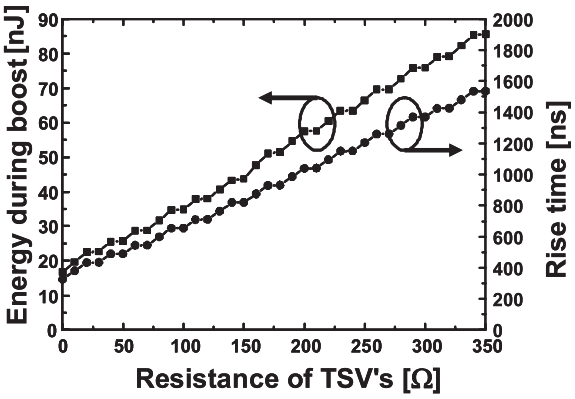


Fig. 18 Simulated dependence of energy consumption during boosting and rising time on resistance of TSV's.

simulated R_{TSV} dependence of the energy consumption during boosting and the rise time of the boost converter. In Fig. 17, it can be seen that the impact of R_{TSV} is small for the output voltage of the boost converter. In contrast, Fig. 18 shows that R_{TSV} has a large effect on both the rise time and the energy consumption. Compared with the ideal case where R_{TSV} is 0 Ω, both the rise time and the energy consumption are twice and 5 times larger when R_{TSV} is 90 Ω and 330 Ω, respectively. For example, in the aforementioned 64-chip stacked above SSD system, copper TSV's (total resistance of 12.8 Ω) are acceptable, though the polysilicon TSV's (total resistance of 320 Ω) are not acceptable. Therefore, in order to maintain the advantages of the boost converter over the charge pump in terms of rise time and energy consumption, as shown in Sect. 3, the reduction of R_{TSV} is very important.

5. Conclusion

Two essential technologies for 3D-SSD with a boost converter, that is, the spiral inductor design and the effect of TSV's on the boost converter were discussed in this paper. These technologies are very important in achieving 3D-SSD with a boost converter. In the inductor design, the on-board inductor from 250 nH to 320 nH was the best design feature that meets all requirements, including a high output voltage above 20 V, fast rise time, low energy consumption, and area smaller than 25 mm^2. The use of the boost converter with the proposed inductor led to the reduction of the energy consumption during the write operation of the proposed 1.8-V 3D-SSD by 68% compared with the conventional 3.3-V 3D-SSD with the charge pump. Although the on-board inductor was the best in this study when typical thickness and line width were adopted for the inductor, the on-interposer inductor can be used if a thicker metal is available, and in fact, it is necessary for realizing the 3D-SSD.

The effect of the parasitic resistance of TSV's on the performance of the boost converter was also simulated. In the 64-chip stacked SSD system, the copper TSV's (total resistance of 12.8 Ω) were acceptable, but the polysilicon TSV's (total resistance of 320 Ω) were not acceptable. Therefore, in order to maintain the advantages of the boost converter over the charge pump in terms of rise time and energy consumption, the reduction of the parasitic resistance of TSV's is very important.

Acknowledgments

The authors appreciate S. Ohshima, T. Hara, Y. Watanabe, T. Futatsuyama and G. Iwasaki and the Toshiba NAND team for their support and for chip fabrication.

References

[1] K. Takeuchi, "Novel co-design of NAND flash memory and NAND flash controller circuits for sub-30 nm low-power high-speed solid-state drives (SSD)," IEEE Symposium on VLSI Circuits Dig. Tech. Papers, pp.124–125, 2008.

[2] K. Takeuchi, Y. Kameda, S. Fujimura, H. Otake, K. Hosono, H. Shiga, Y. Watanabe, T. Futatsuyama, Y. Shindo, M. Kojima, M. Iwai, M. Shirakawa, M. Ichige, K. Hatakeyama, S. Tanaka, T. Kamei, J.Y. Fu, A. Cernea, Y. Li, M. Higashitani, G. Hemink, S. Sato, K. Oowada, S.C. Lee, N. Hayashida, J. Wan, J. Lutze, S. Tsao, M. Mofidi, K. Sakurai, N. Tokiwa, H. Waki, Y. Nozawa, K. Kanazawa, and S. Ohshima, "A 56 nm CMOS 99 mm^2 8 Gb multi-level NAND flash memory with 10 MB/s program throughput," IEEE International Solid-State Circuits Conference, pp.144–145, 2006.

[3] K. Ishida, T. Yasufuku, S. Miyamoto, H. Nakai, M. Takamiya, T. Sakurai, and K. Takeuchi, "A 1.8 V 30 nJ adaptive program-voltage (20 V) generator for 3D-integrated NAND flash SSD," IEEE International Solid-State Circuits Conference, pp.238–239, Feb. 2009.

[4] T. Yasufuku, K. Ishida, S. Miyamoto, H. Nakai, M. Takamiya, T. Sakurai, and K. Takeuchi, "Inductor design of 20-V boost converter for low power 3D solid state drive with NAND flash memories," International Symposium on Low Power Electronics and Design, pp.87–91, Aug. 2009.

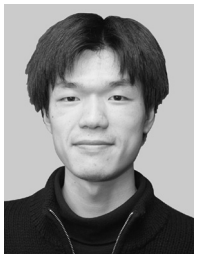
[5] T. Yasufuku, K. Ishida, S. Miyamoto, H. Nakai, M. Takamiya, T. Sakurai, and K. Takeuchi, "Effect of resistance of TSV's on performance of boost converter for low power 3D SSD with NAND flash memories," IEEE International Conference on 3D System Integration, Sept. 2009.

[6] S. Mohan, M. Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," IEEE J. Solid-Sate Circuits, vol.34, no.10, pp.1419–1424, Oct. 1999.

[7] D.M. Jang, C. Ryul, K.Y. Lee, B.H. Cho, J. Kiml, T.S. Oh, W.J. Lee, and J. Yu, "Development and evaluation of 3-D SiP with vertically interconnected through silicon vias (TSV)," Electronic Components and Technology Conference, pp.847–852, May 2007.

[8] P. Leduc, L. Di Cioccio, B. Charlet, M. Rousseau, M. Assous, D. Bouchu, A. Roule, M. Zussy, P. Gueguen, A. Roman, O. Rozeau, M. Heitzmann, J. Nieto, L. Vandroux, P. Haumesser, R. Quenouillere, A. Toffoli, P. Sixt, S. Maitrejean, L. Clavelier, and N. Sillon, "Enabling technologies for 3D chip stacking," International Symposium on VLSI Technology, Systems and Applications, pp.76–78, April 2008.

[9] M. Kawano, N. Takahashi, Y. Kurita, K. Soejima, M. Komuro, and S. Matsui, "Three-dimensional packaging technology for stacked DRAM with 3-Gb/s data transfer," IEEE Trans. Electron Devices, vol.55, no.7, pp.1614–1620, July 2008.



Tadashi Yasufuku received the B.S. degree in applied physics from Keio University, Japan in 2007, and the M.S. degree in electronic engineering from the University of Tokyo, Japan in 2009. He is currently working toward a Ph.D. degree. His research interests include sub/near threshold logic circuit design and switched converters.

Koichi Ishida received the B.S. degree in electronics engineering from the University of Electro-Communications, Tokyo, Japan, in 1998, and received the M.S. and Ph.D. degrees in electronics engineering from the University of Tokyo, Tokyo, Japan, in 2002 and 2005, respectively. He is currently working at Institute of Industrial Science, the University of Tokyo as a research associate. His research interests include low-voltage low-power CMOS analog circuit and RF wireless-communication circuit.

Shinji Miyamoto received the B.E. degree in electrical engineering from Kyusyu Sangyo University, Fukuoka, Japan, in 1987. In 1987, he joined TOSHIBA Corporation, Kanagawa, Japan. He has been engaged in the development and design of memories. He is now manager of Design Methodology & Infrastructure, Yokohama, Japan.

Hiroto Nakai received the B.S. degree in material engineering from Tohoku University, Japan, in 1982, the M.S. degree in material engineering from Tohoku University, in 1984. He was working in the nonvolatile memory area from 1984 to 2002 in Toshiba. His work specializes in NAND flash design from 1991 to 2002.

Makoto Takamiya received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Japan, in 1995, 1997, and 2000, respectively. In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high speed digital LSIs. In 2005, he joined University of Tokyo, Japan, where he is an associate professor of VLSI Design and Education Center. His research interests include the circuit design of the low-power RF circuits, the ultra low-voltage digital circuits, and the large area electronics with organic transistors. He is a member of the technical program committee for IEEE Symposium on VLSI Circuits and IEEE Custom Integrated Circuits Conference (CICC).

Takayasu Sakurai received the Ph.D. degree in EE from the University of Tokyo in 1981. In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC Solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 through 1990, he was a visiting researcher at the University of California Berkeley, where he conducted research in the field of VLSI CAD. From 1996, he has been a professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic IC's and large-area electronics. He has published more than 400 technical publications including 100 invited presentations and several books and filed more than 200 patents. He served as a conference chair for the Symp. on VLSI Circuits, and ICICDT, a vice chair for ASPDAC, a TPC chair for the first A-SSCC, and VLSI symp. and a program committee member for ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He is a recipient of 2005 IEEE ICICDT award, 2004 IEEE ISSCC Takuo Sugano award and 2005 P&I patent of the year award and four product awards. He gave keynote speech at more than 50 conferences including ISSCC, ESSCIRC and ISLPED. He is consulting to startup and international companies. He was an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS distinguished lecturer. He is a STARC Fellow and an IEEE Fellow.

Ken Takeuchi is currently an Associate Professor at the Department of Electrical Engineering and Information Systems, Graduate School of Engineering of the University of Tokyo. He is now working on the VLSI circuit design especially on the emerging non-volatile memories, 3D-integrated SSDs and ultra-low power 3D-circuits for Green-IT. He received the B.S. and M.S. degrees in Applied Physics and the Ph.D. degree in Electric Engineering from the University of Tokyo in 1991, 1993 and 2006, respectively. In 2003, he also received the M.B.A. degree from Stanford University. Since he joined Toshiba in 1993, he had been leading Toshiba's NAND flash memory circuit design for fourteen years. He designed six world's highest density NAND flash memory products such as 0.7 μm 16 Mbit, 0.4 μm 64 Mbit, 0.25 μm 256 Mbit, 0.16 μm 1 Gbit, 0.13 μm 2 Gbit and 56 nm 8 Gbit NAND flash memories. He holds 150 patents worldwide including 88 U.S. patents. Especially, with his invention, "multipage cell architecture," presented at Symposium on VLSI Circuits in 1997, he successfully commercialized world's first multi-level cell NAND flash memory in 2001. He has authored numerous technical papers, one of which won the Takuo Sugano Award for Outstanding Paper at ISSCC in 2007. He has served on the ISSCC memory sub-committee since 2007. He served as a tutorial speaker at ISSCC in 2008 and as a memory forum organizer at ISSCC in 2009.