PAPER Special Section on Circuits and Design Techniques for Advanced Large Scale Integration

Difficulty of Power Supply Voltage Scaling in Large Scale Subthreshold Logic Circuits

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SUMMARY In order to explore the feasibility of large-scale subthreshold logic circuits and to clarify the lower limit of supply voltage (V_{DD}) for logic circuits, the dependence of the minimum operating voltage ($V_{DD\min}$) of CMOS logic gates on the number of stages, gate types and gate width is systematically measured with 90 nm CMOS ring oscillators (RO's). The measured average $V_{DD\min}$ of inverter RO's increased from 90 mV to 343 mV when the number of RO stages increased from 11 to 1 Mega, which indicates the difficulty of V_{DD} scaling in large-scale subthreshold logic circuits. The dependence of $V_{DD\min}$ on the number of stages is calculated using the subthreshold current model with random threshold voltage (V_{TH}) variations and compared with the measured results, and the tendency of the measurement is confirmed. The effect of adaptive body bias control to compensate purely random V_{TH} variation is also investigated. Such compensation would require impractical inverter-by-inverter adaptive body bias control.

key words: *minimum operating voltage, subthreshold, logic, variations, body bias*

1. Introduction

Very low-voltage operation of VLSI's is effective in reducing both dynamic and leakage power and the maximum energy efficiency is achieved at low V_{DD} (e.g., 320 mV [1]). Thus, many works have been carried out on the subthreshold operation of logic circuits [1]–[5] and SRAM's [6], where V_{DD} is less than V_{TH} of transistors. However, the number of transistors in the previously reported subthreshold circuits is small (e.g. 70 k transistor logic circuits at V_{DD} of 230 mV [1], a 32 kbit SRAM at V_{DD} of 160 mV [6], and a 1000-stage inverter chain at V_{DD} of 60 mV [4]), and the possibility of mega-gate-scale subthreshold circuits is not clear.

$V_{DD\min}$ is the minimum power supply voltage when the circuits operate without functional errors. RO's are useful $V_{DD\min}$ detectors [7], because RO's stop oscillation when the first functional error in the logic circuits arises. Figure 1 shows the simulated waveform of the 5-stage CMOS inverter RO. V_{DD} is varied from 0.2 V to 0 V. At $V_{DD\min}$ of 50 mV, RO stops oscillating. In order to emulate the recent SoC's, mega-stage-scale RO's are required, because the recent SoC's have 10–100 Mega logic gates. With technology scaling and an increased number of transistors on a chip,

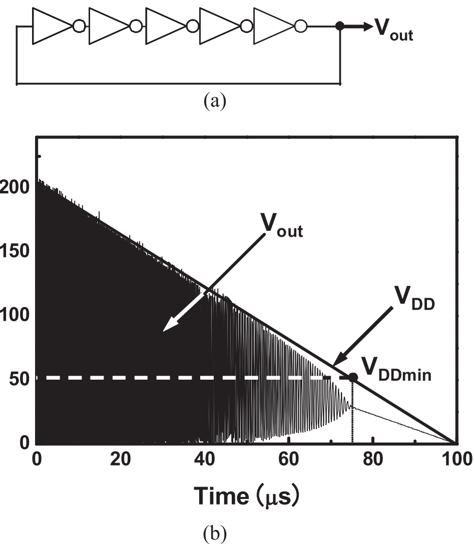

Fig. 1 Simulated waveform of 5-stage CMOS inverter RO. Definition of $V_{DD\min}$ is shown.

$V_{DD\min}$ will increase, because the more gates there are, the more likely it is that the worst-case condition will occur, and thus a higher V_{DD} will be required. However, the systematic measurements of $V_{DD\min}$ of the subthreshold logic circuits made with scaled devices have not yet been reported.

Systematically measured dependence of $V_{DD\min}$ of CMOS logic gates on the number of stages, gate types and gate widths with 90 nm CMOS RO's are reported for the first time, in order to explore the feasibility of large-scale-subthreshold logic circuits and to clarify the lower limit of V_{DD} for logic circuits [7], [8].

In Sect. 2, the design of CMOS RO's for $V_{DD\min}$ measurement and the measured $V_{DD\min}$ is presented. Section 3 presents the analysis of the origin of $V_{DD\min}$ with SPICE and MATLAB to explain the measured results. Section 4 presents the fine-grain adaptive body bias control to reduce $V_{DD\min}$.

2. Measured $V_{DD\min}$ of 90 nm CMOS RO's

2.1 Design of CMOS RO's for $V_{DD\min}$ Measurement

Figure 2 shows a schematic of the proposed RO circuits to enable $V_{DD\min}$ measurement. The output of RO should be amplified, because the output amplitude of the RO is small

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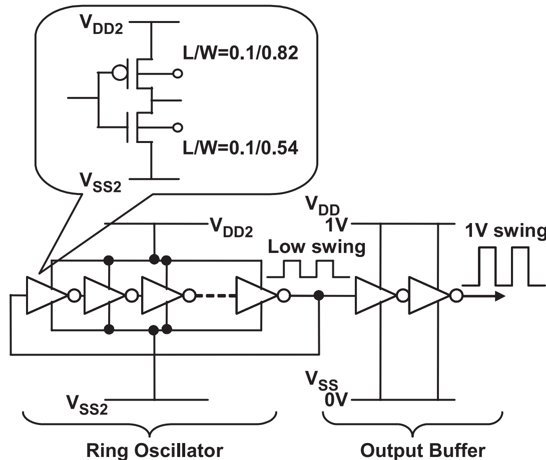

Fig. 2 Schematic of proposed CMOS ring oscillators (RO's) for the $V_{DD\,\mathrm{min}}$ measurement.

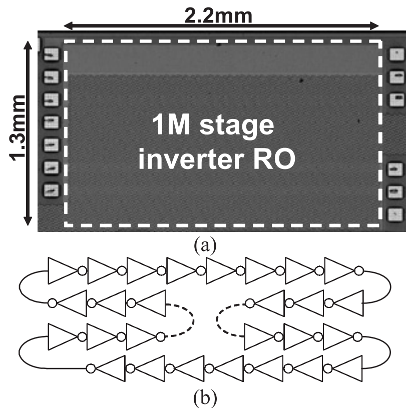

Fig. 3 (a) Micrograph of 1M-stage inverter RO. (b) Layout style of RO's.

(e.g., 70 mV) in the $V_{DD\,\mathrm{min}}$ measurement. The amplification is performed by the output buffer where V_{DD} and V_{SS} of the output buffer are separated from V_{DD2} and V_{SS2} of RO by a triple well process. V_{DD2} and V_{SS2} are tuned manually in 1 mV steps in order to find the lowest V_{DD} (=$V_{DD2} - V_{SS2}$) at which RO can oscillates, which means that the DC level of the output voltage of RO matches the logic threshold of the first stage of the output buffer. The tuning is necessary to achieve a precise measurement of $V_{DD\,\mathrm{min}}$ because the wrong setting of V_{DD2} and V_{SS2} leads to an overestimation of $V_{DD\,\mathrm{min}}$. Figure 3(a) shows the micrograph of a 1 Mega-stage inverter RO in 90 nm CMOS. The core area is 2.2 mm × 1.3 mm. Figure 3(b) shows the layout style of RO's. In order to remove the effect of the within-die systematic transistor variation on RO's, the interconnect length between the inverters is as short as possible and the maximum interconnect length in the 1 Mega-stage inverter RO is 3.5 μm. If the interconnection between inverters is long, both within-die systematic and random transistor variations affect the measurement results and degrade $V_{DD\,\mathrm{min}}$. Therefore, the interconnection is shortened to eliminate the effect of within-die systematic random variation as much as possible.

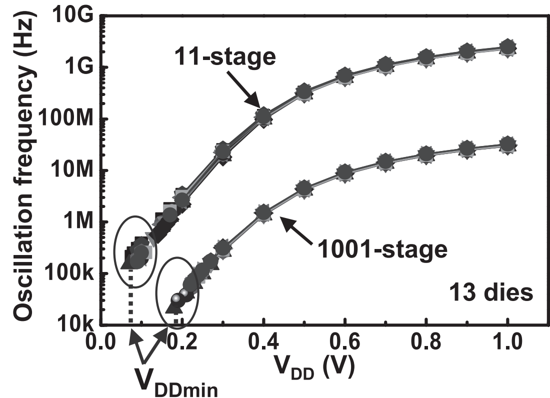

Fig. 4 Measured V_{DD} dependence of oscillation frequency of 11-stage and 1001-stage RO's.

RO's include three different logic gates (inverter, 2NAND and 3NAND) and two inverters with different gate widths. Standard primitive cells are used for the logic gates, and the P/N ratio was not optimized for the minimum V_{DD} operation. The gate length is minimum in the 90 nm CMOS process. The gate widths of nMOS (W_n) and pMOS (W_p) are 0.54 μm and 0.82 μm, respectively. An inverter with this size of transistors is defined as an ×1 inverter, and an inverter with a gate width four times larger than that of the ×1 inverter is defined as an ×4 inverter. RO's were fabricated by the 1 V 90 nm CMOS process in three different lots. The first lot includes inverter RO's from 11 stage to 1 Mega stages that are used to investigate the dependence of $V_{DD\,\mathrm{min}}$ on the number of stages. The second lot includes inverter RO's, 2NAND RO's and 3NAND RO's that are used to investigate the gate-type dependence. The third lot includes inverter RO's and ×4 inverter RO's that are used to investigate the gate-width dependence.

2.2 Dependence of $V_{DD\,\mathrm{min}}$ on Number of Stages

Figure 4 shows the measured V_{DD} dependence of the oscillation frequency of 11-stage and 1001-stage RO's for 13 dies. $V_{DD\,\mathrm{min}}$ is defined as the supply voltage (= $V_{DD2} - V_{SS2}$) when the RO's stop oscillating and no voltage transitions from the output buffer are observed, which corresponds to functional errors in logic LSI's. It should be noted that $V_{DD\,\mathrm{min}}$ of 11-stage RO's is lower than that of 1001-stage RO's.

Figure 5 shows the measured die-to-die distribution of $V_{DD\,\mathrm{min}}$ of inverter RO's with 11 to 1M-stages. Thirty to thirty-six dies are measured. Figure 6 shows the measured dependence of the average $V_{DD\,\mathrm{min}}$ with a $\pm 1\sigma$ error bar of inverter RO's on the number of stages extracted from Fig. 5. As the number of stages is increased, the average $V_{DD\,\mathrm{min}}$ increases, because $V_{DD\,\mathrm{min}}$ is determined by the worst inverter(s) in each RO. For example, the average $V_{DD\,\mathrm{min}}$ increases from 90 mV to 343 mV when the number of RO stages increases from 11 to 1 Mega. The 343 mV indicates

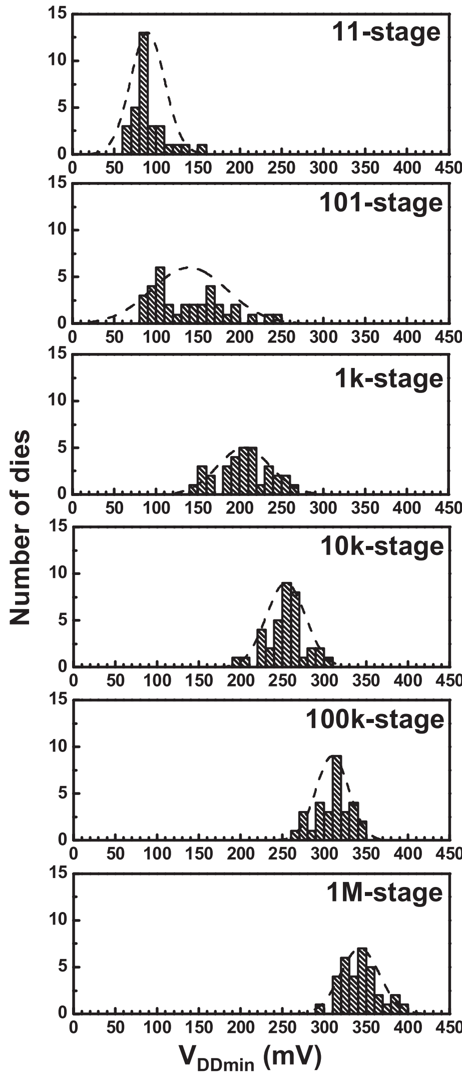

Fig. 5 Die-to-die distribution of $V_{DD\,\min}$ of inverter RO's with 11 to 1M-stage.

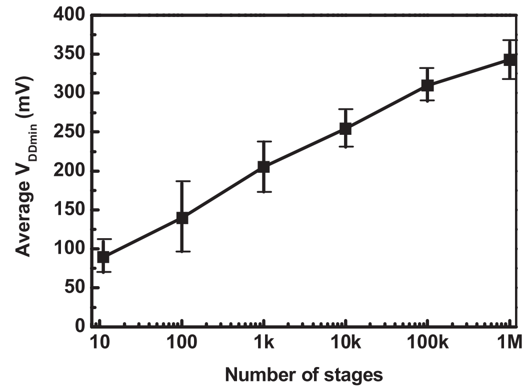

Fig. 6 Measured dependence of average $V_{DD\,\min}$ of inverter RO's on number of stages.

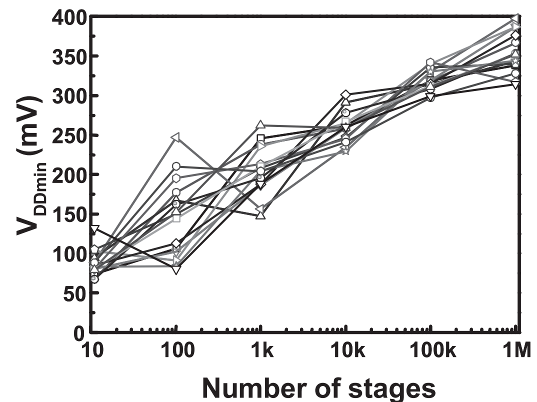

Fig. 7 Measured dependence of $V_{DD\,\min}$ of inverter RO's on number of stages for 15 dies.

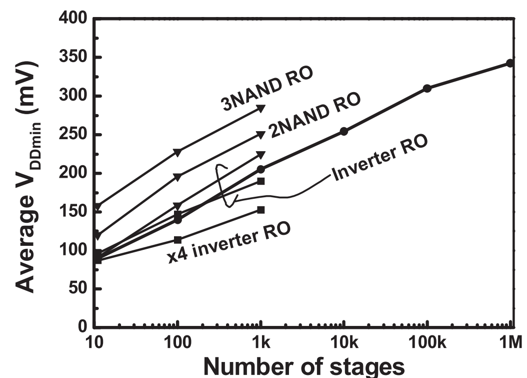

Fig. 8 Measured dependence of average $V_{DD\,\min}$ of all RO lots on number of stages.

a superthreshold V_{TH} operation. The results indicate that $V_{DD\,\min}$ for logic circuits depends on the scale of the circuits, and large-scale logic circuits have high $V_{DD\,\min}$. In order to analyze the die-to-die $V_{DD\,\min}$ variations, Fig. 7 shows the measured dependence of $V_{DD\,\min}$ of inverter RO's on the number of stages for 15 dies. Each line in Fig. 7 represents a measured $V_{DD\,\min}$ of each chip. Each chip contains 6 RO's with 11 to 1M stages. The 6 RO's are isolated from each other, and do not share any part of the circuit. Note that no specific line is higher or lower than the others, and lines are random. Therefore, it can be concluded that there is no systematic chip-to-chip variation such that all 6 types of RO's are all high or low, but rather, the RO's vary randomly.

2.3 Dependence of $V_{DD\,\min}$ on Gate Types and Gate Width

Figure 8 shows the measured dependence of the average $V_{DD\,\min}$ of the inverter, ×4 inverter, 2NAND and 3NAND RO's on the number of stages. In 2NAND, an nMOS transistor connected to V_{SS} is used for signal propagation, and the gate of the other nMOS transistor is tied to V_{DD}. The lowest $V_{DD\,\min}$ was 58 mV for the 11-stage RO's. The three lines corresponding to the inverter RO's show the measured average $V_{DD\,\min}$ in three different lots. While increasing the number of stages and the number of stacked transistors increases $V_{DD\,\min}$, the wide gate width decreases $V_{DD\,\min}$.

The three lines of the inverter, 2NAND and 3NAND

RO's have similar gradients but different offsets. The gradient is determined by the transistor variations, and the offsets are determined by the imbalance between the current drivability of nMOS and that of pMOS. In this work, 3NAND RO's, have the highest average $V_{DD\min}$, because both W_n and W_p are the same for the inverter, 2NAND and 3NAND RO's and the 3NAND RO's have the largest imbalance in current drivability. The imbalance, however, can be solved by tuning the W_p/W_n ratio; this tuning minimizes $V_{DD\min}$ because V_{INV} becomes equal to $V_{DD}/2$ after tuning. The gradients of curves for inverter RO's and ×4 inverter RO's in Fig. 8 are different, because the V_{TH} variations of the ×4 inverter RO's are less than that of the inverter RO's.

3. Analysis of $V_{DD\min}$

3.1 Analysis of $V_{DD\min}$ with SPICE

The origin of $V_{DD\min}$ is analyzed by Monte Carlo SPICE simulations. Figure 9(a) shows the schematic of the simulated 11-stage RO's where each transistor has a random V_{TH}. The inverter chain with the input of V_{DD} is simulated. Figure 9(b) shows the node voltages ($V_1 - V_{11}$) and the inversion voltages (V_{INV}'s) of the inverters. V_{INV} is defined as the voltage when the input and output of each inverter is shorted, which is equivalent to the logic threshold of the inverter. Normally, the logical low of $V_1 - V_{11}$ is lower than V_{INV} and the logical high of $V_1 - V_{11}$ is higher than V_{IN}. The inverter chain, however, has a functional error at the #7 and #8 inverters, because the #7 inverter has slow nMOS and fast pMOS, V_{INV} of the #7 inverter is high, and the logical low of V_7 ($V_{OUT_LOW_7}$) is higher than V_{INV} of the #8 inverter. The functional error stops the RO oscillation.

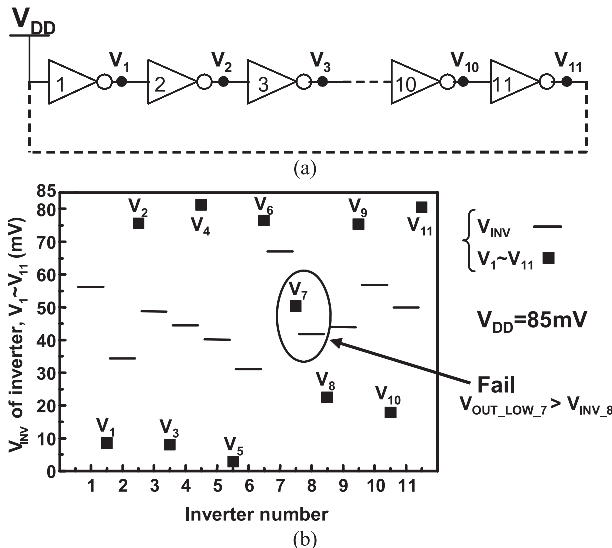

Fig. 9 (a) Simulated 11-stage inverter chain where each transistor has random V_{TH}. (b) Node voltages ($V_1 - V_{11}$) and inversion voltages (V_{INV}'s) of inverters.

3.2 Comparison of Measured and Calculated $V_{DD\min}$

In order to investigate the increasing average $V_{DD\min}$ with the number of stages, the simulations of $V_{DD\min}$ from 11-stage to 1 Mega-stage RO's are required. However, the simulations of $V_{DD\min}$ of up to 1 Mega-stage RO's by Monte Carlo SPICE take too long and are not practical. Therefore, $V_{DD\min}$ is calculated using the subthreshold current model with random V_{TH} variations, and the results are compared with the measured results. Equation (1) shows the drain current model of MOSFET in the subthreshold region.

$$I_D = C_1 e^{C_2(V_{GS}-V_{TH})}(1 - e^{-C_3 V_{DS}}) \tag{1}$$

I_D is the drain current, V_{GS} is the gate-to-source voltage and V_{DS} is the drain-to-source voltage. C_1, C_2 and C_3 are constants. In the CMOS inverter, the input-output characteristic of the inverter is derived by equating I_D of nMOS and pMOS. Figure 10 shows the inverter characteristics determined by SPICE and the calculation with Eq. (1). MATLAB was used for the calculation. V_{DD} was varied from 50 mV to 0.4 V. The calculation is verified by comparison with the result of SPICE. Below V_{DD} of 0.2 V, the calculation error is small. In contrast, above V_{DD} of 0.3 V, the calculation error is large, because the calculation includes only the diffusion current (= subthreshold current) and neglects the drift current (= strong inversion current).

Figure 11 shows the calculation steps for obtaining $V_{DD\min}$ of n-stage RO using Eq. (1), where n is an odd number. The Monte Carlo method is adopted in this calculation. V_{TH} in Eq. (1) is varied by the Monte Carlo method, because the transistors in the RO have random V_{TH} variations. The probability distribution of V_{TH} is assumed to be Gaussian. First, the probability density function (PDF) of the output (V_{n-1}) of the $(n-1)$-stage inverter chain with the input of 0 V is calculated by cascading the $(n-1)$-stage inverters as shown in Fig. 11(b). Although the correct V_{n-1} is low, Fig. 11(b) shows some incorrect high V_{n-1} values due to functional error. Figure 11(c) shows the probability of an error (= logic low) that occurs at V_n. Figure 11(d) shows the probability of V_n error derived by multiplying the value in Fig. 11(b) with that in Fig. 11(c). Finally, Fig. 11(e) shows

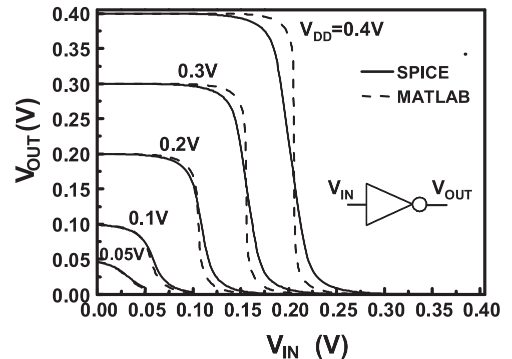

Fig. 10 Inverter characteristics obtained using SPICE and Matlab.

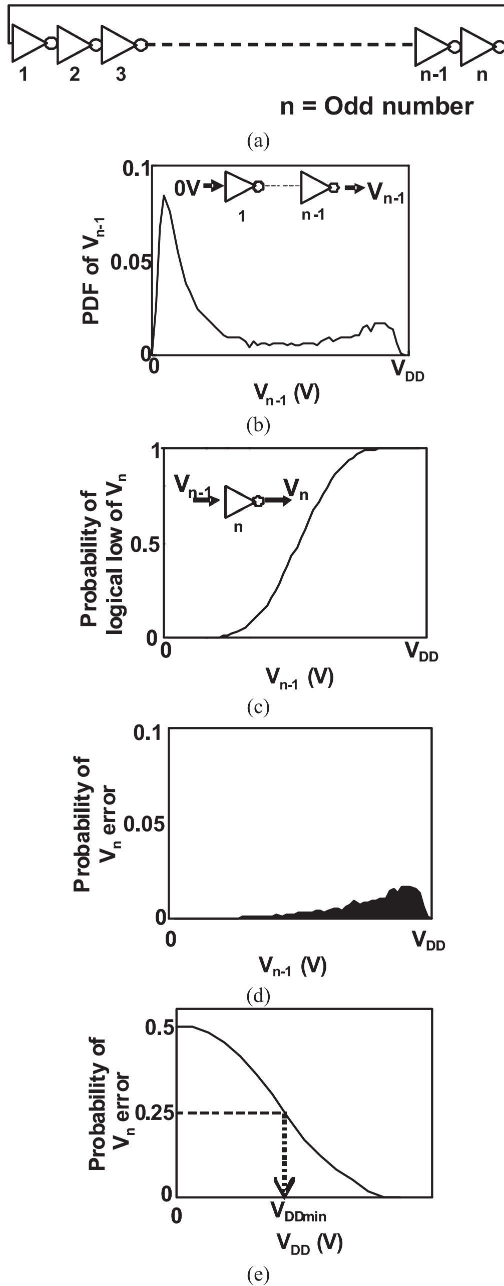

Fig. 11 Calculation steps of $V_{DD\min}$ of n-stage RO. (a) Calculated n-stage inverters. (b) Probability of output of $(n-1)$-stage inverter chain with input of 0 V. (c) Probability of logical low (=error) of V_n. (d) Probability of V_n error dependence on V_{n-1}. (e) Probability of V_n error dependence on V_{DD}.

the probability of V_n error derived by integrating the value in Fig. 11(d). A value obtained from this integration corresponds to a point in Fig. 11(e) at a given V_{DD}. The curve in Fig. 11(e) is obtained by sweeping V_{DD}, and integrating the value in Fig. 11(d), which is drawn at each V_{DD}. Strictly speaking, the probability of V_n error in the n-stage inverter chain with the input of V_{DD} should also be calculated and added to Fig. 11(e). However, the inputs of 0 V or V_{DD} are symmetrical. Therefore, $V_{DD\min}$ is defined as V_{DD} when the

Table 1 Several sets of σV_{TH}'s of nMOS and pMOS used in calculation.

Name	σV_{TH} (mV)		Remarks
	nMOS	pMOS	
Sim075	25.8	22.5	x0.75
Sim100	34.4	30.0	x1
Sim125	43.0	37.5	x1.25
Sim150	51.6	45.0	x1.5

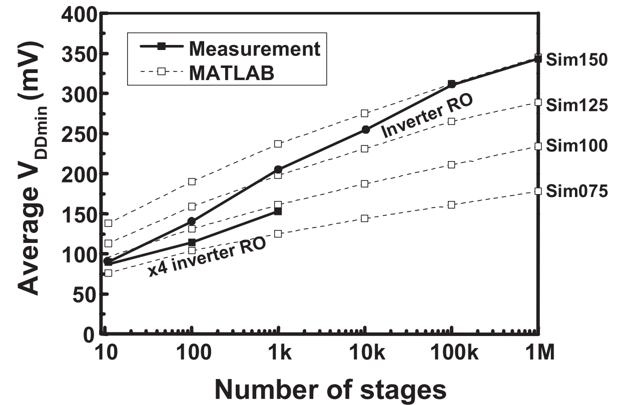

Fig. 12 Measured and calculated dependences of average $V_{DD\min}$ of inverter RO's on the number of stages.

probability of V_n error equals to 25%, as shown in Fig. 11(e).

Table 1 shows the 4 sets of σV_{TH}'s of nMOS and pMOS used in the calculation. σV_{TH}'s are originally determined from the Pelgrom plot, however, σV_{TH}'s are varied as the fitting parameter to fit the calculated result to the measured results. Figure 12 shows the measured and calculated dependences of the average $V_{DD\min}$ of inverter RO's on the number of stages. The measured results for ×4 inverter RO's are also plotted. The calculation shows the expected increasing gradients and offsets with increasing σV_{TH}, which confirm the tendency of the measurement. Two conceivable reasons for the quantitative error between the measurement and MATLAB are (1) only V_{TH} variations are considered in the calculation and no other variations are not considered; (2) The inverter characteristic error increases with increasing V_{DD}, as shown in Fig. 10, because the model includes only the subthreshold current and neglects the strong inversion current.

4. Fine-Grain Adaptive Body Bias Control to Reduce $V_{DD\min}$

An increasing $V_{DD\min}$ as the number of stages increases is not acceptable. Fine-grain adaptive body bias control is effective for compensating for the intra die *systematic* V_{TH} variations [9]. Its effectiveness on the intra die *random* V_{TH} variations, however, is not clear. The required circuit block size for fine-grain control is also unclear. Therefore, $V_{DD\min}$ has been extracted by Monte Carlo SPICE simulations for different grain sizes. Figure 13 shows the initial and compensated $V_{DD\min}$ for the 11-stage RO. The body bias

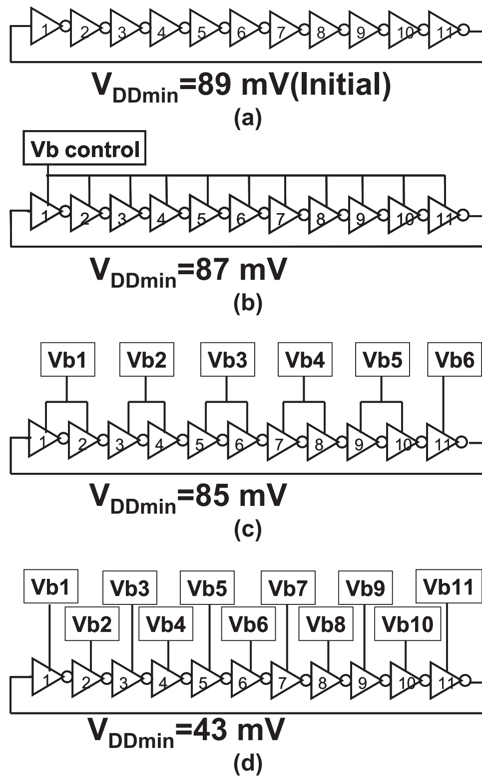

Fig. 13 Initial and compensated $V_{DD\min}$ by various fine-grain adaptive body bias controls for 11-stage RO. (a) No body bias. (b) Common body bias. (c) Body bias for every 2 inverters. (d) Inverter-by-inverter body bias.

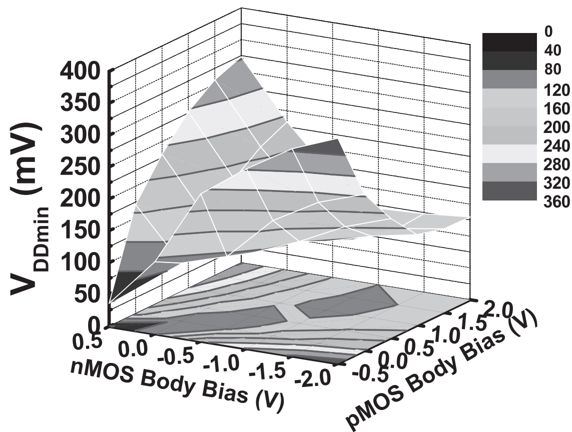

Fig. 14 Measured $V_{DD\min}$ dependence of body bias of both nMOS and pMOS for 11-stage RO.

of pMOS is adaptively controlled to minimize $V_{DD\min}$ and the body bias of nMOS is fixed. When a common body bias is applied to the 11 inverters (Fig. 13(b)), $V_{DD\min}$ is improved from 89 mV to 87 mV, because the current drivability of nMOS and pMOS is balanced and V_{INV} becomes equal to $V_{DD}/2$. The $V_{DD\min}$ reduction by common body bias control is also verified by the measurement results.

Figure 14 shows the measured $V_{DD\min}$ dependence on the body bias of both nMOS and pMOS for an 11-stage RO. When V_{TH} of nMOS and that of pMOS are balanced, $V_{DD\min}$ is low. In contrast, when they are unbalanced, $V_{DD\min}$ is high [3], [4]. The initial $V_{DD\min}$ is 91 mV when both body biases are 0 V. Common body bias control enables the reduction of reducing $V_{DD\min}$ to 87 mV, i.e. by 4 mV only. This is in agreement with the simulation results and shows that coarse-grain body bias control is not effective in significantly reducing $V_{DD\min}$.

When independent body bias is applied for every 2 inverters, $V_{DD\min}$ decreases to 85 mV, as shown in Fig. 13(c). In contrast, when inverter-by-inverter body bias is applied, $V_{DD\min}$ is drastically reduced to 43 mV, as shown in Fig. 13(d). Despite the significant improvement, inverter-by-inverter body bias control is impractical because of the large area penalty. Therefore, when granularity is more than 2 inverters, fine-grain adaptive body bias control is not effective for compensating the intra die *random* V_{TH} variations in ultra low-voltage logic circuits.

5. Conclusions

The minimum operation voltage ($V_{DD\min}$) of 90 nm CMOS logic gates has been investigated using ring oscillators. The measured average $V_{DD\min}$ of inverter RO's increased from 90 mV to 343 mV when the number of RO stages increased from 11 to 1 Mega, which indicates the difficulty of V_{DD} scaling in large-scale subthreshold logic circuits. Whereas increasing the number of stages and the number of stacked transistors increases $V_{DD\min}$, a large gate width decreases $V_{DD\min}$. It should be noted that these results are only one example of the process used in this study, because these measurement results have process dependence.

The dependence of $V_{DD\min}$ on the number of stages was calculated with the subthreshold current model with random threshold voltage variations, and the tendency revealed by the measurement was confirmed. Lowering $V_{DD\min}$ is difficult, because the compensation of purely random V_{TH} variations would require impractical inverter-by-inverter adaptive body bias control.

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