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0.18-V Input Charge Pump with Forward Body Bias to Startup Boost Converter for Energy Harvesting Applications

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SUMMARY In this paper, a 0.18-V input three-stage charge pump circuit applying forward body bias is proposed for energy harvesting applications. In the developed charge pump, all the MOSFETs are forward body biased by using the inter-stage/output voltages. By applying the proposed charge pump as the startup in the boost converter, the kick-up input voltage of the boost converter is reduced to 0.18 V. To verify the circuit characteristics, the conventional zero body bias charge pump and the proposed forward body bias charge pump were fabricated with 65 nm CMOS process. The measured output current of the proposed charge pump under 0.18-V input voltage is increased by 170% comparing to the conventional one at the output voltage of 0.5 V. In addition, the boost converter successfully boosts the 0.18-V input to higher than 0.65-V output.

key words: *charge pumps, switched capacitor, startup, boost converter, low voltage*

1. Introduction

Recently, there has been an increasing demand for portable energy sources harvesting the energy from the surrounding environment. It makes the possibility to self-powering the battery for portable and implantable electronic devices. However, the output voltages provided from energy harvesting sources such as single solar cells and the thermoelectric generators (TEGs) are usually several hundreds of mV and needs to be converted to a higher voltage by using the boost converter. Since the threshold voltage of the standard CMOS technology is higher than the output voltage of energy harvesting source, the startup circuit which startup the boost converter from the low voltage is required.

Several low input voltage boost converters applying startup mechanism have been reported [1]–[6]. 20 mV input boost converter [1] is implemented for thermal electric energy harvesting. However, it requires 0.65-V external voltage to startup the system. Another solution is applying a startup circuit with a mechanical switch [2] to startup the boost converter. However, it requires mechanical vibrations and the application is limited. In [3], the separate charge pump IC [4] is used as the startup circuit. It uses fully depleted Silicon on Insulator (SOI) to enable low-voltage operation. References [5]–[7] integrate the startup circuit and boost converter by using standard CMOS process. However, they do not use voltage booster as the startup circuit and the minimum startup voltage is larger than 0.9 V which is higher than output voltages of energy harvesting sources. Therefore, it is necessary to integrate the low voltage startup circuit with the boost converter by using standard CMOS process to meet the requirements for energy harvesting applications.

The charge pump circuit applying as startup circuit for boost converter can reduce the startup voltage [3]. However, the challenge is to extract the enough output current and output voltage to drive the boost converter. The minimum input voltage depends on the output current that the boost converter requires. In our design, the target output current and the output voltage of the charge pump are 5 μA and 0.5 V, respectively.

In this paper, a 0.18-V input voltage charge pump circuit is proposed and fabricated using 65 nm standard CMOS technology [8]. The proposed circuit is implemented by using three-stage charge pump circuit based on voltage doubler structure. It applies forward body bias to every MOSFET by feedback the voltage from the ground, inter-stage and the output voltages. From the measurement results, the output current of the proposed charge pump under 0.18-V input voltage is increased by 170% comparing to conventional one at the output voltage of 0.5 V. The charge pump is suitable for a startup circuit for low voltage operation.

To verify the startup ability of the proposed charge pump circuit, we also implemented the boost converter together with the startup circuit utilizing the proposed charge pump. The measurement results show that the boost converter successfully boosted the 0.18-V input to the output voltage higher than 0.65 V. When the output voltage of the boost converter is boosted higher than 0.65 V, it is sufficient to drive the feedback circuit of the boost converter by using its output voltage [1].

This paper is organized as follows. The circuit topology and comparison of the proposed and the conventional charge pumps are described in Sect. 2. The boost converters with the startup circuit are introduced in Sect. 3. The experimental results are shown in Sect. 4. Finally, conclusion will be drawn in Sect. 5.

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2. Charge Pump Circuit

2.1 Circuit Topologies and Operation Principle

Most of the charge pump (CP) circuits are based on the Dickson type CP circuit [9] as shown in Fig. 1. The output current of the Dickson CP greatly decreases at low input voltage (V_{DD}) because of diode connected MOSFET switches. For low voltage applications, the voltage doubler [10] in Fig. 2 is a popular solution. The voltage doubler has a cross coupled switches driven by complementary clocks. When CLK is high, the MN2 and MP1 turn on and the node D1 is charged to V_{DD}. When CLK changes from high to low, the MN1/MP2 turn on and the node U1 is charged to V_{DD}. The node D1 is driven by the capacitor Cd1 and boosted from V_{DD} to $2\,V_{DD}$ thereby charging the node V_{OUT} at the same time. On the next half cycle, the node D1 becomes to V_{DD} and the node U1 is also pumped to $2\,V_{DD}$ which also charges the node V_{OUT}. As a result, the node V_{OUT} can always been charged to $2\,V_{DD}$.

The conventional 3-stage voltage doubler with zero body bias is shown in Fig. 3. Since the deep n-well is available in this process, the bodies of all the MOSFETs are connected to their sources respectively to avoid the body effect. The operation of the inter-stage output voltages V_{O1} and the V_{O2} are described as follows. When CLK is high, the MOSFETs MP1/MN4 turn on and the V_{O1} is charged to $2\,V_{DD}$ from the node U1 to D2. On the other half cycle, the MP2/MN3 turn on and the Vo1 is also charged to $2\,V_{DD}$. The node Vo2 is operated likewise and can be pumped to $3\,V_{DD}$. As a result, each of the inter-stage voltage can be pumped to a fixed DC value. To clamp the output voltage, we added a P-N diode to V_{OUT}. V_{OUT} is lower than 0.7 V.

For energy harvesting applications, the target input voltage of the proposed CP is 0.18 V, where the MOSFET is operating under the cut-off region. In addition, the large on-resistance of the MOSFETs cause voltage drops and decrease the output voltage, especially when the load requires large current. To alleviate this problem, we propose the CP circuit which applies the forward body bias to each MOSFET, as shown in Fig. 4. The proposed CP reduces the turn-on resistance of the MOSFETs and keeps the output voltage even the output current increases. Since the source terminal of each MOSFET is pumped to different voltage, the three-stage CP circuit requires six different voltages to provide the forward body bias. However, it is very difficult to generate six different body voltages. In the proposed circuit, all of the forward body biases are provided by the self-pumped voltage or the ground by only adding an additional CP stage. Each body of nMOSFET is biased to the next stage output (i.e. the body of 2nd stage nMOSFETs are biased from 3rd output voltage V_{OUT}) and each body of pMOSFET is biased to the input voltage of the previous stage (i.e. the body of 2nd stage pMOSFETs are biased from 1st input voltage V_{DD}). In case of pMOSFETs in the first stage, since there is no previous stage, the bodies of the pMOSFETs are connected to the ground. In case of nMOSFETs in the third stage, we added an additional stage to provide the forward

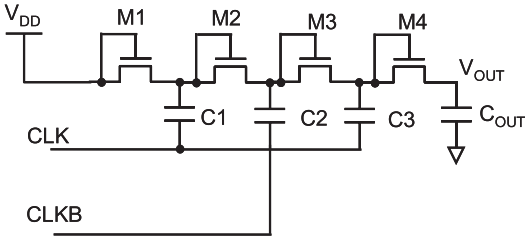

Fig. 1 The circuit schematics of the 3-stage Dickson charge pump circuit.

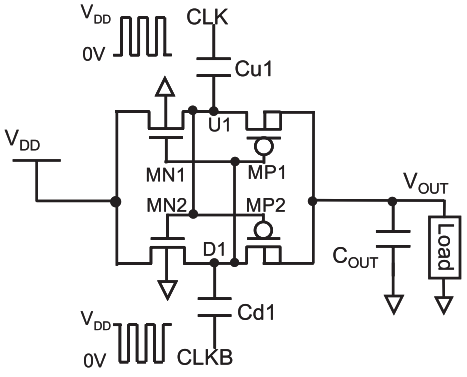

Fig. 2 The circuit schematic of the conventional voltage doubler.

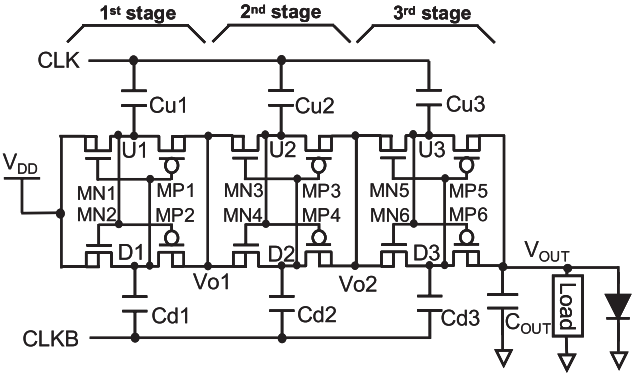

Fig. 3 Conventional 3 stages voltage doubler with zero body bias.

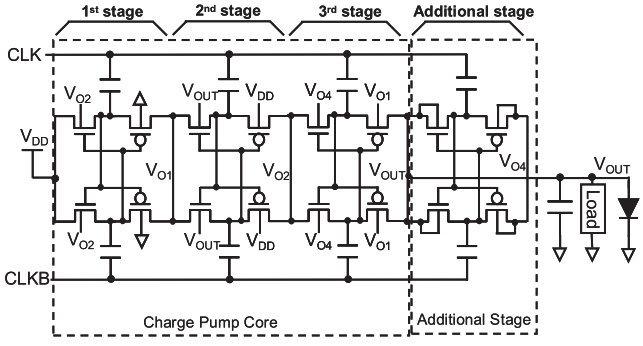

Fig. 4 Proposed 3-stage charge pump circuit with forward body bias.

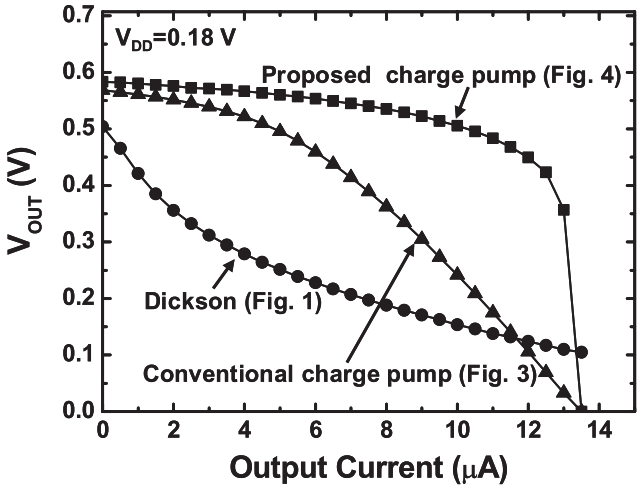

Fig. 5 Simulated dependence of output voltages of Dickson, the conventional and the proposed charge pumps on output current at 0.18-V input voltage and fixed area.

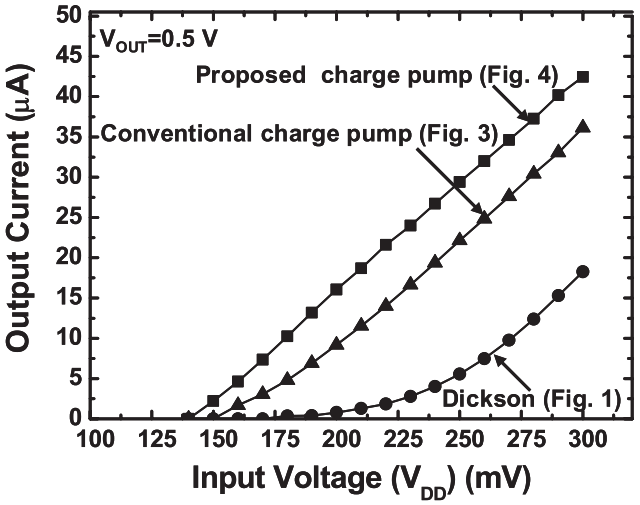

Fig. 6 Simulated dependence of output current of Dickson, the conventional and the proposed charge pumps on input voltages at 0.5-V output voltage and fixed area.

body bias. The additional stage is implemented by using two small capacitors and MOSFETs with 1.5% area overhead since it is only used to provide the forward body bias.

Although the operation voltage is much lower than the threshold voltage, the inverter-based ring oscillator can generate the clock signal under 0.18-V supply voltage. The minimum operation voltage (V_{DDMIN}) of the CMOS inverter ring oscillator can be as low as 0.1 V [11]. We have simulated the ring oscillator under 0.18 V, and it did generate the 10-MHz clock signal. Therefore, we applied 10-MHz clock signal for the CP.

2.2 Simulation Results and Comparison

The performances of the CPs in Sect. 2.1 are compared using SPICE simulation with 65 nm CMOS process. The gate width of the transistors in charge pump core and additional stage are 324 μm and 54 μm, respectively. The gate length uses minimum value in 65-nm CMOS. The characteristics of the proposed circuit (Fig. 4) are compared with the Dickson's CP (Fig. 1) and the conventional CP (Fig. 3) under 10-MHz clock frequency. The proposed and the conventional 3-stage CPs are compared with 3-stage Dickson's charge pump because the stages of the CP depends on the number of pumping stages, not the number of series-connected MOSFETs. For fair comparison, the area of total pumping capacitors and the number of pumping stages should be the same. Therefore, the pumping capacitors in the Dickson's CP and the conventional CP are set to 25.2 pF and 12.6 pF, respectively and the number of pumping stage is set to be three. All of the on-chip capacitors are implemented by using metal-insulator-metal (MIM) capacitor. For the simulation, we added the 70-pF load capacitor (C_{OUT}) to obtain the stable output waveform.

Figure 5 compares the dependence of output voltages of Dickson, the conventional and the proposed CPs on output currents at 0.18-V input voltage. The output voltages of all the circuits are reduced with the increasing output current. However, the proposed CP keeps the highest output voltage compared to the other CPs.

Figure 6 compares the dependence of output current of Dickson, the conventional and the proposed CPs on input voltage when the output voltage is 0.5 V, which is closed to the threshold voltage of this process. As can be seen, the proposed CP has the highest output current, especially at lower input voltage. Therefore, the proposed circuit is suitable for extremely low-voltage applications such as energy harvesting.

3. Boost Converter with Startup Circuit

Figure 7 shows the system diagram of the proposed boost converter. It consists of a CP circuit, a clock generator, and a boost converter. Figure 8 shows the detail circuit schematics of the boost converter and the clock generator. The clock generator consists of the ring oscillator, duty cycle generator and buffer chains to drive the power switches of the boost converter.

To kick-up the boost converter from low input voltage, clock signals with high amplitude and high duty cycle is required to drive the power MOSFETs. Because the design target of the boost converter is 0.18-V input voltage and higher than 0.65-V output voltage, the clock amplitude should be larger than 0.5-V which is higher than threshold voltage of the MOSFET. In addition, the duty cycle of more than 80% is also required. In order to generate the 0.5-V output voltage with output current larger than 5 μA, the proposed CP in previous section is used. The proposed CP circuit is driven by the 0.18-V input voltage and 0.18-V swing clock signal. In addition, the input voltage of the boost converter is also provided from the input voltage (V_{DD}).

The boost converter shown in Fig. 7 can be triggered from 0.18-V input voltage and the output voltage can be

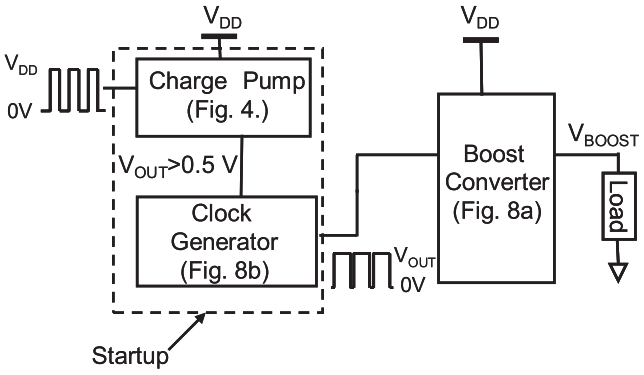

Fig. 7 Block diagram of the boost converter applying proposed 3-stage charge pump with forward body bias as a startup circuit.

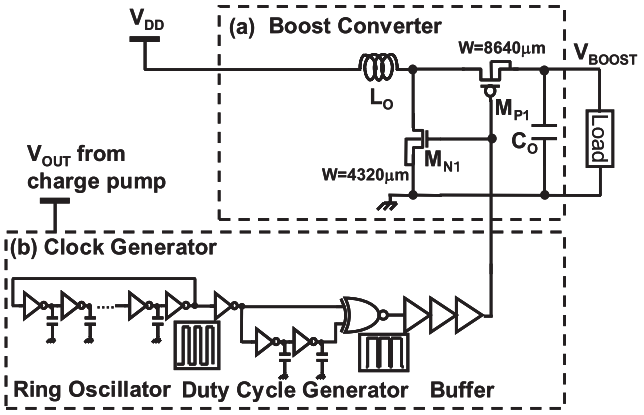

Fig. 8 Circuit schematics of the (a) boost converter and (b) clock generator.

higher than 0.65 V. When the output voltage of the boost converter is boosted to higher than 0.65 V [1], the control circuitry can be driven by the output of the boost converter itself and the startup circuit including the CP can be stopped. Therefore, the power consumption caused by the startup circuit is not an issue and will not affect the power conversion efficiency of the boost converter.

4. Experimental Result

4.1 Measurement Results of Charge Pump Circuits

A test chip was fabricated using 65 nm standard CMOS technology. The microphotograph of the proposed CP circuits (Fig. 4) is shown in Fig. 9. Each pumping capacitor of the CP core and the additional stage is 12.3 pF and 0.4 pF, respectively and the clock frequency is set to 10 MHz. The chip area of the proposed CP is 0.3 mm^2 including all test pads. As can be seen, the area overhead of the additional stage in this design is 1.5%.

To show the effectiveness of the forward body bias, we also fabricated the conventional CP with zero body bias (Fig. 3) for comparison. The layout is the same with the proposed circuit excluding the body connection of the MOSFET and the additional stage.

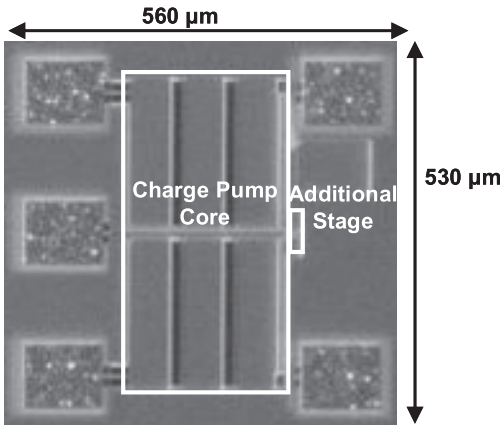

Fig. 9 Photographs of the proposed 3-stage charge pump circuit with forward body bias. Area overhead of additional stage is 1.5%.

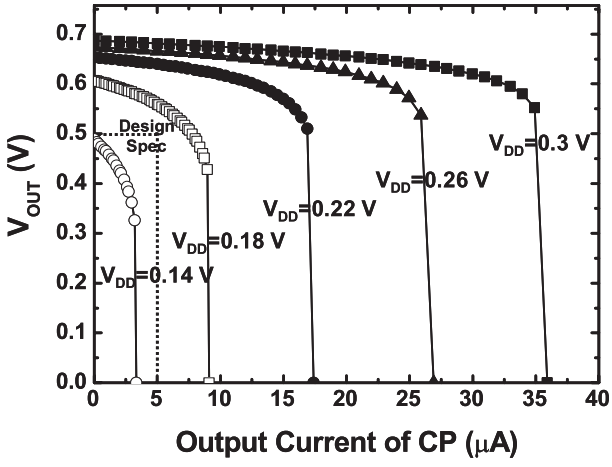

Fig. 10 Measured dependence of output voltage of proposed charge pump circuit on output current with different input voltages (V_{DD}).

Figure 10 shows the measured dependence of output voltage of the proposed CP circuit on output currents with different V_{DD}. In the proposed CP, we added a P-N diode at the output to clamp the output voltage, as shown in Fig. 4. Therefore, the measured output voltage differs from the ideal output voltage. As V_{DD} increases, the output current of the CP also increases. Therefore, the minimum required V_{DD} depends on the output current that driver circuit of boost converter consumes. In our design, to startup the boost converter, the target CP output voltage and the output current are 0.5 V and 5 μA, respectively. The input voltage of 0.18 V can meet the design target.

The measured dependence of output voltages of the proposed and the conventional CPs on output current at 0.18-V input voltage under various process corners are shown in Fig. 11. FF means fast nMOS and fast pMOS. TT means typical nMOS and typical pMOS. SS means slow nMOS and slow pMOS. These corner chips are provided by the foundry. As can be seen, the proposed CP circuit has higher V_{OUT} than the conventional CP especially when the output current increases. At the target output voltage of

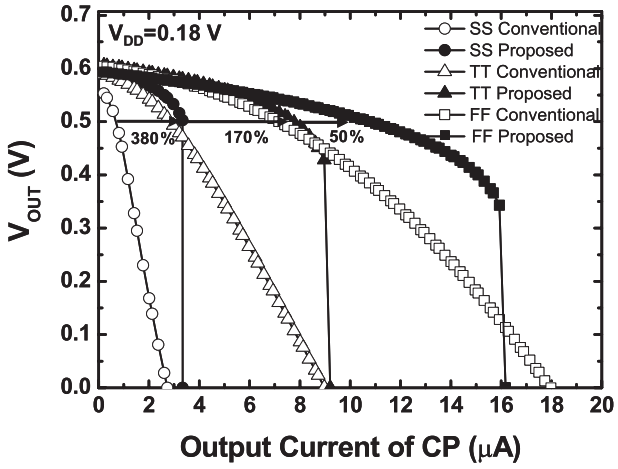

Fig. 11 Measured dependence of output voltage of proposed (Fig. 4) and conventional (Fig. 3) charge pumps on output current at 0.18-V input voltage under various process corners.

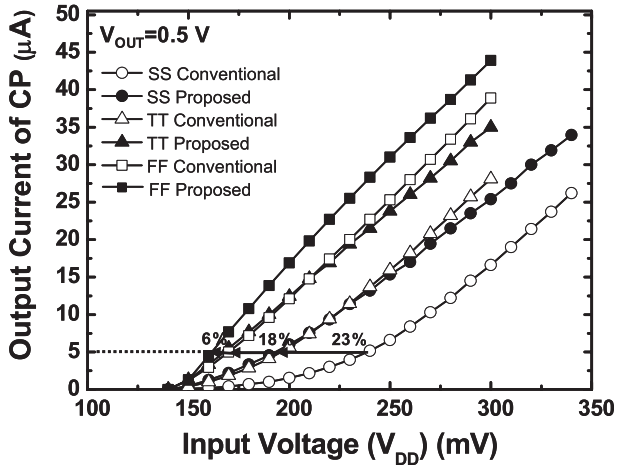

Fig. 12 Measured dependence of output current of proposed (Fig. 4) and conventional (Fig. 3) charge pumps on input voltage (V_{DD}) at 0.5-V output voltage under various process corners.

0.5 V, compared with the conventional CP, the output current of the proposed CP is increased by 380%, 170% and 50% for SS, TT and FF corner, respectively. This improvement can reduce the chip area of the CP circuit which is limited by size of pumping capacitors. Figure 12 compares the measured dependence of output current of the conventional and the proposed CPs on input voltage at 0.5-V output voltage under various process corners. As can be seen, at the target output current of 5 μA, compared with the conventional CP, the V_{DD} of the proposed CP is decreased by 23%, 18% and 6% for SS, TT and FF corners, respectively. Although applying forward body bias requires considering the latch-up issues, the proposed circuit does not latch-up because a diode is added at the output as shown in Fig. 4.

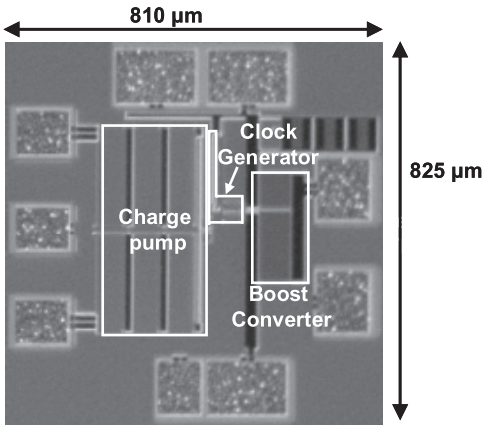

Fig. 13 Photographs of the boost converter integrated with the proposed charge pump circuit as the startup circuit.

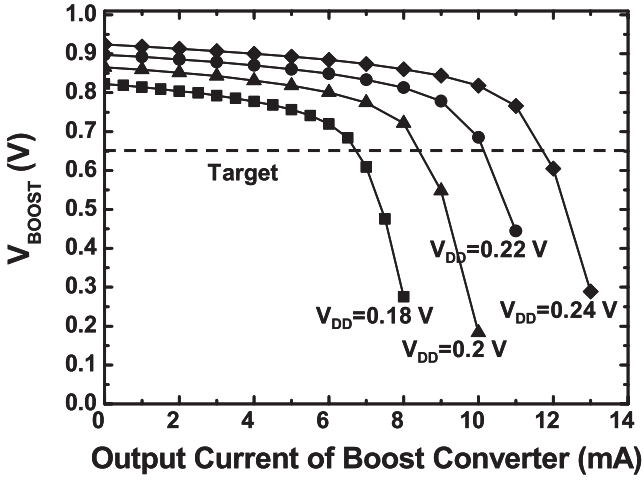

Fig. 14 Measured dependence of output voltage of the boost converter with startup circuit on output current of the boost converter with different input voltages (V_{DD}).

4.2 Measurement Results of Boost Converter Integrated with Startup Circuit

To verify the proposed CP can be used as startup circuit for low voltage boost converter, we also fabricated the boost converter test chip which integrated with the proposed CP as the startup circuit. Figure 13 shows the chip microphotograph of this test chip. The chip area including all test pads is 0.67 mm^2. The off-chip inductor with 4.7 μH and output capacitor of 3.3 μF is used. The measured dependence of output voltage of the boost converter with startup circuit on output current of the boost converter is shown in Fig. 14. It proves that the boost converter can be boosted up to larger than 0.65 V even V_{DD} of 0.18 V, which satisfy the design target. Larger V_{DD} provides higher output voltage and larger output current of the boost converter. These output voltages are enough for the feedback circuit to regulate and control the output voltage.

The comparison of recently published boost converters

Table 1 Comparison with published boost converters applying startup mechanism.

	Tech.	Startup Mechanism	Min. Input Voltage	Min. Startup Voltage	Output Voltage	Note
[1]	130-nm CMOS	External voltage	0.02V	0.65V	1V	External Voltage is required
[2]	350-nm CMOS	Mechanical switch	0.025V	0.035V	1.8V	Vibration is required
[3]	350-nm SOI -BCD	Charge pump	0.36V	0.36V	3.6V	Separate startup IC is applied
[5]	600-nm CMOS	Oscillator based. No voltage booster	1V	1V	1.5V	1-chip integration
[6]	500-nm CMOS	Oscillator based. No voltage booster	0.7V	1.1V	4.4V	1-chip integration
[7]	600-nm CMOS	Oscillator based. No voltage booster	0.6V	0.9V	3.3V	1-chip integration
This Work	65-nm CMOS	Charge pump with forward body bias	0.18V	0.18V	>0.65V	1-chip integration

applying startup mechanism is shown in Table 1. The minimum input voltage means the minimum input voltage of boost converter after the boost converter finishes the startup mechanism. The minimum startup voltage means that the minimum input voltage to enable the startup functions. The boost converter in [1] and [2] can startup from extremely low input voltage. However, [1] requires 0.65-V external voltage to startup the system. [2] requires mechanical vibrations and the application is limited. In [3], the boost converter starts at 0.36 V by using separate CP IC as startup circuit is proposed. The CP IC uses fully depleted Silicon on Insulator (SOI) to enable low-voltage operation. In [5]–[7], the boost converters are implemented together with the startup circuit by using the standard CMOS technology. Since they do not use voltage booster as startup circuit, the startup voltage is higher (> 0.9 V) than the input voltage provided from the energy harvesting sources. Utilizing the proposed CP circuit with forward body bias to startup the boost converter provides a solution to use the boost converter from the input voltage of 0.18 V by using the standard CMOS technology. It does not require the external high voltage input or mechanical switches to startup the circuit.

5. Conclusion

To startup the boost converter in low operation voltage, the charge pump circuit with forward body bias is proposed and fabricated with 65 nm CMOS process. At the target output voltage of 0.5 V, compared with the conventional CP with zero body bias, the output current of the proposed CP is increased by 380%, 170% and 50% for SS, TT and FF corner, respectively. At the target output current of 5 μA, compared with the conventional CP, the V_{DD} of the proposed CP is decreased by 23%, 18% and 6% for SS, TT and FF corner, respectively. The area overhead of the additional stage in the proposed CP circuit is only 1.5%. The boost converter connected with the proposed CP can boost the output voltage of boost converter to larger than 0.65 V when the input voltage is 0.18 V. With the higher pumping ability and the lower startup voltage, the proposed CP circuit is suitable for energy harvesting applications.

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