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0.5-V Input Digital Low-Dropout Regulator (LDO) with 98.7% Current Efficiency in 65 nm CMOS

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SUMMARY In this paper, Digital Low Dropout Regulator (LDO) is proposed to provide the low noise and tunable power supply voltage to the 0.5-V near-threshold logic circuits. Because the conventional LDO feedback-controlled by the operational amplifier fail to operate at 0.5 V, the digital LDO eliminates all analog circuits and is controlled by digital circuits, which enables the 0.5-V operation. The developed digital LDO in 65 nm CMOS achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7-μA quiescent current at 200-μA load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's, which indicates the good energy efficiency of the digital LDO at 0.5-V operation.

key words: *low dropout regulator, digital control, low voltage*

1. Introduction

Very low-voltage operation of VLSI's is effective in reducing both dynamic and leakage power and the maximum energy efficiency is achieved at low power supply voltage (V_{DD}) below 0.5 V (e.g., 340 mV [1] and 320 mV [2]). Thus, many works have been carried out on the sub/near-threshold logic circuits [1]–[5]. Stable and tunable VDD (e.g., 320 mV±50 mV [2]) is required in the near-threshold logic circuits, because the gate delay in the near-threshold logic circuits is very sensitive to V_{DD} and the process variations. Therefore, a 0.5-V LDO enabling the low ripple and tunable V_{DD} is strongly required. The conventional analog LDO, however, fails to operate at 0.5 V. In order to solve the problem, the digital LDO [6] enabling the 0.5-V operation is proposed and demonstrated in this paper. The concept and the circuit implementation of the proposed digital LDO is shown in Sect. 2. Measurement results from 65-nm CMOS test chips are described in Sect. 3.

2. Proposed Digital LDO

2.1 Concept and Schematic of the Proposed Digital LDO

In order to explain the concept of the proposed digital LDO, Fig. 1 shows the circuit schematic of the digital LDO in contrast with the conventional analog LDO. The conventional analog LDO shown in Fig. 1(a) consists of an operational amplifier and a power transistor. The conventional LDO fails to operate at 0.5 V, because the operational amplifier does not operate at 0.5 V and cannot control the analog gate voltage of the power transistor. In order to solve the problem, the digital LDO shown in Fig. 1(b) is proposed. The digital LDO includes a switch array, a comparator, and a digital controller. The analog controlled power transistor is replaced with the switch array and the number of turned-on switches is changed digitally by the controller. The output voltage (V_{OUT}) is monitored by the comparator instead of the operational amplifier. Thus, the digital LDO eliminates all analog circuits and is controlled by digital circuits, which enables the 0.5-V LDO operation, because the digital circuits including the comparator can operate at 0.5 V.

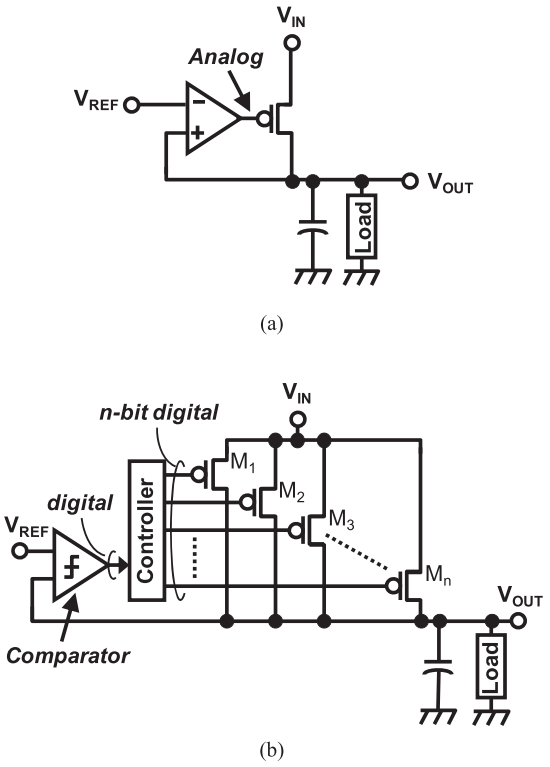

Fig. 1 (a) Conventional analog LDO. (b) Proposed degital LDO.

Figure 2 shows the circuit schematic of the fabricated digital LDO. The digital LDO consists of a comparator, a serial-in parallel-out bi-directional shift register, and switch

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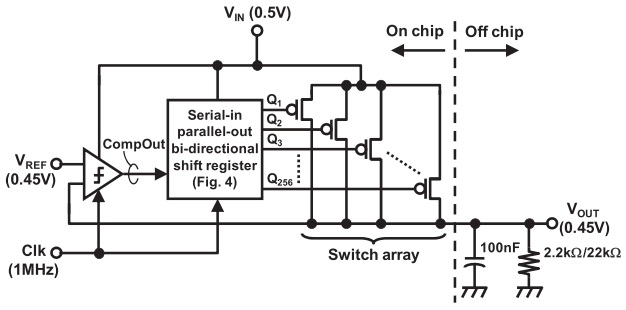


Fig. 2 Circuit schematic of the fabricated digital LDO.

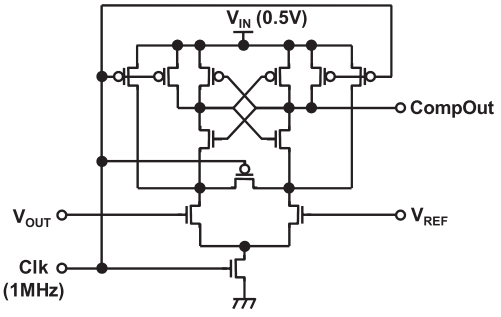


Fig. 3 Circuit schematic of clocked comparator used in digital LDO.

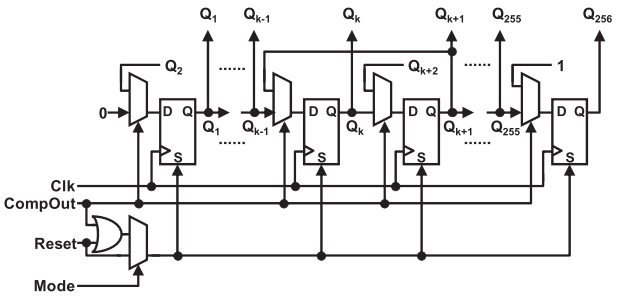


Fig. 4 Circuit implementation of serial-in parallel-out bi-directional shift register.

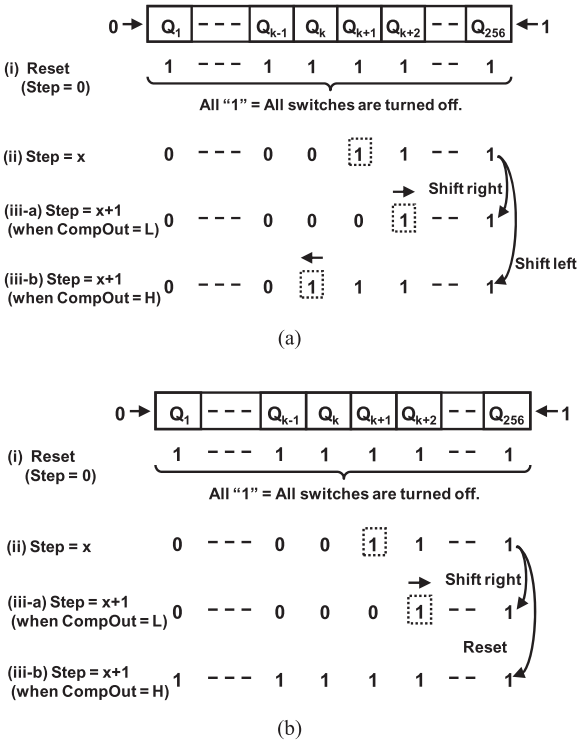


Fig. 5 (a) Up-down control of bi-directional shift register for large I_{LOAD}. (b) Reset control of bi-directional shift register for small I_{LOAD}.

array of 256 pMOS FET's. In order to reduce the ripple due to the switching of the switches, in this implementation, the shift register is used as the controller, because the number of switching in the switch array is only one at each clock edge. The typical input voltage (V_{IN}) and V_{OUT} are 0.5 V and 0.45 V, respectively. The typical clock frequency of the comparator and the shift register is 1 MHz. The off-chip decoupling capacitor is 100 nF and the typical load current (I_{LOAD}) is 200 μA, because most of sub/near-threshold logic circuits can be operated below 200 μA [2], [4], [5]. The current source is used for the static output load in the measurement in Figs. 8, 9 and 12-14, and the resistance of 2.2 kΩ or 22 kΩ is used for the transient output load in the measurement in Fig. 10 and 11. Figure 3 shows the circuit schematic of the clocked comparator used in the digital LDO. In the design of LDO with I_{LOAD} of 200 μA, low quiescent current is very important, because the large quiescent current degrades the current efficiency of LDO. In order to reduce the quiescent current, the clocked comparator is used in the digital LDO, because the clocked comparator can operate at 0.5 V and consumes no DC-power.

2.2 Digital Controller for the Proposed Digital LDO

Figure 4 shows the circuit implementation of the serial-in parallel-out bi-directional shift register for the digital controller in the proposed digital LDO. The bi-directional shift register consists of selectors and D-FF's. In order to achieve a superior transient response of the digital LDO at various ILOAD, two control modes including "up-down control" and "reset control" are implemented in the shift register. When Mode is low, the shift register operates with up-down control. In contrast, when Mode is high, the shift register operates with reset control. The shift-right or the shift-left operation of the bi-directional shift register is determined by the comparator output (CompOut). When CompOut is low, each Q_K except Q_1 moves to Q_{K+1}, and Q_1 is set to "0", which achieves the shift-right operation. In contrast, when CompOut is high, each Q_K except Q_{256} moves to Q_{K-1}, and Q_{256} is set to "1", which achieves the shift-left operation.

Figure 5(a) shows the operation of the bi-directional shift register in the up-down control mode. At first, all 256 bits are set to "1" in order to turn off all pMOS switches. After that, when CompOut is low, which means V_{OUT} is lower than the reference voltage (V_{REF}), all 256 bits are shifted toward right in order to increase the number of turned-on switches. In contrast, when CompOut is high, which means

V_{OUT} is higher than V_{REF}, all 256 bits are shifted toward left in order to decrease the number of turned-on switches. Similarly, Fig. 5(b) shows the operation of the shift register in the reset control mode. Unlike the up-down control mode, when CompOut is high, which means V_{OUT} is higher than V_{REF}, all 256 bits are set to "1" in order to turn off all pMOS switches.

In this up-down control mode, the ideal DC voltage gain of the feedback loop achieves infinity, because the shift register achieves the integrated operation. Therefore, PSRR is good when the power supply noise frequency is lower than the clock frequency of the digital LDO.

Figure 6 shows the schematic of the transient of the number of turned-on switches in order to explain the feedback control of the digital LDO with the up-down control mode and the reset control mode. I_{LOAD} is large and small in Figs. 6(a) and (b), respectively. The digital LDO controls the number of turned-on switches at each clock edge depending on CompOut. At first, the number of charged to V_{REF} (=target voltage) and I_{LOAD} is supplied turned-on switches increases until the output capacitor is through the switches. After that, when V_{OUT} equals to V_{REF}, the number of turned-on switches is equals to I_{LOAD} and changes up and down by 1-bit, which determines the ripple of the digital LDO.

As shown in Fig. 6(a), when I_{LOAD} is large, the overshoot of V_{OUT} is suppressed with the up-down control mode, because the charging current of the output capacitor is smaller than I_{LOAD}. In contrast, as shown in Fig. 6(b), when I_{LOAD} is small, the overshoot of V_{OUT} is large with the up-down control mode, because the charging current of the output capacitor is larger than I_{LOAD}. The measured overshoot waveforms V_{OUT} with the up-down control mode will be shown in Fig. 11. In order to reduce the overshoot of V_{OUT} at small I_{LOAD}, the reset control mode is proposed. As shown in Fig. 6(b), when I_{LOAD} is small, the overshoot of V_{OUT} is reduced with the reset control mode, because all pMOS switches are turned off, when V_{OUT} is higher than V_{REF}. In contrast, as shown in Fig. 6(a), when I_{LOAD} is large, the ripple of V_{OUT} is large with the reset control mode, because all pMOS switches are turned off. The measured waveforms V_{OUT} with the reset control mode will be shown in Fig. 11. Therefore, in this paper, in order to achieve superior transient characteristics, the up-down control mode is proposed for large I_{LOAD} and the reset control mode is proposed for small I_{LOAD}.

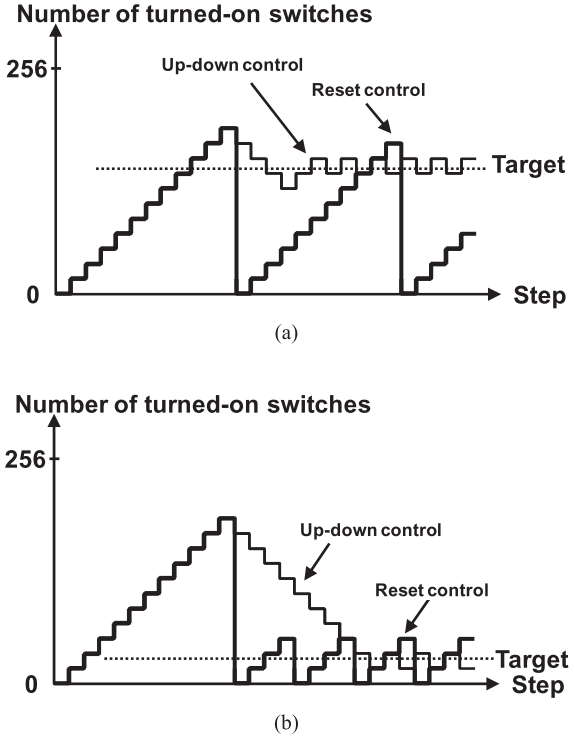


Fig. 6 Schematic of the transient of the number of turned-on switches in order to explain the feedback control of the digital LDO with the up-down control mode and the reset control mode. (a) Load current I_{LOAD} is large. (b) Load current I_{LOAD} is small.

3. Measurement Results and Discussion

To demonstrate the advantage of the proposed digital LDO, a test chip is fabricated in 65 nm CMOS. Figure 7 shows the chip microphotograph and the layout. The total chip area including pads is $0.9 \times 0.8\,mm^2$ and the active area of the digital LDO is $0.042\,mm^2$.

In the following measurements, the up-down control mode is used except Fig. 11. Figure 8(a) shows measured V_{OUT}–V_{IN} characteristics at I_{LOAD} of $200\,\mu A$. V_{REF} is varied from 0.35 V to 0.55 V by 0.05-V step. The digital LDO successfully regulates V_{OUT} from 0.35 to 0.45 V at V_{IN} of 0.5 V. At the design target of V_{IN} of 0.5 V and V_{OUT} of 0.45 V, the dropout voltage is 50 mV and the measured line regulation is 3.1 mV/V. Figure 8(b) shows measured V_{OUT}–V_{IN} characteristics at V_{REF} of 0.45 V. I_{LOAD} is varied from $20\,\mu A$ to $200\,\mu A$. The LDO achieves a successful load regulation of 0.65 mV/mA with V_{IN} from 0.5 V to 1.2 V.

Figure 9 shows the measured I_{LOAD} dependence of the current efficiency and the quiescent currents at 1-MHz and 10-MHz clock. Thanks to the digital LDO architecture, the measured quiescent current does not depend on I_{LOAD}, though the quiescent current increases with I_{LOAD} in the conventional analog LDO. At 1-MHz clock, the measured quiescent current is $2.7\,\mu A$, which is the smallest quiescent

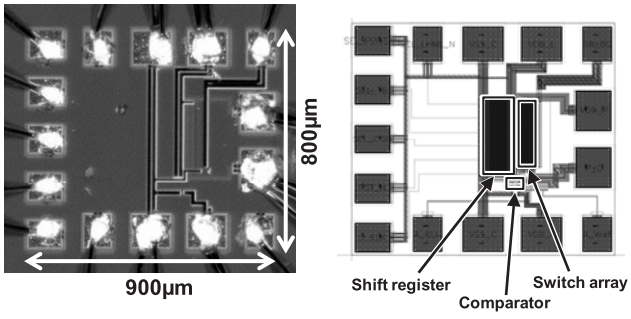
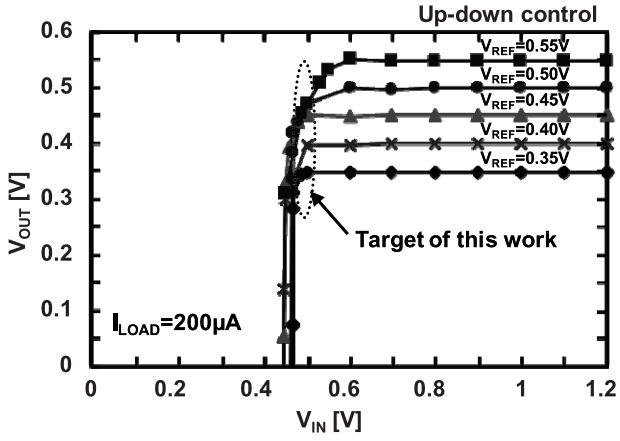
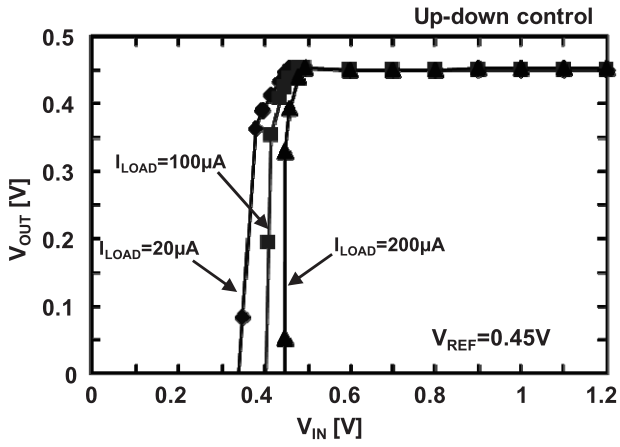


Fig. 7 Chip microphotograph and layout.



(a)



(b)

Fig. 8 (a) Measured V_{OUT}-V_{IN} characteristics. (a) V_{REF} is varied from 0.35 V to 0.55 V at I_{LOAD} of 200 μA. (b) I_{LOAD} is varied from 20 μA to 200 μA at V_{REF} of 0.45 V.

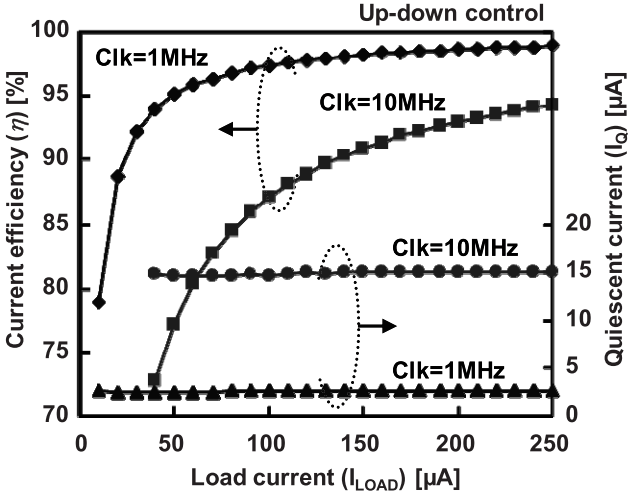


Fig. 9 Measured I_{LOAD} dependence of the current efficiency and the quiescent currents at 1-MHz and 10-MHz clock.

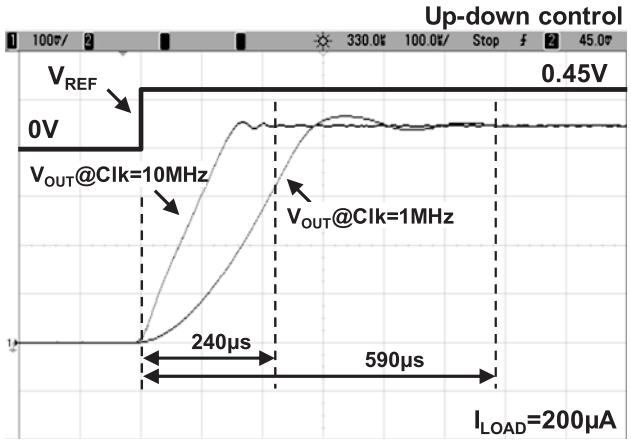


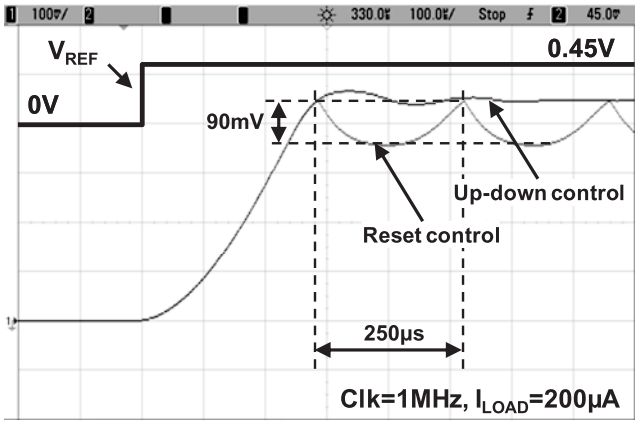
Fig. 10 Measured transient waveform of V_{OUT} when V_{REF} changes from 0 V to 0.45 V at 1-MHz and 10-MHz clock and I_{LOAD} of 200 μA.

current in LDO's to the author's knowledge. The current efficiency is 98.7% at I_{LOAD} of 200 μA.

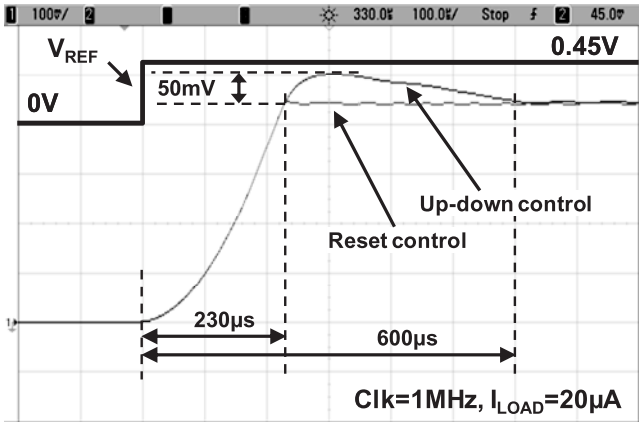
Figure 10 shows the measured transient waveform of V_{OUT} when V_{REF} changes from 0 V to 0.45 V at 1-MHz and 10-MHz clock and I_{LOAD} of 200 μA. The settling time of V_{OUT} at 1-MHz clock is 590 μs. By increasing the clock frequency from 1-MHz to 10-MHz, the settling time can be reduced by 60% from 590 μs to 240 μs at the cost of increasing quiescent current from 2.7 μA to 15 μA and the corresponding degradation of the current efficiency by 5% at I_{LOAD} of 200 μA as shown in Fig. 9. The tunable performance by changing the clock frequency is the advantage of the digital LDO.

Figures 11(a) and (b) show the measured transient waveforms of V_{OUT} with the up-down control mode and the reset control mode when V_{REF} changes from 0 V to 0.45 V at 1-MHz clock and I_{LOAD} of 200 μA and 20 μA, respectively. As shown in Fig. 11(a), the overshoot of V_{OUT} is suppressed with the up-down control mode and I_{LOAD} of 200 μA. As shown in Fig. 11(b), however, the 50-mV overshoot of V_{OUT} and 600-μs settling time are observed with the up-down control mode and I_{LOAD} of 20 μA as shown in Fig. 6(b). In order to solve the problem, the reset control mode clearly eliminates the overshoot of V_{OUT} and reduces the settling time from 600 μs to 230 μs. As shown in Fig. 11(a), however, the reset control mode generates the 90-mV ripple at I_{LOAD} of 200 μA as shown in Fig. 6(a). Therefore, in this paper, in order to achieve superior transient characteristics, the up-down control mode is proposed for large I_{LOAD} and the reset control mode is proposed for small I_{LOAD}.

Figure 12 shows the measured transient waveform of V_{OUT} when V_{REF} changes between 0.4 V to 0.45 V at 100 Hz. The clock frequency is 1-MHz and I_{LOAD} is 200 μA. Figure 13 shows the measured transient waveform of V_{OUT} when I_{LOAD} changes between 0 A to 200 μA at 100 Hz. V_{OUT} is 0.45 V and the clock frequency is 1-MHz. The measured undershoot and overshoot of V_{OUT} are 40 mV and 30 mV, respectively. As shown in Figs. 12 and 13, these results show reasonable performance of the digital LDO to be



(a)



(b)

Fig. 11 Measured transient waveform of V_{OUT} when the up-down control mode and reset control mode when V_{REF} changes from 0 V to 0.45 V at 1-MHz clock. (a) Load current I_{LOAD} is 20 μA. (b) Load current I_{LOAD} is 20 μA.

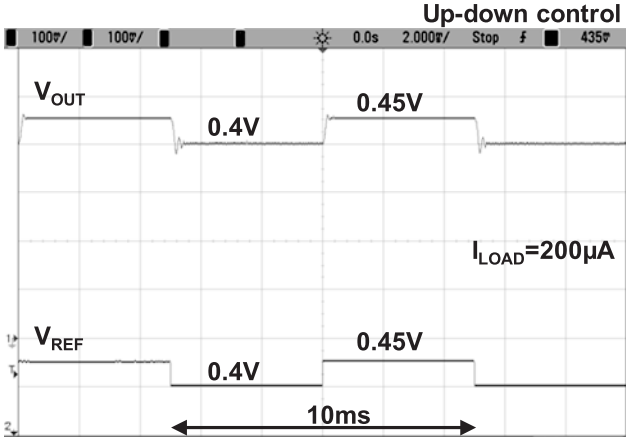


Fig. 12 Measured transient waveform of V_{OUT} when V_{REF} changes between 0.4 V to 0.45 V at 100 Hz. The clock frequency is 1-MHz and I_{LOAD} is 200 μA.

applied to the power supply for near-threshold logic circuit.

Since the switch array in the digital LDO is switched digitally, the clock-related digital noise may cause LDO

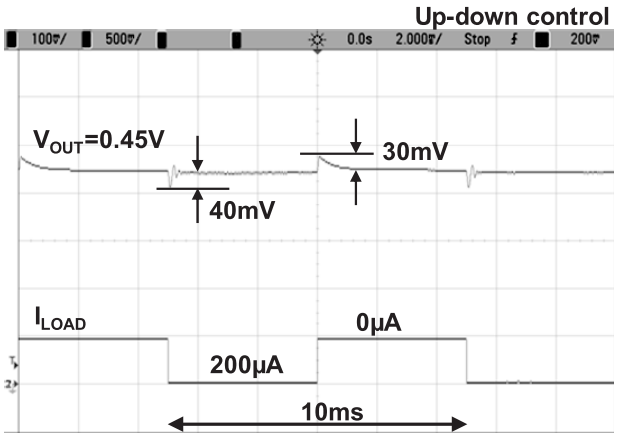


Fig. 13 Measured transient waveform of V_{OUT} when I_{LOAD} changes between 0.4 A to 200 μA at 100 Hz. V_{OUT} is 0.45 V and the clock frequency is 1-MHz.

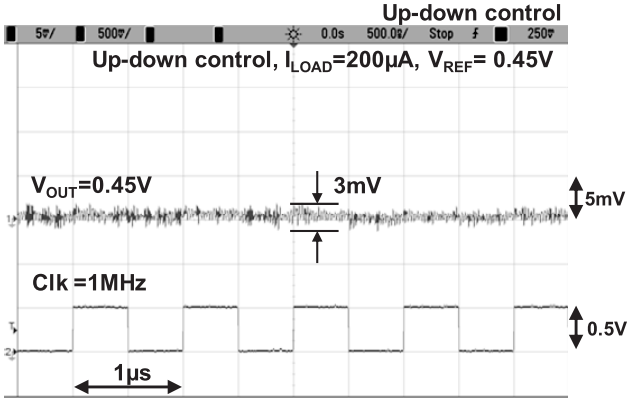


Fig. 14 Measured waveform of V_{OUT} and 1-MHz clock. V_{OUT} is 0.45 V and I_{LOAD} is 200 μA.

output ripple. To evaluate the ripple caused by the digital noise, output ripple is measured as shown in Fig. 14. V_{OUT} is 0.45 V and the clock frequency is 1-MHz. The ripple of V_{OUT} is less than 3 mV. The measured V_{OUT} shows no significant ripple at clock edges and its harmonic tones, which indicates that the clock-related digital noise does not affect the LDO output ripple in the developed digital LDO.

The key performance summary of the proposed digital LDO and comparison with some previous regulators are listed in Table 1. The digital control is proposed in [7]. The regulator in [7], however, is not LDO but a half V_{DD} generator. In this paper, both the digital LDO and 0.5-V LDO are demonstrated for the first time. The developed digital LDO achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7-μA quiescent current at 200-μA load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's.

4. Conclusion

In this paper, the digital LDO enabling the 0.5-V operation

Table 1 Key pwerformance summary of the proposed digital LDO and comparison with previous regulators.

	Unit	[7]	[8]	[9]	[10]	This work
Type of regulator	-	Half V_{DD} generator	LDO	LDO	LDO	LDO
Control	-	Digital	Analog	Analog	Analog	Digital
CMOS Technology	-	90nm	90nm	350nm	350nm	65nm
Active area	mm^2	0.03	0.008	0.264	0.053	0.042
Minimum input voltage	V	2.4	1.2	2	1.05	0.5
Nominal output voltage	V	1.2	0.9	1.8	0.9	0.45
Maximum load current	mA	1000	100	200	50	0.2
Line regulation	mV/V	-	-	2	1.1	3.1
Load regulation	mV/mA	-	1	0.17	0.06	0.65
Decoupling capacitor	μF	0.0024 (on-chip)	0.0006 (on-chip)	1 (off-chip)	1 (off-chip)	0.1 (off-chip)
Quiescent current	μA	25700	6000	20 to 320	4.02 to 164	2.7
Current efficiency	%	97.5	94.3	99.8	99.7	98.7

is proposed and demonstrated for the first time. In order to achieve superior transient characteristics, both the up-down control mode for large I_{LOAD} and the reset control mode for small I_{LOAD} are proposed. The developed digital LDO in 65 nm CMOS achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7-μA quiescent current at 200-μA load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's, which indicates the good energy efficiency of the digital LDO at 0.5-V operation.

Acknowledgments

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References

[1] A. Agarwal, Amit, S. Mathew, S. Hsu, M. Anders, H. Kaul, F. Sheikh, R. Ramanarayanan, S. Srinivasan, R. Krishnamurthy, and S. Borkar, "A 320 mV-to-1.2 V on-die fine-grained reconfigurable fabric for DSP/Media accelerators in 32 nm CMOS," IEEE International Solid-State Circuits Conference, pp.328–329, Feb. 2010.

[2] H. Kaul, M. Anders, S. Mathew, S. Hsu, A. Agarwal, R. Krishnamurthy, and S. Borkar, "A 320 mV 56 μW 411GOPS/Watt ultra-low voltage motion estimation accelerator in 65 nm CMOS," IEEE International Solid-State Circuits Conference, pp.316–317, Feb. 2008.

[3] B. Calhoun and A. Chandrakasan, "Ultra-dynamic voltage scaling (UDVS) using sub-threshold operation and local voltage dithering," IEEE J. Solid-State Circuits, vol.41, no.1, pp.238–245, Jan. 2006.

[4] S. Hanson, B. Zhai, M. Seok, B. Cline, K. Zhou, M. Singhal, M. Minuth, J. Olson, L. Nazhan-dali, T. Austin, D. Sylvester, and D. Blaauw, "Performance and variability optimization strategies in a sub-200 mV, 3.5 pJ/inst, 11 nW subthreshold processor," IEEE Symposium on VLSI Circuits, pp.152–153, June 2007.

[5] M. Hwang, A. Raychowdhury, K. Kim, and K. Roy, "A 85 mV 40 nW process-tolerant subthreshold 8×8 FIR filter in 130 nm technology," IEEE Symposium on VLSI Circuits, pp.154–155, June 2007.

[6] Y. Okuma, K. Ishida, Y. Ryu, X. Zhang, P. Chen, K. Watanabe, M. Takamiya, and T. Sakurai, "0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65 nm CMOS," IEEE Custom Integrated Circuits Conference, pp.323–326, Sept. 2010.

[7] P. Hazucha, S.T. Moon, G. Schrom, F. Paillet, D.S. Gardner, S. Rajapandian, and T. Karnik, "A linear regulator with fast digital control for biasing integrated DC-DC converters," IEEE International Solid-State Circuits Conference, pp.536–537, Feb. 2006.

[8] P. Hazucha, T. Karnik, B.A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," IEEE J. Solid-State Circuits, vol.40, no.5, pp.933–940, April 2005.

[9] M. Al-Shyoukh, H. Lee, and R. Perez, "A transient-enhanced low-quiescent current low-dropout regulator with buffer impedance attenuation," IEEE J. Solid-State Circuits, vol.42, no.8, pp.1732–1742, Aug. 2007.

[10] Y.H. Lam and W.H. Ki, "A 0.9 V 0.35 μm adaptively biased CMOS LDO regulator with fast transient response," IEEE International Solid-State Circuits Conference, pp.442–443, Feb. 2008.

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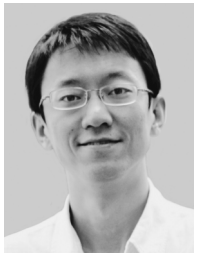

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