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# A Variable Output Voltage Switched-Capacitor DC-DC Converter with Pulse Density and Width Modulation (PDWM) for 57% Ripple Reduction at Low Output Voltage

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**SUMMARY** In this paper, a novel switched-capacitor DC-DC converter with pulse density and width modulation (PDWM) is proposed with reduced output ripple at variable output voltages. While performing pulse density modulation (PDM), the proposed PDWM modulates the pulse width at the same time to reduce the output ripple with high power efficiency. The prototype chip was implemented using 65 nm CMOS process. The switched-capacitor DC-DC converter has 0.2-V to 0.47-V output voltage and delivers 0.25-mA to 10-mA output current from a 1-V input supply with a peak efficiency of 87%. Compared with the conventional PDM scheme, the proposed switched-capacitor DC-DC converter with PDWM reduces the output ripple by 57% in the low output voltage region with the efficiency penalty of 2%.

***key words:*** *DC-DC converter, low ripple, low voltage, pulse density modulation, pulse width modulation, switched-capacitor*

## 1. Introduction

For emerging ultra-low power SoCs which utilize near-threshold or sub-threshold supply voltages and draw less than 10 mA of current [1], [2], a switched-capacitor (SC) DC-DC converter is a viable choice for its tunable output voltage and the probability of on-chip full integration [3]. However, the previously reported SC DC-DC converters [3]–[8] often overlook the effect of output ripple on the sub-threshold digital circuits.

With the trend of the power supply voltage ($V_{DD}$) scaling, power supply ripple is extremely detrimental to their digital building blocks. This is because the delay of logic circuits is influenced by $V_{DD}$ in an exponential way in the sub-threshold region. The net result is that a very small amount of injected ripple can cause a very large delay uncertainty. Figure 1 clearly shows such impact of power supply ripples ($V_{Ripple}$) on the frequency of an FO4-per-stage ring oscillator. The central frequency $f_{center}$ is obtained at $V_{DD}$ = 200 mV. The upper and lower bounds of the frequency, i.e., $f_{max}$ and $f_{min}$, are obtained at $V_{DD} = 200\,mV + V_{Ripple}/2$ and $V_{DD} = 200\,mV - V_{Ripple}/2$, respectively. Note that in Fig. 1, $f_{max}$ and $f_{min}$ are normalized to $f_{center}$. As seen, an 80 mV ripple can result in a more than 200% delay uncertainty.

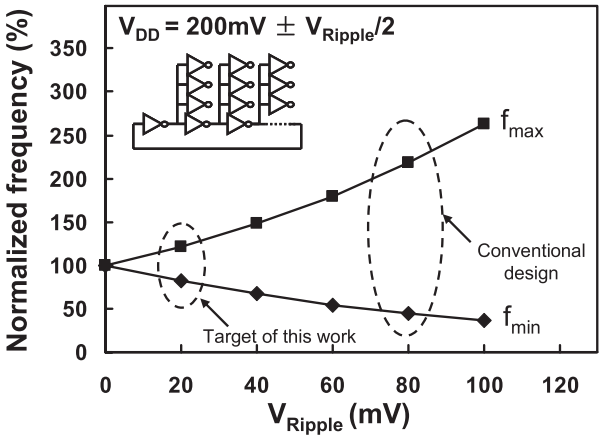


**Fig. 1** Normalized ring oscillator frequency at different power supply ripples and the target of this work.

In the super-threshold region, the ripple of the DC-DC converter and ground-bounce noise (also referred to as Ldi/dt noise) are two major sources of power supply noise at digital blocks. As $V_{DD}$ scales to the sub-threshold region, the transient current of digital blocks also scales rapidly, in this way mitigating the ground-bounce noise. However, the problem of the ripple of the DC-DC converter remains and it even goes severer with the decreasing output voltage.

Motivated by the above concerns, it is of great importance to look for solutions which can reduce the output ripple of switched-capacitor DC-DC converter which supplies variable output voltages to the sub-threshold digital circuits. Interleaving techniques can also be employed for lower ripples [9], however, this method comes with the cost of increased component count and complicated timing control. Therefore, exploring a more effective control scheme [10] to reduce output ripple of switched-capacitor DC-DC converter with the variable output voltages for sub-threshold digital circuits is the focus of this paper.

## 2. Proposed PDWM Control Scheme of SC DC-DC Converter

Conventional SC DC-DC converters employ pulse density

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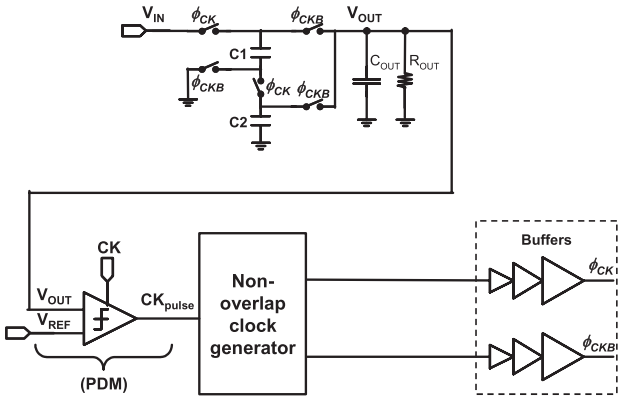



**Fig. 2** Schematic of conventional SC DC-DC converter with only PDM.

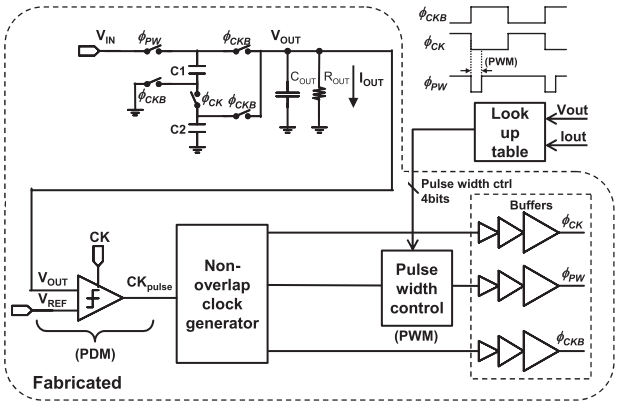



**Fig. 3** Schematic of proposed SC DC-DC converter with PDWM.

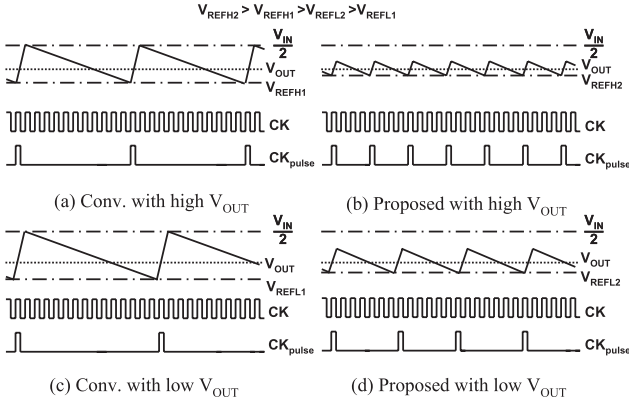



**Fig. 4** Waveforms of conventional and proposed method. (a) conventional PDM with high $V_{OUT}$, (b) proposed PDWM with high $V_{OUT}$, (c) conventional PDM with low $V_{OUT}$, (d) proposed PDWM with low $V_{OUT}$.

modulation (PDM) for feedback control [2]–[4], as shown in Fig. 2. The core of the system is a switch matrix which includes the charge-transfer capacitors and the charge-transfer switches. In this paper, the switching topology of half $V_{IN}$ generator is employed. A PDM based control scheme is used to regulate the output voltage to the desired value with a suitable clock density. The PDM works as follows: a comparator clocked by the clock (CK) is used to compare $V_{OUT}$ and $V_{REF}$. When the output voltage $V_{OUT}$ is above $V_{REF}$, the output of comparator, $CK_{pulse}$ is set to 0, which means switching signals $\phi_{CK}$ and $\phi_{CKB}$ are paused. When $V_{OUT}$ falls below $V_{REF}$, the comparator triggers a pulse on $CK_{pulse}$, which will be transported to $\phi_{CK}$ and $\phi_{CKB}$, thus charges up the output load capacitor ($C_{OUT}$). The non-overlap clock generator is used to eliminate any overlap between $\phi_{CK}$ and $\phi_{CKB}$, thus prevent the power loss while switching. The clock buffers are employed to provide drive ability to the power switches in the switch matrix.

With the above PDM control scheme, pulse densities of $\phi_{CK}$ and $\phi_{CKB}$ are effectively adjusted. The switches are switched less frequently as $I_{OUT}$ decreases, thereby reducing the switching losses and the power consumed by control circuit. With the PDM control scheme, this converter is able to achieve a high power efficiency with a wide output current range.

However, the conventional PDM architecture suffers from the problem of large ripple at low output voltage region. Combining the switch matrix shown in Fig. 2 with a linear regulator may solve the problem of large ripple. However, the additional power MOSFET and opamp required for the linear regulator will consume large chip area, which is uneconomic in advanced technologies.

A novel scheme which employs both PDM and pulse width modulation (PWM) in the feed back control block is proposed to cope with this kind of problem. In the proposed scheme [10] shown in Fig. 3, a pulse width control block and a look up table (LUT) are introduced to perform pulse width modulation. Only one of the switches connected to $V_{IN}$ is necessary to be controlled by a modulated pulse signal $\phi_{PW}$, because by controlling the pulse width of this switch, the power transferred from $V_{IN}$ to the capacitors at every circle can be precisely controlled. While applying the proposed PDWM to other switch matrix, any switches connected to $V_{IN}$ should be selected for $\phi_{PW}$, in order to modulate the power transferred from $V_{IN}$. The pulse width of $\phi_{PW}$ is controlled by the pulse width control block. A 4-bit control signal is read from a LUT to determine the pulse width for $\phi_{PW}$, according to different $I_{OUT}$ and $V_{OUT}$.

The function of proposed PDWM is analyzed in Fig. 4. Figures 4(a) and (b) show the waveform of conventional method with different $V_{REF}$'s, and Figs. 4(c) and (d) show proposed method. By comparing Figs. 4(a) and (b), it is observed that lower $V_{REF}$ causes bigger ripple, because $V_{OUT}$ is charged to a $V_{IN}/2$ at every pulse of $CK_{pulse}$, because excessive power is transferred by the switch matrix. This implies that the ripple problem goes severer with the decreasing $V_{REF}$. On the other hand, as shown Figs. 4(c) and (d), proposed PDWM has a much lower ripple due to the PWM control. Because variable pulse width can be applied to drive $\phi_{PW}$, according to different $V_{REF}$'s, shown in Fig. 3, the power transferred from $V_{IN}$ is thereby under control. Therefore, $V_{OUT}$ is now charged to a lower value than in the conventional scheme shown in Figs. 4(a) and (b). Thus a significant reduction of output ripple is obtained.

Figure 5 shows the pulse width control circuit of the

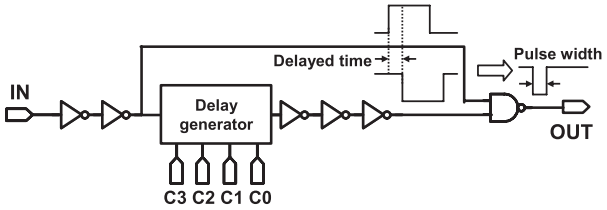



**Fig. 5** 4-bit pulse width control circuit.

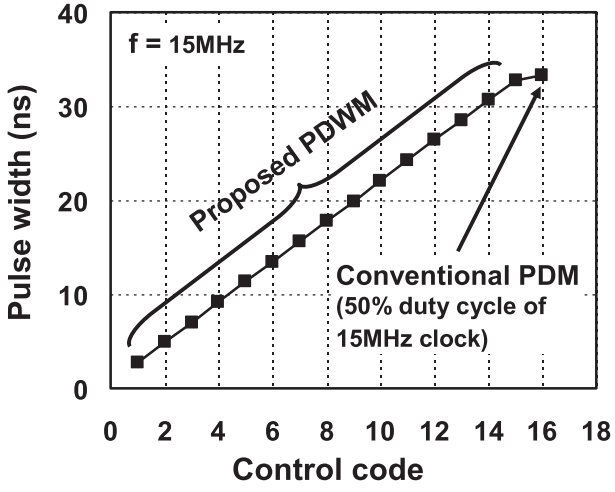



**Fig. 6** Simulated result of the 4-bit pulse width control circuit.

proposed DC-DC converter. A delay generator is employed for controllable timing delay with a 4-bit digital input signal. The input clock signal (IN) is delayed by the delay generator and then reversed by inverters. Then the reversed signal and original signal are connected to a nand gate. In this way the output signal (OUT) with controlled pulse width is obtained. Post-layout simulation results show that the pulse width control circuit generates an output with pulse width from 2.7 ns to 32.8 ns, with 2.1-ns step. Good linearity is observed, as shown in Fig. 6.

## 3. Measurement Results and Discussion

The proposed SC DC-DC converter is fabricated with 65 nm CMOS process, except for the LUT as shown in Fig. 3. Capacitors $C_1$, $C_2$, and $C_{OUT}$ shown in Fig. 3 are implemented using off-chip ceramic capacitors with values of 4.7 nF, 4.7 nF, and 47 nF, respectively. Figure 7 shows the chip micro-photograph and the layout. Multiple bonding wires are applied for power lines for less parasitic resistance. The active area of the DC-DC converter is 0.074 $mm^2$.

Figure 8 shows the measured dependence of the power efficiency on the output current at 0.47-V output voltage. The DC-DC converter delivers 0.25 mA to 10 mA output current from a 1 V input supply, with an efficiency higher than 82%, and a peak value of 87%.

Figure 9 shows the measured transient waveform of $V_{OUT}$ of both conventional and proposed DC-DC converters with 0.2-V output voltage and 1-mA output current. The

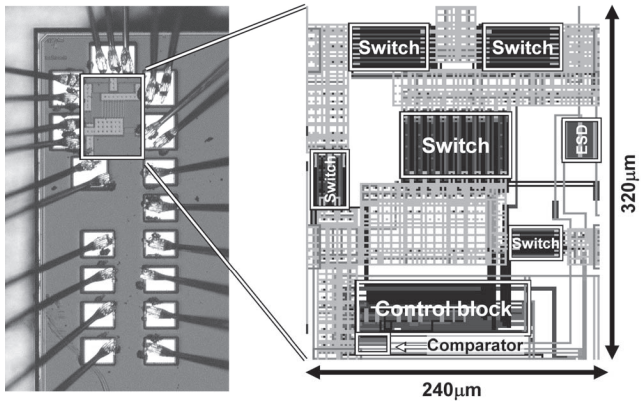



**Fig. 7** Chip microphotograph and layout.

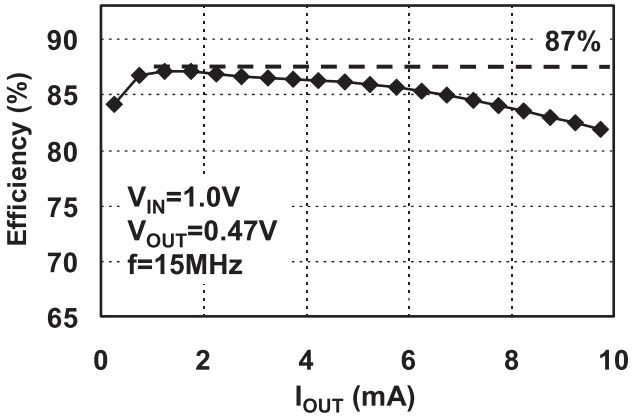
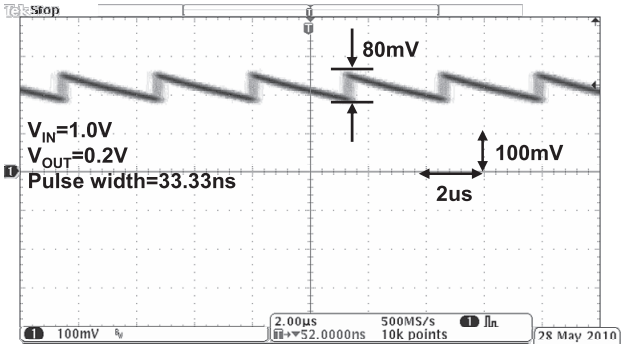
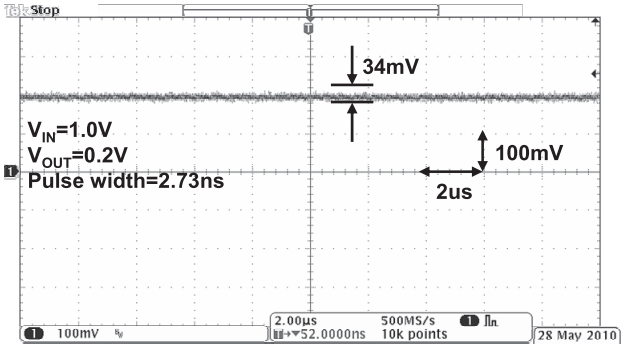



**Fig. 8** Measured efficiency vs. output current with proposed PDWM.




(a) Conventional (PDM)




(b) Proposed (PDWM)

**Fig. 9** Measured transient waveform of $V_{OUT}$ of conventional DC-DC converter and proposed DC-DC converter.

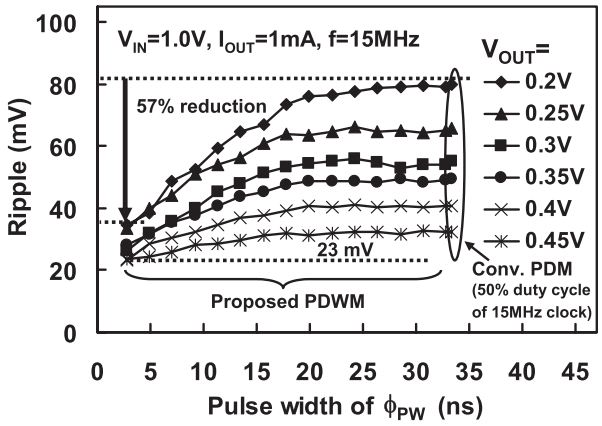



**Fig. 10** Measured ripple vs. pulse width with various $V_{OUT}$.

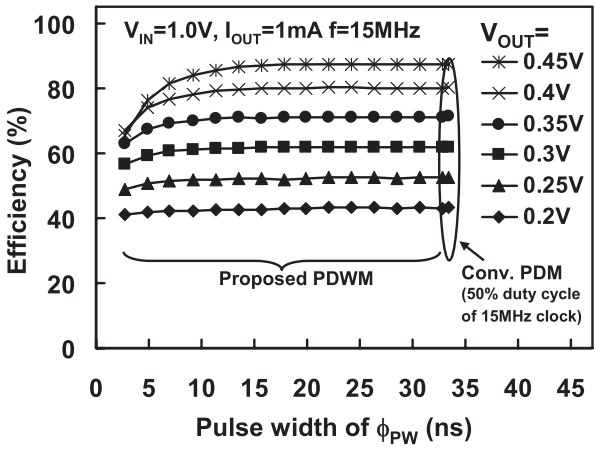



**Fig. 11** Measured efficiency vs. pulse width with various $V_{OUT}$.

pulse width of conventional DC-DC converter is 33.33 ns, as clock frequency is 15 MHz. While in the proposed DC-DC converter, the pulse width is chosen to be 2.73 ns with the same clock frequency. As analyzed in Fig. 4, in the conventional DC-DC converter, $V_{OUT}$ is charged much higher than the object voltage: 0.2 V, because excessive power is transferred by the switch matrix at every clock cycle. Therefore, an output ripple of 80 mV is observed, as shown in Fig. 9(a). In the proposed DC-DC converter, the power transferred from $V_{IN}$ by the switch matrix is under control, because pulse width is controlled by the proposed PDWM. Therefore, $V_{OUT}$ is now charged to a lower value than in the conventional scheme. Thus a low output ripple of 34 mV is obtained, as shown in Fig. 9(b).

Figure 10 shows the measured output ripple with different pulse width and different $V_{OUT}$. $V_{OUT}$ is controlled by changing $V_{REF}$. The conventional PDM with a 15 MHz clock (equals to 33.3 ns pulse width) is shown in the right of the graph. As seen, compared with the conventional PDM, the proposed PDWM greatly suppresses the output ripple, especially with low output voltages, because the pulse width of PDM is too wide for transferring required power from the switch matrix to the output. A maximum reduction of 57% on output ripple is obtained. When $V_{IN}$ changes, for example, to 1.2 V or 0.8 V, same tendency of ripple with different pulse width will be observed. The conventional PDM will have the biggest ripple and the ripple will decrease with the decreasing pulse width.

Figure 11 shows the measured efficiency with different pulse width. As seen, for each output voltage, the efficiency degrades a little with narrower pulse width. The reason is when narrow pulse width is applied, little power is transferred by the switch matrix at each clock cycle, then the pulse density will increase for transferring the required power, in this case more power is consumed by the clock driver and the switch matrix, therefore the power efficiency decreases. On the other hand, the efficiency degrades greatly with lower output voltage. That is due to the series resistance of output switches, which can be alleviated by sizing the output switches at different output voltage.

When $V_{IN}$ changes, for example, to 1.2 V or 0.8 V, same tendency of efficiency with different pulse width will be observed. When pulse width is decreasing, efficiency decreases gradually. The conventional PDM will have the highest efficiency because no PWM is performed.

By combining Fig. 10 and Fig. 11, the dependence of output ripple on power efficiency with different output current is shown in Fig. 12. As observed, the ripple is reduced by narrowing the pulse width, at the cost of slightly degraded power efficiency. That is because narrowing the pulse width also increases the pulse density, as discussed above, thus increases the power consumption. Therefore, a group of practical optimum choice on pulse width for different $I_{OUT}$ and $V_{OUT}$ was defined by allowing a 2% degradation on power efficiency, as shown in Fig. 12.

The measured optimum pulse width for different $I_{OUT}$ and $V_{OUT}$ is shown in Fig. 13. The center of each rectangle represents a measured point. As observed, 6 different optimum pulse widths are selected for different $I_{OUT}$ and $V_{OUT}$. The optimum pulse width tends to increase with increasing $I_{OUT}$ and $V_{OUT}$, because there is a larger need of power to be transferred by the switch matrix, thus there is a demand for wider pulse on the switch. The selected pulse width information is then stored in the LUT. Therefore, users of the proposed SC DC-DC converter can choose the optimum pulse width based on Fig. 13 for the required $I_{OUT}$ and $V_{OUT}$. For example, with the required $I_{OUT}$ of 5.5 mA and $V_{OUT}$ of 0.41 V, a pulse width of 9.2 ns is the optimum solution. For the required $I_{OUT}$ and $V_{OUT}$ which lie on the crossings of the squares shown in Fig. 13, any value of neighbored square could be applied for the optimum solution. In this way, the SC DC-DC converter will be configured to the optimum pulse width for the optimum output ripple and power efficiency.

Further measurement would be carried out to expand the contour shown in Fig. 13. For example, in the current contour, the optimum pulse width does not change when $I_{OUT}$ is larger than 1.5 mA. If more measurement as shown in Fig. 12 would be carried out for $I_{OUT}$ larger than 10 mA, the

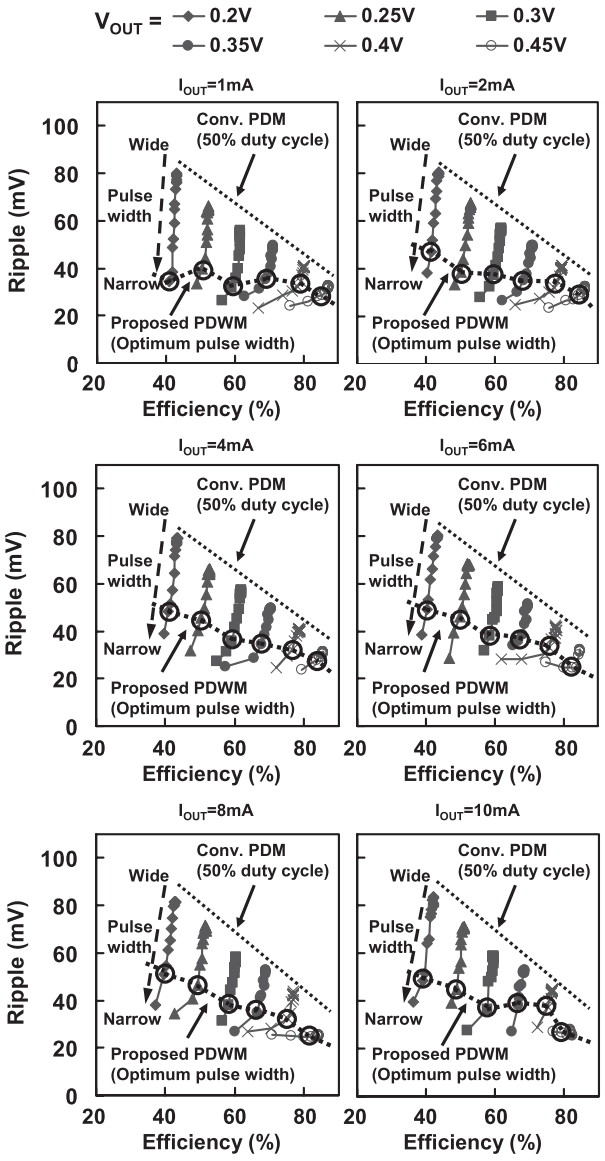



**Fig. 12** Measured ripple vs. power efficiency with various $V_{OUT}$ and $I_{OUT}$, at $V_{IN}$=1.0 V.

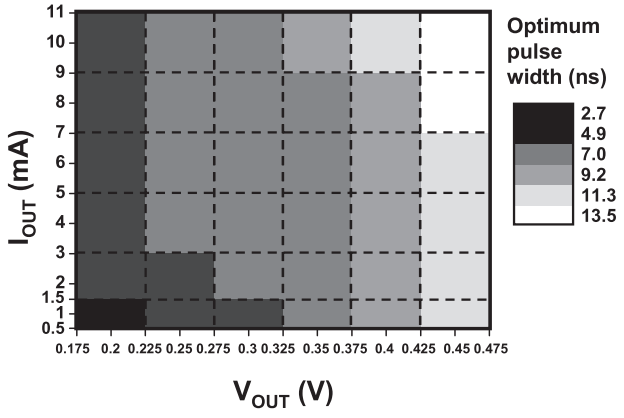



**Fig. 13** Contour of optimum pulse width with regarding to $I_{OUT}$ and $V_{OUT}$, at $V_{IN}$=1.0 V.

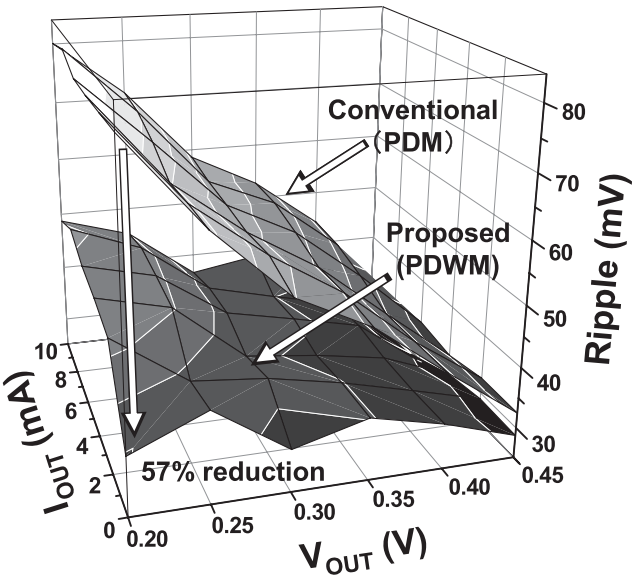



**Fig. 14** Measured ripple of conventional and proposed DC-DC converters with regarding to $I_{OUT}$ and $V_{OUT}$, at $V_{IN}$=1.0 V.

**Table 1** Performance summary of the proposed PDWM SC DC-DC converter.

| | |
|---|---|
| Process | 1.2V 65-nm CMOS |
| Active area | 0.074 $mm^2$ |
| Clock frequency | 15MHz |
| Input voltage | 1.0V |
| Output voltage | 0.2~0.48V |
| Output current | 0.25~10mA |
| Max efficiency | 87% |
| Min output ripple | 23mV |

range of Y-axis of Fig. 13 will be extend and dependence of optimum pulse width on $I_{OUT}$ will be observed. In addition, if more measurement as shown in Fig. 12 would be carried out for more different $V_{OUT}$'s, the resolution of X-axis of Fig. 13 will increase.

In the future, the current sensor [11] and the LUT would be integrated with the proposed PDWM DC-DC converter, and then the optimum pulse width will be automatically selected according to different $I_{OUT}$ and $V_{OUT}$. The switch matrix shown in Fig. 3 would be improved to include other topologies like 1/3, 2/3, etc., to further improve the power efficiency of the proposed PDWM DC-DC converter at different output voltage.

Figure 14 shows the measured output ripple of conventional and proposed PDWM DC-DC converters with regarding to $I_{OUT}$ and $V_{OUT}$. Significant reduction of the output ripple is observed in the whole range of $I_{OUT}$ and $V_{OUT}$. Moreover, the output ripple is more effectively reduced in low output voltage region (to a peak of 57%). Recall that ripple has a larger impact on digital circuits at a lower voltage, the proposed DC-DC converter provides a promising

solution for sub-threshold digital circuits. The performance the proposed PDWM SC DC-DC converter is summarized in Table 1.

## 4. Conclusion

A switched-capacitor (SC) DC-DC converter with novel PDWM control scheme for high power efficiency and low output ripple is proposed. Compared with the conventional PDM, significant reduction of the output ripple is achieved by the proposed SC DC-DC converter with PDWM in the whole range of $I_{OUT}$ and $V_{OUT}$. A maximum reduction of 57% on the output ripple is observed with 0.2-V output voltage. The proposed converter is fabricated using 65 nm CMOS process with an active area of 0.074 $mm^2$. A control scheme using both PDM and PWM is introduced to enable a high efficiency with wide output current range, and meanwhile suppress the output ripple with low output voltage. The proposed SC DC-DC converter works on a 1-V input supply, and generates 0.2-V to 0.47-V output voltage. It achieves an efficiency above 82% in output current range of 0.25-mA to 10-mA, with a peak value of 87%. With the low ripple, high efficiency and low output voltage, the proposed PDWM SC DC-DC converter shows a promising solution for sub-threshold digital circuits.

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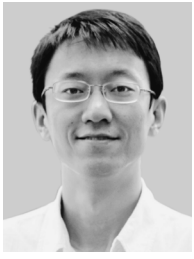

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