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0.6 V Voltage Shifter and Clocked Comparator for Sampling Correlation-Based Impulse Radio UWB Receiver

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SUMMARY A 0.6-V voltage shifter and a 0.6-V clocked comparator are presented for sampling correlation-based impulse radio UWB receiver. The voltage shifter is used for a novel split swing level scheme-based CMOS transmission gate which can reduce the power consumption by four times. Compared to the conventional voltage shifter, the proposed voltage shifter can reduce the required capacitance area by half and eliminate the non-overlapping complementary clock generator. The proposed 0.6-V clocked comparator can operate at 100-MHz clock with the voltage shifter. To reduce the power consumption of the conventional continuous-time comparator based synchronization control unit, a novel clocked-comparator based control unit is presented, thereby achieving the lowest energy consumption of 3.9 pJ/bit in the correlation-based UWB receiver with the 0.5 ns timing step for data synchronization.

key words: *impulse radio ultra-wideband (IR-UWB), voltage shifter, clocked comparator, low voltage*

1. Introduction

The market and the need to develop efficient electronic equipment have pushed the industry to design circuits with very low power supply voltage, and also often constrained to low power consumption. This work targets to develop a 0.6 V voltage shifter and a 0.6 V clocked comparator for the multi-phase sampling application, such as correlation-based ultra-wideband (UWB) receiver or analog-to-digital converter (ADC). As an application example, the proposed voltage shifter and the clocked comparator are used for the impulse radio UWB receiver.

Impulse radio UWB refers to a radio technology for transmitting information by means of extremely short duration pulses without radio frequency modulation. Ideal targets for IR-UWB system are low power, low cost, high data rates, and extremely low interference, which makes it an attractive option for ad hoc and sensor network where groups of wireless terminals are located in a limited area and communicate in an infrastructure-free fashion without any central coordinating unit or base-station.

Conventional impulse UWB transceivers usually require 1.2 V supply voltage or above [1]–[3]. However, in the single solar cell powered ad hoc and sensor network, the maximum available supply voltage is less than 0.6 V. To make the existing circuits to operate at 0.6 V supply voltage, a 0.6 V to 1.2 V DC-DC converter is often used. To reduce the DC-DC converter output power in this work, a 0.6 V voltage shifter and a 0.6 V clocked comparator are proposed for the correlation-based IR-UWB receiver [4]. Figure 1 shows block diagram of the proposed receiver. To verify the performance of the 0.6 V voltage shifter and the 0.6 V comparator, a novel synchronization control unit is also implemented in the same chip with the sampling clock generator. 1.2 V supply voltage for the synchronization control unit and the sampling clock generator are provided by a 0.6 V to 1.2 V DC-DC converter. The DC-DC converter is not implemented in this work.

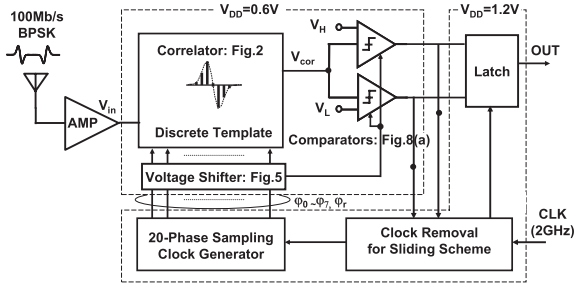

Fig. 1 Block diagram of impulse radio UWB receiver. 0.6-V voltage shifter supplies boosted voltage to charge-domain correlator and comparator.

Section 2 shows the switching driving problem in the conventional charge-domain sampling correlator. Section 3 presents the circuit implementations of the voltage shifter. The 0.6 V voltage comparator is described in Sect. 4 and synchronization scheme is described in Sect. 5. Experimental results are presented in Sect. 6 and Sect. 7 concludes the paper.

2. Split Swing Level Scheme for CMOS Transmission Gates

Figure 2 shows the circuit schematic of the charge-domain sampling correlator used in the UWB receiver [2]. Correlation operation is achieved in two steps. First the switches controlled by clocks $\phi_1, \phi_2 \ldots \phi_7$ are turned on sequentially and the incoming signal is sampled and stored to the corresponding capacitors respectively, then the stored voltages are weighted summed and averaged by turning on all the ϕ_r controlled switches. After summing and averaging, the correlator output is reset to 0.6 V by clock ($\overline{\phi_r}$).

The sampling correlator circuits make use of two basic building blocks, namely the capacitor and the switch. Lowering the supply voltage of the correlator has implications

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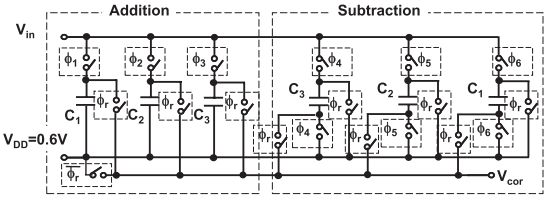


Fig. 2 Charge-domain sampling correlator.

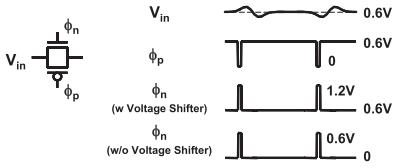


Fig. 3 Split swing level scheme for CMOS transmission gate.

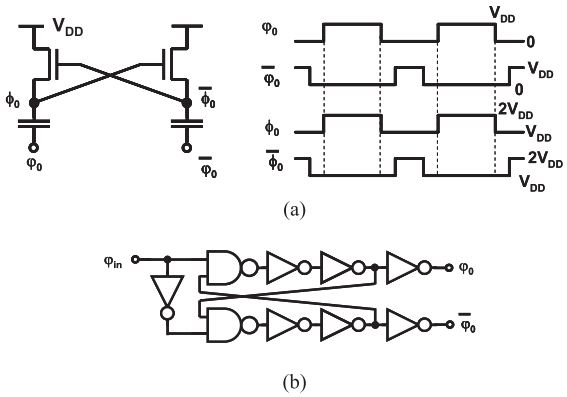


Fig. 4 Conventional voltage shifter [6]. (a) Circuit schematic and waveforms. (b) Non-overlapping complementary clock generator (© 2010 IEEE).

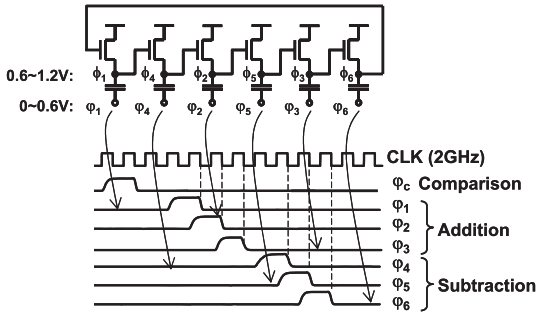


Fig. 5 Simplified circuit schematic of the proposed voltage shifter for the sampling correlator (© 2010 IEEE).

on the operation of some building blocks. The functional property of a capacitor, namely its capacitance, is in fact independent of the supply voltage. The most problematic issue in low voltage sampling correlator design is the switch driving problem. One effective way to cope with the low supply is to apply voltage shifting. This technique uses circuits which convert the voltage from the available supply to another one.

Figure 3 shows the proposed split swing level scheme-based CMOS transmission gate. The DC level of the incoming signal is 0.6 V and the peak-to-peak voltage is around 40 mV. Because the thresholds of NMOS and PMOS are higher than 0.4 V, the 0~0.6 V inputs are used to drive the PMOS and the 0.6~1.2 V outputs of the voltage shifters are directly used to drive the NMOS without converting to 0~1.2 V full swing level. This split swing level scheme can reduce the power consumption of the CMOS transmission gates by four times due to the $P \propto CV^2$ relationship.

3. Voltage Shifter

3.1 Conventional Voltage Shifter

Various circuits have been proposed and used in literature to implement voltage boost. Originally monolithic boosted voltage generators stem from non-volatile memory circuits where a relatively high potential is needed to write or erase information [5]. A conventional voltage booster from DRAM applications is found in [6] and shown in Fig. 4(a). The key feature of this voltage booster is to use feedback technique to obtain a boosted voltage of $2V_{DD}$ even at low operating voltage. When one clock is high, the bootstrapped voltage is high enough to turn on the other NMOS, which charges the other capacitor to V_{DD}. In the next phase the roles are exchanged. This feedback technique can eliminate a voltage loss due to a threshold voltage of MOSFET.

The required clock signals used in the conventional voltage booster can be generated by the non-overlapping complementary clock generator show in Fig. 4(b). This circuit takes a clock signal and generates a two-phase non-overlapping clock. The amount of separation is set by the delay through the NAND gate and the two inverters on the NAND gate output. When driving a large capacitance, where the rise time of the signals can be significant, a large number of inverters are required as part of the delay which will dominate the power consumption of the voltage booster.

3.2 Proposed Voltage Shifter

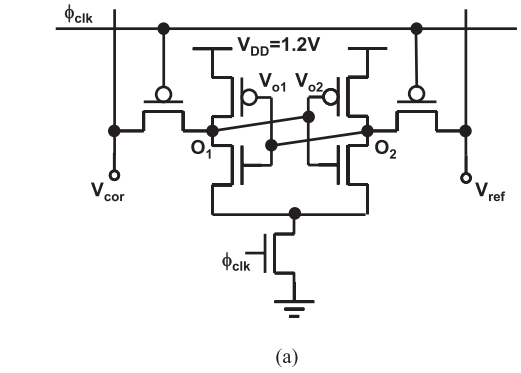
In the sampling correlator, the complementary clock signals are not required. If the conventional voltage boosters are directly used to generate the 20-phase sampling clocks for the correlator in Fig. 1, half of chip area and power dissipation of the voltage shifters will be wasted due to the complementary clock signals. To overcome this problem, the proposed voltage shifter for the multi-phase sampling correlator is shown in Fig. 5. The non-overlapping requirement on the adjacent input signals can be satisfied by swapping the clocks $\varphi_1, \varphi_2, \varphi_3, \varphi_4, \varphi_5, \varphi_6$ to $\varphi_1, \varphi_4, \varphi_2, \varphi_5, \varphi_3, \varphi_6$ thus eliminating the non-overlapping complementary clock generator. When driving a large capacitance, power consumption of the voltage shifter will be increased but the numbers of the required transistors and the control clocks are reduced by half and thus the power consumption can be also reduced by half. The voltage shifter outputs $\phi_1, \phi_2 \ldots \phi_6$ are used to drive the switches in Fig. 2 correspondingly.

4. Clocked Comparator

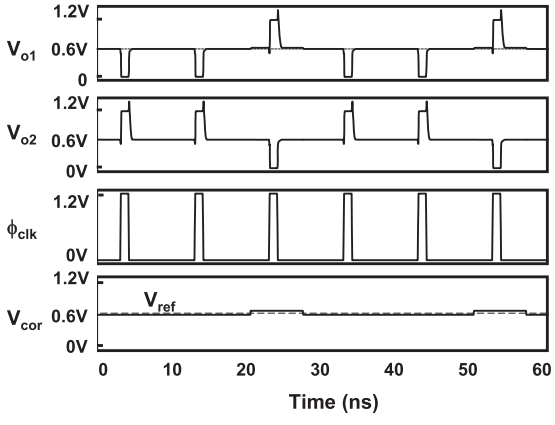
Comparators are used for synchronization control and data decision in the proposed UWB receiver as shown in Fig. 1. For 0.6-V supply voltage, it doesn't suffice to force an existing circuit to operate at 100-MHz clock. It requires the development of dedicated circuits.

4.1 Conventional Clocked Comparator

Figure 6 shows the circuit schematic and the simulated waveforms of the conventional clocked comparator [7] at 1.2-V power supply voltage. The reset is done to the metastable state and the regeneration is satisfied by two MOS inverters in positive feedback configuration. When clock is low, the drains of the two inverters (O_1, O_2) are charged to V_{cor} or V_{ref} (creating an imbalance). When clock goes high, the imbalance causes the circuit latch high or low depending on the state of the inputs. This comparator doesn't consume DC power in reset mode but it fails to operate at 100 MHz clock when the supply voltage is reduced to 0.6 V.



(a)



(b)

Fig. 6 Conventional clocked comparator [7]. (a) Circuit schematic. (b) Waveforms. (© 2010 IEEE)

4.2 Proposed Clocked Comparator

To make the conventional clocked comparator operate at 100 MHz with 0.6 V supply voltage, in the proposed comparator, supply voltage is doubled from 0.6 V to 1.2 V when clock goes high. Figure 7 shows the complete circuit schematic of the proposed voltage shifter for both the sampling correlator and the clocked comparator where ϕ_1, $\phi_2, \ldots, \phi_6$ are used for the sampling clock of the correlator and ϕ_{cmp} is used for the supply voltage of the comparator. Figure 8 shows the circuit schematic and the simulated waveforms of the proposed comparator. The proposed clocked comparator operates with 100-MHz clock at a 0.6-V power supply voltage. When ϕ_{clk} is low, the circuit outputs

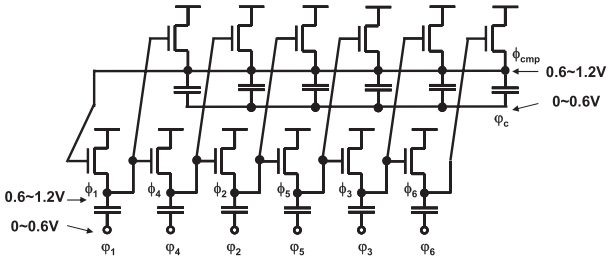
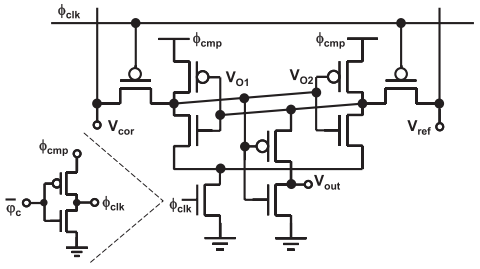
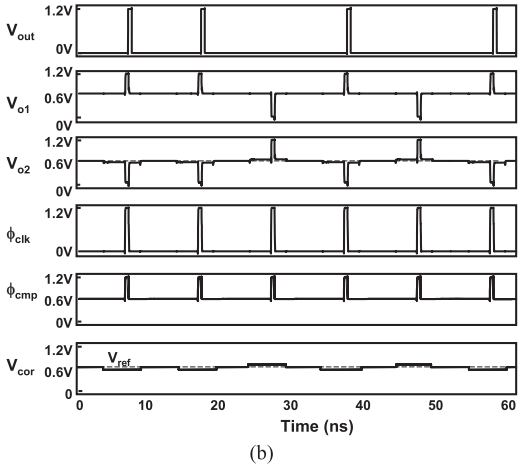


Fig. 7 Complete circuit schematic of the proposed voltage shifter for both the sampling correlator and the clocked comparator. (© 2010 IEEE)



(a)



(b)

Fig. 8 Proposed clocked comparator. (a) Circuit schematic. (b) Waveforms. (© 2010 IEEE)

are not valid logic signals but rather, ideally, track the input signals. This form of the latch has the advantage of lower power dissipation because no current is flowing when the latch is in reset mode.

5. Synchronization Scheme

1.2 V Supply voltage for the synchronization control unit is provided by a 0.6 V to 1.2 V DC-DC converter. One of the advantages of the proposed clocked comparator is that the output swings from 0 to 1.2 V which can be used for the synchronization control unit directly without additional level shifter. The operation principle of the sliding scheme for data synchronization is shown in Fig. 9(a). Before synchronization is achieved, the incoming signal lags the template of the correlator by ΔT. Sliding scheme can slide the timing error ΔT towards zero at the step of 0.5 ns. Conventionally the control unit for sliding scheme is implemented by tapped delay-lines [8]. However, the delay-lines not only consume additional power but also have uncertainty due to the variation of process, voltage, and temperature across large dies. In the proposed discrete-time receiver, the sliding control unit can be embedded to the charge-domain correlator seamlessly by utilizing the 2 GHz clock for the sampling correlator.

To reduce the power consumption of the continuous-time comparator based sliding control unit in [2], a novel clocked-comparator based control unit is proposed in Fig. 9(b). The continuous-time comparator in [2] always consumes power when signals come while the clocked comparator doesn't consume power in reset mode and thus power consumption can be reduced. This control unit is implemented by preprocessing the clock signal CLK. The gated inverter which drives the divide-by-five frequency divider is transparent to "0" but not transparent to "1". When the timing mismatch ΔT between the incoming signal and the template of the correlator is larger than 0.5 ns, the auto-correlation result V_{cor} is lower than the threshold of the following comparators. In this case, both UP and DN are generated and thus the clock removal signal RM is generated. This clock removal pulse will block the propagation of the input clock by one period. With the one-period delay, the phase of the sampling clock slides by 0.5 ns and the period of the sampling clock is increased from 10 ns to 10.5 ns. When the timing mismatch ΔT between the incoming signal and the template of the correlator is less than 0.5 ns, the auto-correlation result V_{cor} is large enough to be detected by the comparators. In this case, either UP or DN is generated and RM is not generated, which keeps the period of the sampling clock 10 ns. The 20-phase sampling clock is generated by combining the output edges of the divide-by-5 divider and the divide-by-4 divider.

Figure 10 shows the timing chart of the whole synchronization process. In the worst case the data synchronization can be finished within 19 phase slides because the period of input signal is 10 ns and differs with the period of the sampling clock by 0.5 ns. Before synchronization is achieved, there is no output in the receiver and thus it cannot be used for data communication. After the synchronization is achieved, the sampling clock period returns to 10 ns and it can be used for communication.

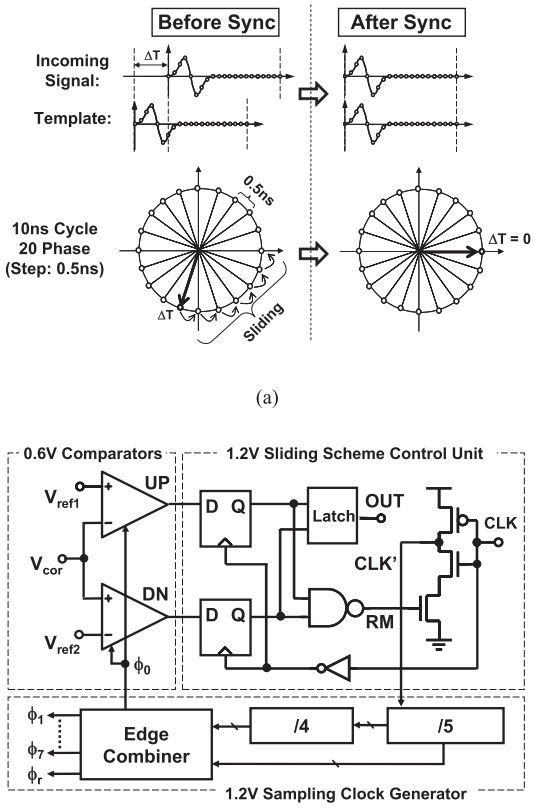


Fig. 9 Sliding scheme for data synchronization. (a) Operation principle. (b) Circuit implementation.

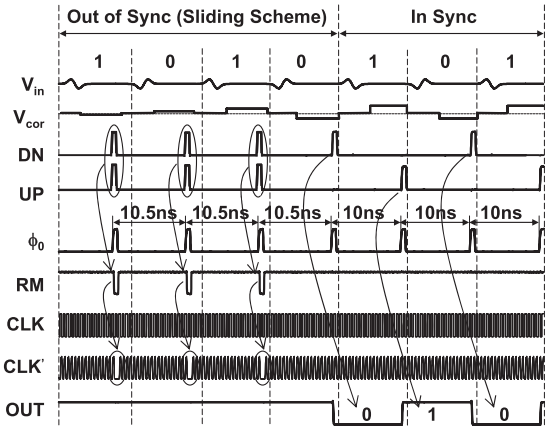


Fig. 10 Timing chart of sliding scheme for data synchronization.

6. Measurement Results

The proposed UWB receiver without the front-end amplifier was designed and fabricated in 1.2 V 65 nm CMOS process.

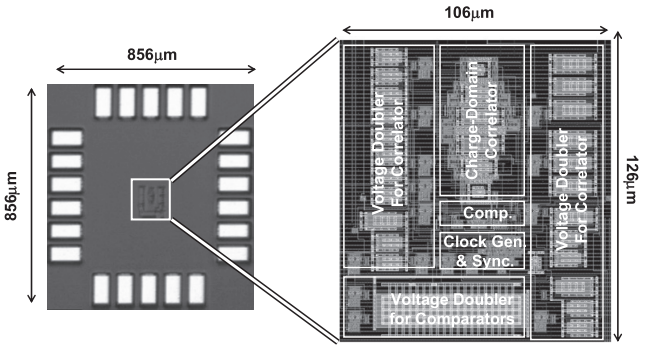


Fig. 11 Chip micrograph and layout of UWB receiver. (© 2010 IEEE)

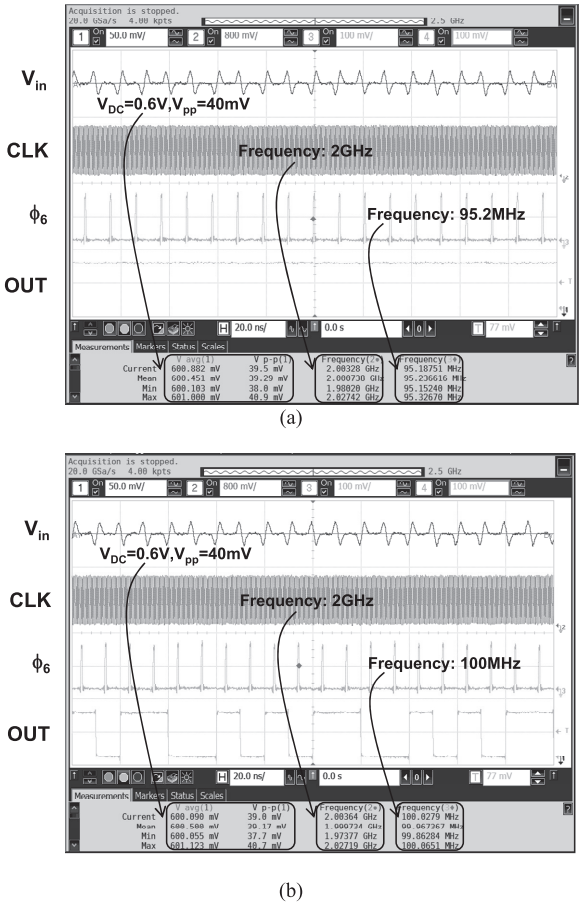


Fig. 12 Measurement results of UWB receiver. (a) Sliding scheme for timing alignment. (b) Measured waveforms in synchronization. (© 2010 IEEE)

The chip micrograph and layout are shown in Fig. 11. To verify the performance of the proposed 0.6 V voltage shifter and the 0.6 V clocked comparator, the 1.2 V level outputs of the clock generator are down-shifted to 0.6 V for the input in Fig. 1. Figure 12(a) shows the measured waveforms before synchronization is achieved, where V_{in} is the incoming UWB pulse, CLK is the 2 GHz input clock, ϕ_6 is the sixth sampling clock and OUT is the output data. Before synchronization is achieved, due to the clock-swallow sliding scheme, for every incoming UWB pulse one input clock is swallowed and the period of the sampling clock generator output is increased to 10.5 ns which corresponds to the frequency 95.2 MHz. Figure 12(b) shows the measured waveforms when synchronization is achieved. Because the sliding scheme for timing alignment is inactivated, the frequency of the sampling clock returns to 100 MHz and the UWB receiver receives 100-Mbps data correctly.

Table 1 Performance summary. (w/o front-end amp.)

		[2]	This Work
CMOS Technology		180nm	65nm
Supply Voltage		1.8V	0.6V,1.2V
Data Rate		100Mb/s	100Mb/s
Clock Frequency		2GHz	2GHz
Power	Correlator & Comparators	0.75mW @1.8V	0.05mW @0.6V
	Clock Gen. & Sync Control	0.53mW @1.8V	0.34mW @1.2V
	Total	1.28mW	0.39mW
Energy per bit		12.8pJ/bit	3.9pJ/bit
Core Area		5561 μm² (w/o Volt. Doubler)	13356 μm² (with Volt. Doubler)

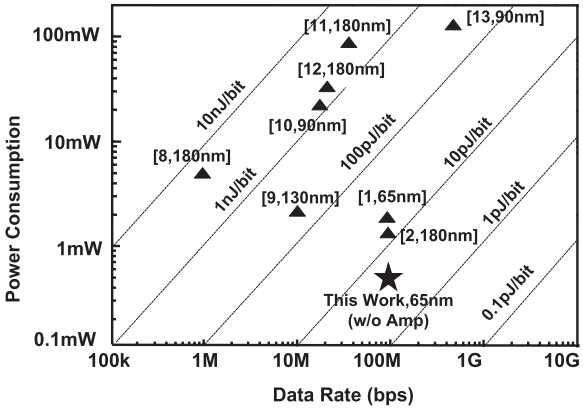


Fig. 13 Comparison with state-of-the-art correlation-based UWB receivers. (Reference and CMOS process technology are shown. [1], [2] are without front-end amp. [8]–[13] are with front-end amp.)

The receiver performance is summarized in Table 1. Compared to the conventional 1.8 V UWB receiver [2], the total power consumption is reduced from 1.28 mW to 0.39 mW where 0.72 mW power reduction is caused by process technology and 0.17 mW power reduction is caused by circuit topology. The power consumption of the correlator and the comparators is reduced by 93% (from 0.75 mW to 0.05 mW) by reducing the power supply voltage from 1.8 V to 0.6 V. The performance comparison with the state-of-the-art correlation-based IR-UWB receivers is shown in Fig. 13. The proposed UWB receiver with the 0.6-V voltage shifter and the 0.6-V clocked comparator achieves the lowest energy consumption of 3.9 pJ/bit in the correlation-based IR-UWB receivers with the 0.5 ns timing step for data synchronization.

7. Conclusions

This paper presents a 0.6-V voltage shifter and a 0.6-V

clocked comparator in 65 nm CMOS. For the multi-phase sampling application, such as charge-domain correlator for impulse UWB receivers or analog-to-digital converter, the proposed voltage shifter can reduce the power consumption and the chip area by half compared to the conventional one. The non-overlapping complementary clock generator used in the conventional voltage shifter can be eliminated by simply swapping the input clock order in the voltage shifter. The proposed 0.6-V clocked comparator can operate at 100-MHz clock with the proposed voltage shifter. Compared to the conventional 1.8 V UWB receiver [2], the power consumption of the correlator and the comparators is reduced by 93% by reducing the power supply voltage from 1.8 V to 0.6 V.

Acknowledgments

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