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1 Gb/s, 50 μm × 50 μm Pads on Board Wireless Connector Based on Track-and-Charge Scheme Allowing Contacted Signaling

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SUMMARY A capacitive coupling wireless connector circuit is implemented with 50 μm × 50 μm pads, which is a 25X reduction of pad size compared with previous wireless connectors by allowing contacting and non-contacting modes. The proposed track and charge scheme allows both contacting and non-contacting communication through PCB capacitive pads. By making the precharge level of the input V_{DD} or V_{SS}, instead of $1/2\,V_{DD}$, the time necessary to precharge is reduced. The proposed digitally tunable comparator does not require analog voltages, reduces the power to less than 1/20 at lower frequencies compared to previous capacitive coupling receivers. A test chip successfully transmitted and received 1 Gb/s, $2^7 - 1$PRBS signal at 1 mW while increasing design freedom of the wireless connectors.

key words: *capacitive coupling, proximity communication, wireless connectors*

1. Introduction

Wireless connectors are a promising means of connecting highly parallel channel between two boards with small feature sizes. They provide a means to overcome some of the shortcomings of conventional mechanical connectors by increasing pin density, reducing height, reducing insertion force and providing higher reliability [1]. In a wireless connector, the proximity coupling of two terminals is made by a flexible Printed Circuit Board (PCB) as is shown in Fig. 1, where small pressure is generated by natural bending of the flexible PCB. For this application, a capacitive coupling approach has advantages over inductive coupling counterpart [2] since a coil pattern for the inductive coupling on a PCB consumes more than 10 times the area of a simple square pad area needed for the capacitive coupling assuming the same line and space design specifications on the PCB. The clearance rules of through-hole vias on PCBs hider the use of them for the interface. The schematic diagram of a generic capacitive coupling interface is shown in Fig. 2. When the output of the TX swings rail-to-rail, the signal swing at the receiver side, RX_{IN}, is expressed as $V_{DD}C_C/(C_{PR} + C_C)$, where C_C is the coupling capacitance of the coupling pads and C_{PR} is the parasitic capacitance on the RX side. C_{PR} includes capacitances of the wiring on PCB, bonding wires, bonding pads and ESD structure of the chip which amounts to 2 pF which is about two orders of magnitude higher than on-chip node capacitance. Thus the wireless connector must handle smaller input signals compared to chip to chip capacitive coupling interfaces [3], [4]. To cope with the small received signal the wireless connector previously reported [1] sacrificed density of the capacitive pads and used 250 μm × 250 μm to get a large enough C_C.

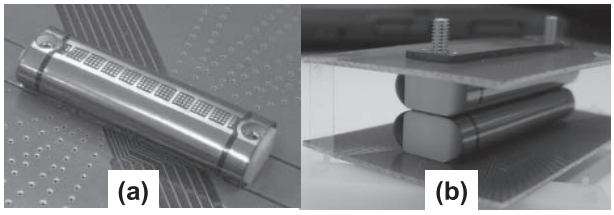

Fig. 1 Examples of wireless connectors (a) showing capacitive coupling pads and (b) in closed circuit configuration. (Structure applicable but not used in this work)

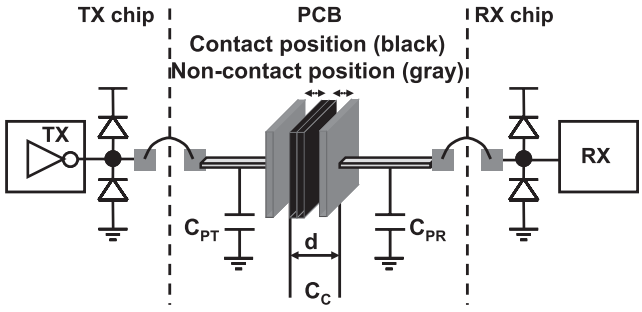

Fig. 2 A generic capacitive coupling connector circuit.

2. Design Considerations for Wireless Connectors

High density, high reliability, ease of manufacturing should be some of the key points in making a connector. To meet those goals, two major design considerations were made between mechanical connector and wireless connectors, and inductive coupling and capacitive coupling.

2.1 Mechanical Connectors vs. Wireless Connectors

To attain a stable connection, mechanical connectors must scrape off residue and oxides on the surface of the connec-

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Table 1 Mechanical connectors and wireless connectors.

	Conventional (mechanical)	Non-contacting
Pressure/pin	20gf	~0gf
Height	0.6mm	~0.1mm
Pin density	1pin/mm^2	10pins/mm^2
Reliability	△	○
Water proof	×	○

tor pins, and apply close to 20 gf of pressure to maintain low resistance and stability. They are facing many problems for applying this pressure. The complex spring mechanism implemented in each pin for low profile connectors reduces the number of times the connector can be detached to as few as 5 times. To reduce the force needed to attach/detach a connector with many pins, Zero Insertion Force (ZIF) connectors which hold and release the connector pins with a lever were developed, which however has large feature sizes so cannot be used in area critical applications.

Wireless connectors on the other hand, do not need pressure to reduce resistance nor do they need scraping mechanisms since they can communicate through the natural oxides or residue, thus simplifying the structure of the connector. They could reduce footprint as well as faulty connections. The capacitive coupling technique used here will also be useful in implementing connectors have large number of pins. In a case where 10,000 pins are necessary and 20 gf of pressure is needed for a stable mechanical connection, 200 kgf is needed to press the connector, while in the case of wireless connectors, there is no need to put pressure on the pins.

Table 1 compares some of the strengths and weaknesses of mechanical and wireless connectors.

2.2 Inductive Connectors vs. Capacitive Connectors

For non-contacting chip to chip communication, there are two main approaches, using capacitive coupling and using inductive coupling. When implementing connectors on PCBs, the inductor or capacitor must be drawn on the PCB. Common technology for PCBs is 125 μm line and space, so using inductors drawn on PCBs will require more area per pin compared to capacitively coupled connectors. Wireless connectors using inductors have been published which utilize inductors drawn on-chip, presumably because of the smaller design rules and lower parasitic inductance and capacitance. This approach requires careful alignment of the TX chip and RX chip so that they are on top of each other. This will require new packaging technologies for aligning the chip and the board with very high precision. On the other hand, if the connectors are implemented using the PCB boards, traditional wire bonding, BGA, or packaging can be used making it easier to use. Therefore, capacitively coupled technology using the pads drawn on PCBs was chosen over inductively coupled communication for wireless connectors.

The wireless connector demonstrated here, and previously reported capacitively coupled chip to chip communication circuits share similar topologies but are completely different in that for the connector, the parasitic capacitance is very large (500 fF~1 pF) and differ between pin to pin because of parasitic capacitance on PCB boards which may vary according to the pattern on the PCB, and I/O diodes on the receiver chip which are excluded in chip to chip communication.

3. Contact Allowing Wireless Connector

As shown in the previous section, the input swing that comes through the capacitive pads is $V_{DD}C_C/(C_{PR}+C_C)$. To reduce the size of capacitive pads while keeping the same input swing, you would need to either increase V_{DD}, reduce C_{PR}, or keep the C_C constant. Since V_{DD} is limited by the process and/or power dissipation of TX, it is difficult to change. The parasitic capacitance C_{PR} strongly correlates to the length of the wires from the capacitive pads to the input of the RX chip, so reducing C_{PR} will reduce the flexibility of the design of the wireless connector. It is therefore needed to keep the coupling capacitance C_C constant while reducing the pad size. Since C_C can be expressed as $C_C = \varepsilon_0\varepsilon S/d$ where ε is the dielectric constant of the insulator, S is the area of the pads, and d is the distance between the two pads, to keep C_C constant when S becomes smaller, d must be reduced. Conventionally, d is determined by the thickness of the insulating overcoat of the pads, which is difficult to control precisely and is more than 40 μm. This paper proposes to totally remove the insulating overcoat to reduce d to eventually zero. Then, the pad metal, normally Au or Cu (Au in this paper), can be in a fully contacting mode. There may be cases, however, that thin insulating layers exist between two pads made by oil, air-gap, or natural oxide. Thus, two cases have to be considered: a contacting case and a non-contacting case. Since there is a non-contacting case, the transceiver should be based on C-coupling interface circuit. In the conventional receiver, RX_{IN} is precharged to 1/2 V_{DD} this causes a problem when the pads get contacted. The transmitter tries to output V_{SS} or V_{DD} which contends with the 1/2 V_{DD} precharger at the RX side resulting in the increase of DC power. This problem is addressed by the proposed track and charge scheme. This track and charge scheme has two major features. The first is that it allows the TX outputs and RX inputs to be short circuited without having leakage issues, and the second is that since the precharge voltages are V_{DD} and V_{SS} instead of the normal 1/2 V_{DD} it precharges faster, increasing data rate, and also eliminates the need for a 1/2 V_{DD} generator which dissipates DC power.

The digitally tunable comparator proposed here is a current latch comparator with digital tunability. This tunability is fully used so that no analog DC reference voltage

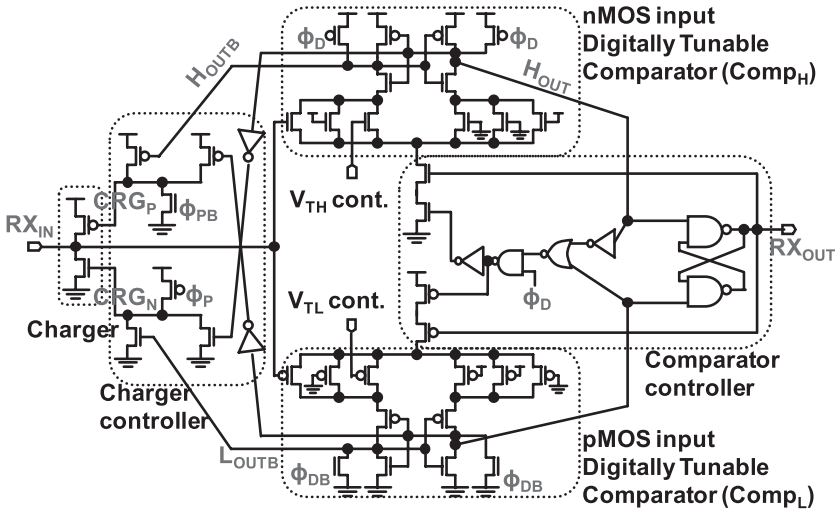

Fig. 3 Receiver circuit schematic of contact allowing wireless connector.

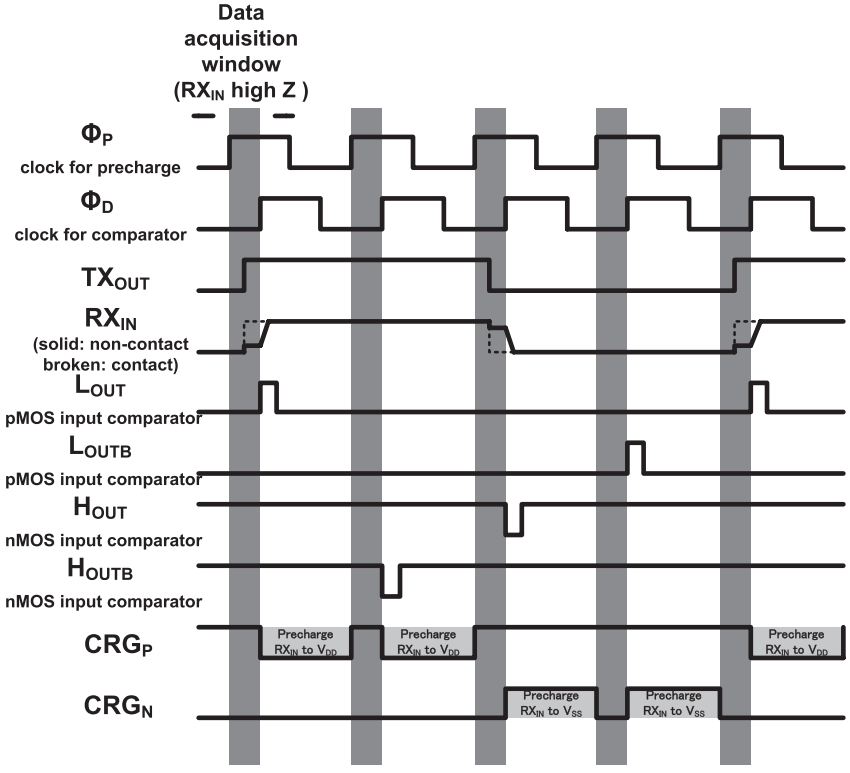

Fig. 4 Detailed timing charts of wireless connector.

will be needed in detecting either a high signal or a low signal, thus making this circuit completely DC free, which will reduce the power dissipation at lower bit rates, and when the channel is idle or is working at low data rates.

The overall circuit diagram of the receiver circuit of the proposed wireless connector is shown in Fig. 3 and the operation timing chart is shown in Fig. 4. The prominent circuit elements are explained in the following sections.

4. Track and Charge Scheme Receiver

Figure 5 describes the concept of the proposed 'track-and-charge' scheme to allow the contacting case without increasing DC power. Tracking the incoming data, RX_{IN} is charged to either V_{SS} or V_{DD}. By selectively charging RX_{IN} in accordance with the TX_{OUT} level, the contention between RX and TX is removed eliminating the DC current path which existed in the conventional transceiver. To implement the

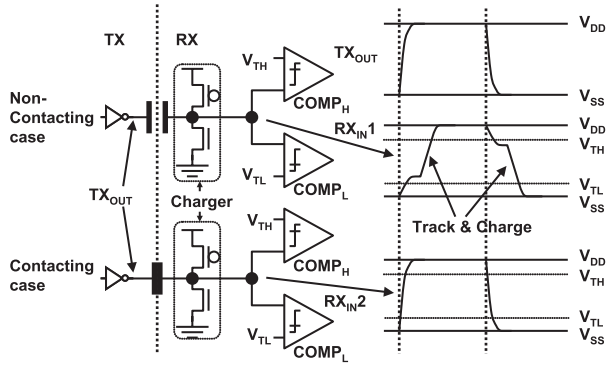

Fig. 5 Conceptual drawing of proposed contact allowable track and charge scheme.

scheme, two comparators are connected to RX_{IN}. One comparator, $COMP_H$, has a logic threshold of V_{TH} which is close to V_{DD}, to detect '0' and the other comparator, $COMP_L$ has a threshold of V_{TL} which is close to V_{SS}, to detect '1'. If the previous data is '1', RX_{IN} is charged to V_{DD} and the '0' detecting comparator, $COMP_H$, is enabled. The circuit diagram of the overall receiver is shown in Fig. 3 together with an operation timing chart in Fig. 4.

Although V_{TH} and V_{TL} are set somewhere in between the V_{SS} and V_{DD}, offset-adjustable comparators are used to eliminate the DC power in generating the intermediate voltages. Since there is no DC path, the power is proportional to data rate. The design is based on synchronous clocking. The clock itself is sent using the conventional RX with a capacitor just in front of the RX. Thus, for the clock signal transmission, there is a half V_{DD} generator but since there is only one channel, the power overhead for the clock itself is minimal compared with the power consumption of multiple data channels.

In previous capacitive coupling receivers, the input of the receiver is precharged to 1/2 V_{DD}. At this voltage, the source voltage of the charger becomes closer to the gate voltage and the gate overdrive becomes lower. This 'track and charge' scheme, however precharges RX_{IN} to V_{DD} or V_{SS} so the gate overdrive is V_{DD} which reduces the time to precharge the input of the receiver. This increases the data rate.

5. Digitally Tunable Comparator

The comparator circuit used here is shown in Fig. 6. The pull-down transistors M1-3 are in the saturation region where the velocity saturation limits the transconductance to the following.

$$g_m = -V_{SAT} W C_{OX} \tag{1}$$

In a case where M2L is V_{DD}, the W of the left side will be $W_{M1}+W_{M2}+W_{M3}$ and the W on the right side will be W_{M1}. Replacing $W=W_{M1}$ and $W_{TUNE}=W_{M2}+W_{M3}$, the following can be obtained as the tipping point of this comparator.

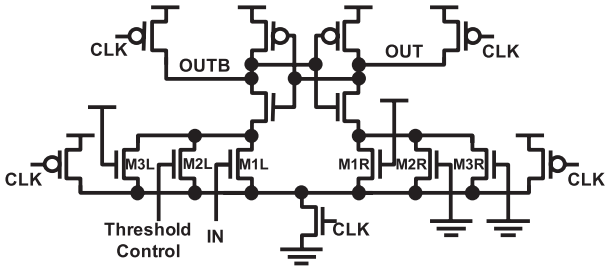

Fig. 6 Proposed digitally controlled comparator with V_{DD} as the reference voltage.

$$(V_{IN} - V_{TH})W = (V_{REF} - V_{TH})(W + W_{TUNE}) \tag{2}$$

$$V_{IN} = \frac{(W + W_{TUNE})}{W} V_{REF} - \frac{W_{TUNE}}{W} V_{TH} \tag{3}$$

Since the reference voltage is V_{DD} and the threshold voltage of the nMOS transistors are constants, the tipping point is controlled completely by the W_{TUNE} which can be tuned by the on and off of M2L.

6. Charger Controller

When the comparators are precharged, the voltage of OUT and OUTB will be both high for the nMOS input comparator and low for the pMOS comparator. When one of the comparators is enabled and the comparator compares the input to the reference voltage, either the OUT or OUTB will change, so by watching the four outputs, the data can be guessed and the input can be precharged accordingly. This scheme reduces the delay to precharge compared to the conventional circuit where the output of the SR latch is used to trigger the precharge.

The actual circuit which can be seen in Fig. 3 is composed of a controller for the pMOS which precharges the line RX_{IN} to V_{DD} and the nMOS which precharges RX_{IN} to low. The controller for the pMOS works as follows. When the comparator clock is low, CRG_P is charged to V_{DD}. If either the L_{OUT} or H_{OUTB} changes, CRG_P becomes low and the pMOS is turned on. This scheme will reduce the need of finely tuning the precharge clock and data delay inside the circuit.

Since L_{OUT} and H_{OUTB} are charged only when the precharge clock is on, it is important that the outputs from the comparator must not dip when they are comparing. If the voltage dips, the precharge will malfunction and both the charger to V_{DD} and the charger to V_{SS} will turn on.

7. Comparator Controller

The comparator controller which is shown in Fig. 3, controls which comparator is enabled according to the previous data. This is mainly done by feeding the outputs of the RS latch to the tail of the comparator. When input data changes and the comparators detect the change, the output of the RS latch will also change, causing the other comparator to be activated during the same clock. This will cause an unwanted oscillation. To eliminate this mode, the outputs of

the comparators are watched, and when the comparators detect a change in input data, the comparators are shut down to prevent the second comparator to be activated.

8. Measurement Results

Figure 7 shows the test chip micrograph and measurement setup. The chip is fabricated in 65 nm CMOS technology. The core area of the RX is $40\,\mu\text{m} \times 30\,\mu\text{m}$ and TX circuit is $5\,\mu\text{m} \times 5\,\mu\text{m}$. Most of the chip area is dedicated to decoupling capacitor for test output buffers. Two flexible PCBs are set and aligned so that the coupling pads of the transmitter and receiver overlap. Figure 8 shows measured waveforms of the transceiver. V_{DD} is 1.2 V and 1 Gb/s data rate is achieved. The pad size is $50\,\mu\text{m} \times 50\,\mu\text{m}$ with a misalignment approximately $25\,\mu\text{m}$. The wire length on the PCB is 10 mm. The RX_{OUT} drives the oscilloscope with pMOS open drain configuration and thus the output voltage is 0.5 V.

Figure 9 shows power consumption dependence on data rate along with the power consumption of conventional work using capacitively coupled channels with similar length and parasitic capacitance [7]. For the proposed circuit, power scales to zero as the data rate approaches zero. At 15 Mb/s there is a 20X improvement in power efficiency. This is important since wide data rate range should be covered in connector applications. Since the V_{DD} of TX and RX are connected during the precharge phase in the contact mode, the power dissipation of TX and RX could not be separated in this measurement setup. Note, however that the sum of the TX and RX in contacting mode and non contacting mode are the same. In the contact mode, the TX charges the parasitic capacitance of TX, and RX while in the non-contact mode, the TX charges the parasitic capacitance of TX and RX charges the parasitic capacitance of RX through precharge. In the non-contacting mode, the two pads are separated with air. The contacting and non-contacting modes were not deliberately made. Figure 10 shows the timing margin of the clock against the data. The target BER (Bit Error Rate) of 10^{-12} is achieved throughout

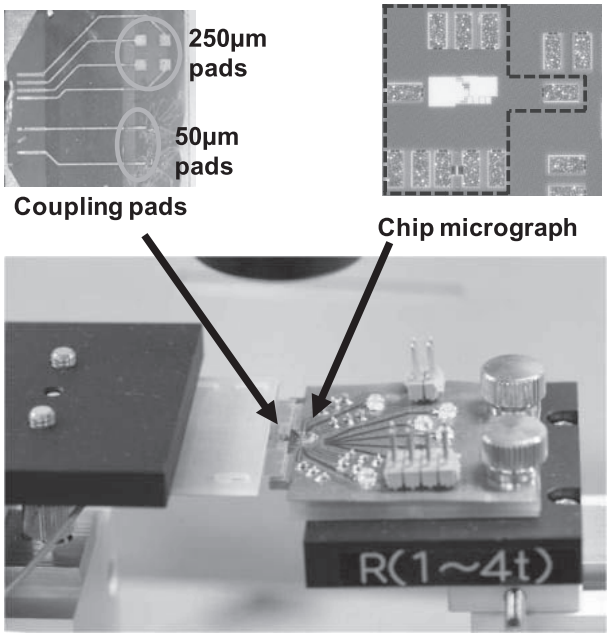

Fig. 7 Measurement setup with detailed views of the coupling pads, and the chip micrograph.

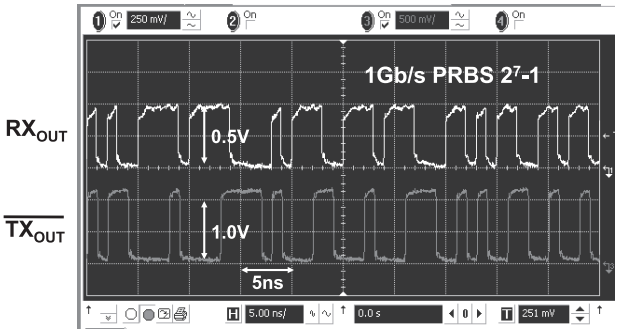

Fig. 8 Measured waveforms of input and output at 1 Gb/s.

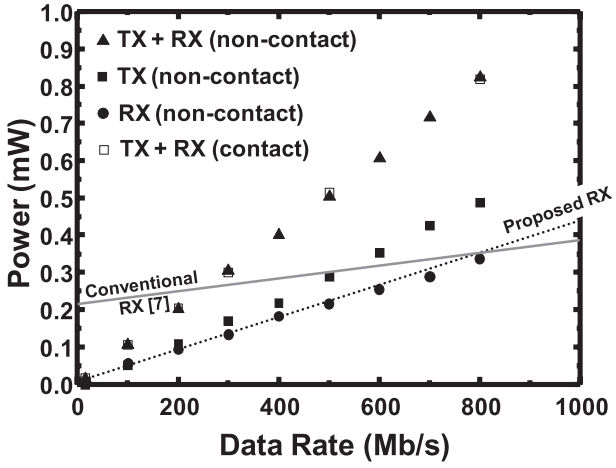

Fig. 9 Power dissipation of TX and RX circuits when contacting and not contacting.

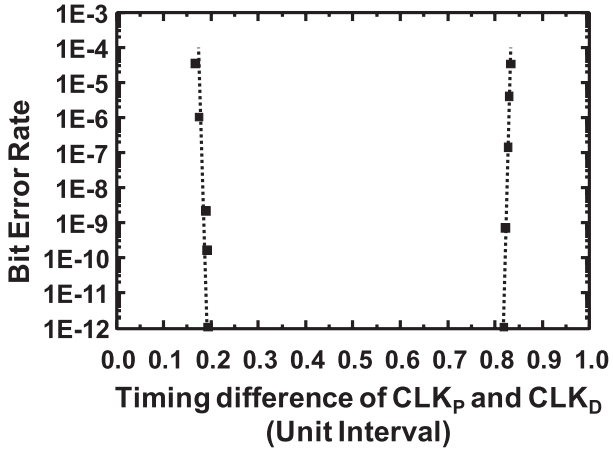

Fig. 10 Measured BER at 800 Mb/s showing a 750 ps timing margin between CLK_P and CLK_D, and stable communication.

a 750 ps timing window, showing that the proposed receiver circuit has a short precharge time and can communicate stably. The 10^{-12} is the minimum BER measureable with the bit error tester used in this work.

9. Discussions

The HDMI type D connector which has one of the smallest pins in mechanical connectors, has 400 μm pitch pins and the pins have a displacement of less than ±50 μm. Presuming that wireless connectors use a similar mechanical structure, the wireless connector in this work can achieve 200 μm pitch pins using 150 μm pads on one side and 50 μm pads on the other side. The smaller pad size and the possibility of placing the pins in a 2D manner increase the number of pins that can be implemented using the same structure.

10. Conclusion

A capacitive coupling wireless connector circuit is implemented with 25X reduction of the pad area compared to previous works, by allowing contacting and non-contacting modes. The proposed track and charge scheme allows both contacting and non-contacting communication through PCB capacitive pads. By making the precharge level of the input of the receiver circuit V_{DD} or V_{SS}, instead of $1/2V_{DD}$, the time necessary to precharge is reduced. The proposed digitally tunable comparator along with the track and charge scheme eliminate the need of $1/2V_{DD}$ or other analog voltages thereby reducing the power to under 1/20 of previous work at low frequencies. A test chip successfully transmitted and received 1 Gb/s, $2^7 - 1$PRBS signal at 1 mW with 50 μm × 50 μm pads, while increasing design freedom of the wireless connectors at the same time.

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