A Closed-form Expression for Estimating Minimum Operating Voltage (V_{DDmin}) of CMOS Logic Gates

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ABSTRACT
In this paper, a closed-form expression for estimating a minimum operating voltage (V_{DDmin}) of CMOS logic gates is proposed. V_{DDmin} is defined as the minimum supply voltage at which circuits can operate correctly. V_{DDmin} of combinational circuits can be written as a linear function of the square-root of logarithm of the number of logic gates and its slope is proportional to the standard deviation of the within-die variation in the threshold voltage difference between PMOS and NMOS transistors. The proposed expression is verified with Monte Carlo simulations using various gate chains. The verification reveals that V_{DDmin} of inverter chains can be estimated within 11% error. The expression is also verified with silicon measurements in a 65nm CMOS process.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General

General Terms
Design, Measurement, Performance, Reliability

Keywords
Minimum operating voltage, subthreshold circuits, variations

1. INTRODUCTION
Scaling down the supply voltage below the threshold voltage (V_{TH}) is a promising approach for achieving ultra-low power circuits [1]. The reduction in the supply voltage, however, could cause functional errors, which is mainly caused by V_{TH} variation. The supply voltage at which the first functional error occurs is defined as a minimum operating voltage (V_{DDmin}) in this paper.

According to [2], the ideal limit of V_{DDmin} is estimated to 52mV. Actually, V_{DDmin} is much higher than the ideal limit due to manufacturing variability. Niiyama et al. reported that V_{DDmin} of ring oscillators rises as the number of logic gates increases [3]. Figure 1 shows V_{DDmin} of an inverter chain as a function of the number of inverters in a 65nm CMOS process. While the difference of V_{DDmin} between the nominal and worst process corners is induced by die-to-die V_{TH} variation, the rise in V_{DDmin} due to the increase in the number of logic gates is caused by within-die V_{TH} variation. In mega gate scale circuits, the rise in V_{DDmin} due to within-die V_{TH} variation is comparable to that due to die-to-die V_{TH} variation. This suggests that the significant rise in V_{DDmin} due to within-die V_{TH} variation must be taken into account for the large-scale subthreshold circuit design.

A common way to obtain V_{DDmin} with consideration for manufacturing variability is to exploit Monte Carlo simulations. However, the simulation time for larger circuits is extremely longer. Therefore, an alternative efficient method to estimate V_{DDmin} is strongly required.

In this paper, a closed-form expression for estimating V_{DDmin} of CMOS logic gates is proposed. Previous researches [2,4] mainly focused on techniques to decrease V_{DDmin} by adjusting body-bias voltages, whereas a lot of attention to the modeling of V_{DDmin} has not been paid. Although several prior works [5,6] modeled V_{DDmin}, the influence of within-die V_{TH} variation has not been discussed well and hence it is not clear how V_{DDmin} depends on the circuit size. This paper is the first work to model V_{DDmin} quantitatively with consideration for both die-to-die and within-die V_{TH} variations and to clearly reveal the dependence of V_{DDmin} on the number of logic gates. The contribution of this paper is that V_{DDmin} of combinational circuits can be easily estimated using the proposed model even in larger circuits.

The proposed model indicates that V_{DDmin} of logic gates can be expressed as a linear function of the square-root of logarithm of the number of logic gates and its slope and intercept depend on within-die and die-to-die V_{TH} variations, respectively. The proposed model is verified with Monte Carlo SPICE simulations using various gate chains in a 65nm and a 40nm CMOS process. This paper reveals that V_{DDmin} of inverter chains can be well estimated by the model with less than 11% error. It is also shown that the proposed model can be applied to circuits fabricated in any manufacturing technologies, since the model is derived from subthreshold characteristics of a MOSFET. In addition, the

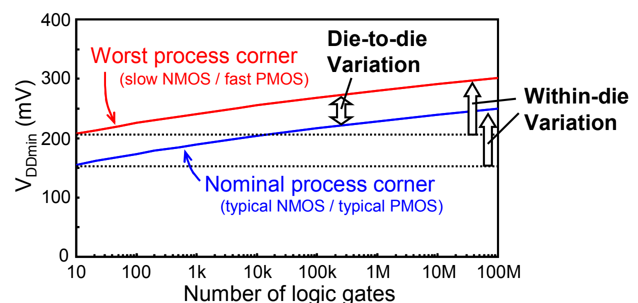

Figure 1. V_{DDmin} of inverter chain in 65nm CMOS process. V_{DDmin} is calculated by closed-form expression proposed in this paper.

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verification is supported by silicon measurements.

2. PROPOSED CLOSED-FORM EXPRESSION

In this section, a closed-form expression for V_{DDmin} of CMOS logic gates is proposed. In order to derive the closed-form model, an inverter chain is used. However, the model is not limited to an inverter and can be extended to other gates, such as NAND and NOR gates.

2.1 VDDmin of Inverter Chain

2.1.1 subthreshold characteristics of MOSFET

The I-V characteristic of a NMOS in subthreshold region is given by [5]

$$I_n = \beta_n \cdot e^{\frac{V_{GS}}{n_n U_T}} \cdot e^{\frac{\eta_n V_{DS}}{n_n U_T}} \left(1 - e^{-\frac{V_{DS}}{U_T}}\right), \quad (1)$$

$$\beta_n = I_{0,n} \frac{W_n}{L_n} e^{-\frac{V_{TH0,n}}{nU_T}}, \quad (2)$$

where V_{GS} and V_{DS} are the gate-source and drain-source voltages, n_n is the subthreshold swing parameter, U_T is the thermal voltage, η_n is the DIBL (Drain Induced Barrier Lowering) coefficient, $V_{TH0,n}$ is the threshold voltage at V_{DS} = 0 V, W_n and L_n are the gate width and length, and $I_{0,n}$ is the technology dependent parameter.

When V_{DS} is much higher than U_T, $(1-\exp(-V_{DS}/U_T))$ in (1) is close to 1, and hence (1) can be approximated to

$$I_n \approx \beta_n \cdot e^{\frac{V_{GS}}{n_n U_T}} \cdot e^{\frac{\eta_n V_{DS}}{n_n U_T}} \quad \text{if} \quad V_{DS} >> U_T. \quad (3)$$

On the other hand, when V_{DS} is much lower than U_T, $(1-\exp(-V_{DS}/U_T))$ can be approximated to V_{DS}/U_T by truncating the Taylor series at the first order [5]. Thus, the subthreshold current can be expressed as

$$I_n \approx \beta_n \cdot e^{\frac{V_{GS}}{nU_T}} \cdot \frac{V_{DS}}{U_T} \quad \text{if} \quad V_{DS} << U_T. \quad (4)$$

For a PMOS, I_p, β_p ($V_{TH0,p}$, W_p, L_p, $I_{0,p}$), n_p, and η_p are substituted for I_n, β_n ($V_{TH0,n}$, W_n, L_n, $I_{0,n}$), n_n, and η_n.

2.1.2 Logical threshold voltage

Figure 2 shows the voltage transfer characteristic of an inverter. When the input voltage is V_{IN} and the output voltage is V_{OUT}, the currents of the NMOS and PMOS of the inverter are identical and from (1) they can be expressed as

$$I_n(V_{GS}=V_{IN}, V_{DS}=V_{OUT}) = I_p(V_{GS}=V_{DD}-V_{IN}, V_{DS}=V_{DD}-V_{OUT}). \quad (5)$$

Let V_{IL} and V_{IH} be input voltages where a unity gain is obtained and they are defined as the logical threshold voltages in this paper. V_{OH} (V_{OL}) is output voltage when the input voltage is V_{IL} (V_{IH}).

When V_{IN} is lower than V_{IL}, V_{OUT} is close to V_{DD}, and hence the following equation is derived from (3), (4), and (5).

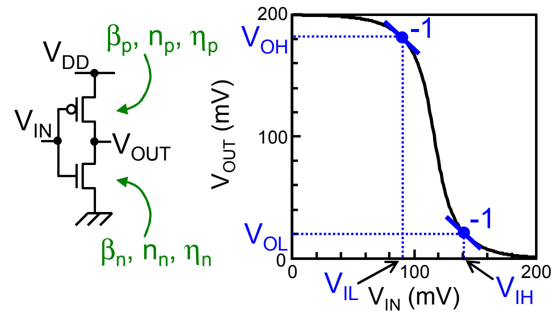

Figure 2. Voltage transfer characteristic of inverter and definition of logical threshold voltages.

$$\beta_n \cdot e^{\frac{V_{IN}}{n_n U_T}} \cdot e^{\frac{\eta_n V_{OUT}}{n_n U_T}} = \beta_p \cdot e^{\frac{V_{DD}-V_{IN}}{n_p U_T}} \cdot \frac{(V_{DD}-V_{OUT})}{U_T}. \quad (6)$$

$\exp(\eta_n V_{OUT}/n_n U_T)$ can be approximated to $\exp(\eta_n V_{DD}/n_n U_T)$, since V_{OUT} is close to V_{DD}, which leads to

$$V_{OUT} = V_{DD} - U_T \frac{\beta_n}{\beta_p} \cdot e^{-\frac{V_{DD}}{n_p U_T}} e^{\frac{2V_{IN}}{nU_T}} \cdot e^{\frac{\eta_n V_{DD}}{n_n U_T}}, \quad (7)$$

where $n=1/((1/n_p+1/n_n)/2)$. When V_{IN} is V_{IL}, the derivative of (7) with respect to V_{IN} is -1. Therefore,

$$-\frac{2}{n}\frac{\beta_n}{\beta_p} \cdot e^{-\frac{V_{DD}}{n_p U_T}} e^{\frac{2V_{IL}}{nU_T}} \cdot e^{\frac{\eta_n V_{DD}}{n_n U_T}} = -1. \quad (8)$$

Consequently, V_{IL} and V_{OH} are obtained as follows.

$$V_{IL} = \frac{V_{DD}}{2} n\left(\frac{1}{n_p} - \frac{\eta_n}{n_n}\right) - \frac{n}{2}U_T\left(\ln\left(\frac{\beta_n}{\beta_p}\right) + \ln\left(\frac{2}{n}\right)\right), \quad (9)$$

$$V_{OH} = V_{DD} - \frac{n}{2}U_T. \quad (10)$$

When V_{IN} is higher than V_{IH}, V_{OUT} is close to the ground (V_{SS}). Thus, the following equation is derived from (3), (4), and (5).

$$\beta_n \cdot e^{\frac{V_{IN}}{n_n U_T}} \cdot \frac{V_{OUT}}{U_T} = \beta_p \cdot e^{\frac{V_{DD}-V_{IN}}{n_p U_T}} \cdot e^{\frac{\eta_p (V_{DD}-V_{OUT})}{n_p U_T}}. \quad (11)$$

Since V_{OUT} is close to V_{SS}, $\exp(\eta_p(V_{DD}-V_{OUT})/n_p U_T)$ can be approximated to $\exp(\eta_p V_{DD}/n_p U_T)$. In the same manner as the abovementioned derivation for V_{IL}, V_{IH} and V_{OL} can be written as

$$V_{IH} = \frac{V_{DD}}{2}\frac{n}{n_p}(1+\eta_p) + \frac{n}{2}U_T\left(\ln\left(\frac{\beta_p}{\beta_n}\right) + \ln\left(\frac{2}{n}\right)\right), \quad (12)$$

$$V_{OL} = \frac{n}{2}U_T. \quad (13)$$

Figure 3 shows the comparison of the logical threshold voltages calculated by (9), (10), (12), and (13) with those obtained from (5) by numerical calculations. When n=1, the error between them is less than 4% as for V_{IL} and V_{IH}, whereas the maximum error when n=2 reaches 20%. This is because the condition of the approximation in (4) is not satisfied when n is large. Since n is typically lower than 2, the logical threshold voltages can be calculated by (9), (10), (12), and (13) with moderate error.

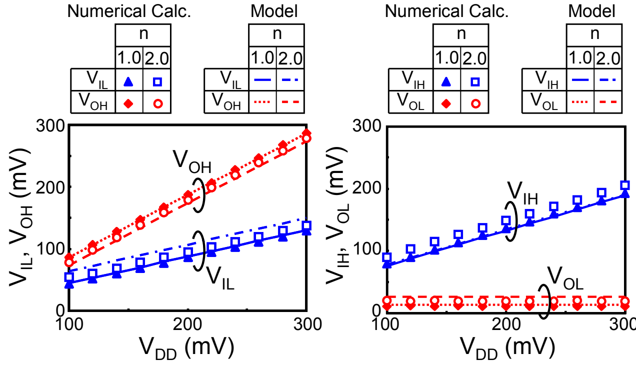

Figure 3. Comparison of logical threshold voltages calculated by models (9), (10), (12), and (13) with those obtained from (5) by numerical calculations.

2.1.3 Expression of V_{DDmin}

Next, the variations of the logical threshold voltages are examined. In this paper, only V_{TH} variation is considered. Random variables $X_{VTH,p}$ and $X_{VTH,n}$ are introduced to express within-die V_{TH} variation as follows.

$$X_{VTH,p} \sim N(0,\sigma_p^{\ 2}),\ X_{VTH,n} \sim N(0,\sigma_n^{\ 2}), \tag{14}$$

where σ_p and σ_n are the standard deviations of within-die V_{TH} variations of PMOS and NMOS transistors, respectively.

Therefore, β_p and β_n in (2) can be written as

$$\beta_p = I_{0,p}\frac{W_p}{L_p}e^{-\frac{V_{TH0,p}+X_{VTH,p}}{n_pU_T}} = \beta_p' e^{-\frac{X_{VTH,p}}{n_pU_T}}, \tag{15}$$

$$\beta_n = I_{0,n}\frac{W_n}{L_n}e^{-\frac{V_{TH0,n}+X_{VTH,n}}{n_nU_T}} = \beta_n' e^{-\frac{X_{VTH,n}}{n_nU_T}}. \tag{16}$$

From (9) and (12), V_{IL} and V_{IH} are given by

$$V_{IL} = \frac{V_{DD}}{2}n\left(\frac{1}{n_p}-\frac{\eta_n}{n_n}\right)-\frac{n}{2}U_T\left(\ln\left(\frac{\beta_n'}{\beta_p'}\right)+\ln\left(\frac{2}{n}\right)\right)+\frac{X_{VTH}}{2}, \tag{17}$$

$$V_{IH} = \frac{V_{DD}}{2}\frac{n}{n_p}(1+\eta_p)+\frac{n}{2}U_T\left(\ln\left(\frac{\beta_p'}{\beta_n'}\right)+\ln\left(\frac{2}{n}\right)\right)+\frac{X_{VTH}}{2}, \tag{18}$$

where

$$X_{VTH} = X_{VTH,n}-X_{VTH,p} \sim N(0,\sigma_{pn}^{\ 2}), \tag{19}$$

$$\sigma_{pn} = \sqrt{\sigma_p^{\ 2}+\sigma_n^{\ 2}}. \tag{20}$$

Equations (17) and (18) indicate that V_{IL} and V_{IH} are normally distributed due to within-die V_{TH} variation. Interestingly, on the other hand, V_{OH} in (10) and V_{OL} in (13) do not depend on V_{TH}.

To investigate V_{DDmin} of an inverter chain, signal transmission between two inverters is analyzed as depicted in Fig. 4. V_{DDmin} is equal to the minimum supply voltage at which the inverter B fails to receive signals from the inverter A. The conditions of the failure can be written as V_{IL} (of inverter B) > V_{OH} (of inverter A) and V_{IH} (of inverter B) < V_{OL} (of inverter A). Please note that we use these conditions instead of SNM (static noise margin) [5,6] since SNM is too strict for evaluating V_{DDmin} of gate chains.

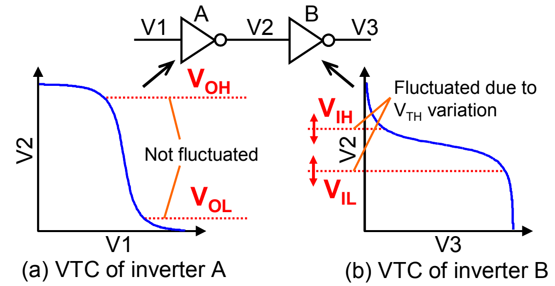

Figure 4. Signal transmission between two inverters.

Thus, the conditions where an inverter is functional are $V_{IL} < V_{OH}$ and $V_{IH} > V_{OL}$. From (10), (13), (17), and (18), the conditions can be written as

$$V_{DD}-\frac{n}{2}U_T > \frac{V_{DD}}{2}n\left(\frac{1}{n_p}-\frac{\eta_n}{n_n}\right)-\frac{n}{2}U_T\left(\ln\left(\frac{\beta_n'}{\beta_p'}\right)+\ln\left(\frac{2}{n}\right)\right)+\frac{X_{VTH}}{2}, \tag{21}$$

$$\frac{n}{2}U_T < \frac{V_{DD}}{2}\frac{n}{n_p}(1+\eta_p)+\frac{n}{2}U_T\left(\ln\left(\frac{\beta_p'}{\beta_n'}\right)+\ln\left(\frac{2}{n}\right)\right)+\frac{X_{VTH}}{2}. \tag{22}$$

Thus, the following inequalities are obtained.

$$g(V_{DD}) < X_{VTH} < f(V_{DD}), \tag{23}$$

$$f(V_{DD}) = aV_{DD}+b-c,\quad g(V_{DD}) = -aV_{DD}+b+c, \tag{24}$$

$$a = 1+\eta, \tag{25}$$

$$b = nU_T\ln\left(\beta_n'/\beta_p'\right), \tag{26}$$

$$c = nU_T(1-\ln(2/n)), \tag{27}$$

where $n \approx n_p \approx n_n$ and $\eta \approx \eta_p \approx \eta_n$.

Let $P_{INV}(V_{DD})$ be the probability for an inverter to work without functional errors at V_{DD}. $P_{INV}(V_{DD})$ is the probability to meet the condition (23), and hence it can be expressed as

$$P_{INV}(V_{DD}) = P(g(V_{DD}) < X_{VTH} < f(V_{DD})) = \Phi\left(\frac{f(V_{DD})}{\sigma_{pn}}\right)-\Phi\left(\frac{g(V_{DD})}{\sigma_{pn}}\right), \tag{28}$$

where $\Phi(x)$ is CDF (cumulative distribution function) of the Gaussian distribution.

Therefore, V_{DDmin} of an inverter chain is given by

$$[P_{INV}(V_{DDmin})]^N = Y, \tag{29}$$

where N is the number of inverters and Y is the probability that the inverter chain is functional at V_{DDmin}, i.e. Y is the yield.

According to the Williams formula [7], $\Phi(x)$ can be approximated to

$$\Phi(x) \approx \frac{1}{2}+\frac{1}{2}\left\{1-\exp\left(-\frac{2x^2}{\pi}\right)\right\}^{\frac{1}{2}} \quad (x \geq 0), \tag{30}$$

$$\approx \frac{1}{2}-\frac{1}{2}\left\{1-\exp\left(-\frac{2x^2}{\pi}\right)\right\}^{\frac{1}{2}} \quad (x \leq 0). \tag{31}$$

When $\exp(-2x^2/\pi) << 1$, the following approximation is given

$$\Phi(x) \approx 1 - \frac{1}{4}\exp\left(-\frac{2x^2}{\pi}\right) \qquad (x \geq 0), \tag{32}$$

$$\approx \frac{1}{4}\exp\left(-\frac{2x^2}{\pi}\right) \qquad (x \leq 0). \tag{33}$$

In the nominal condition, $f(V_{DD}) > 0$ and $g(V_{DD}) < 0$. Thus, the following equation is derived from (28), (32), and (33).

$$P_{INV}(V_{DD}) \approx 1 - \frac{1}{4}\left\{\exp\left(-\frac{2}{\pi}\left(\frac{f(V_{DD})}{\sigma_{pn}}\right)^2\right) + \exp\left(-\frac{2}{\pi}\left(\frac{g(V_{DD})}{\sigma_{pn}}\right)^2\right)\right\}. \tag{34}$$

When PMOS and NMOS transistors are perfectly balanced, i.e. b=0, $f(V_{DD}) = -g(V_{DD})$. Therefore, (29) can be written as

$$[P_{INV}(V_{DD\min})]^N = \left[1 - \frac{1}{2}\exp\left(-\frac{2}{\pi}\left(\frac{f(V_{DD\min})}{\sigma_{pn}}\right)^2\right)\right]^N = Y. \tag{35}$$

Here, the following approximation is introduced.

$$\left[1 - \frac{1}{2}\exp\left(-\frac{2}{\pi}\left(\frac{f(V_{DD\min})}{\sigma_{pn}}\right)^2\right)\right]^N \approx 1 - \frac{N}{2}\exp\left(-\frac{2}{\pi}\left(\frac{f(V_{DD\min})}{\sigma_{pn}}\right)^2\right). \tag{36}$$

From (35) and (36), V_{DDmin} can be expressed as

$$V_{DD\min} = \frac{\sigma_{pn}}{a}\sqrt{\frac{\pi}{2}\ln\left(\frac{N}{2(1-Y)}\right)} + \frac{c}{a}. \tag{37}$$

Generally, PMOS and NMOS transistors are not completely balanced, and the unbalance is relatively large. In this case, $P_{INV}(V_{DD})$ in (34) can be approximated to

$$P_{INV}(V_{DD}) \approx 1 - \frac{1}{4}\exp\left(-\frac{2}{\pi}\left(\frac{f(V_{DD})}{\sigma_{pn}}\right)^2\right) \quad \text{if } \beta_p > \beta_n, \tag{38}$$

$$P_{INV}(V_{DD}) \approx 1 - \frac{1}{4}\exp\left(-\frac{2}{\pi}\left(\frac{g(V_{DD})}{\sigma_{pn}}\right)^2\right) \quad \text{if } \beta_p < \beta_n. \tag{39}$$

By applying the same approximation as (36) to (29), V_{DDmin} is derived as

$$V_{DD\min} = \frac{\sigma_{pn}}{a}\sqrt{\frac{\pi}{2}\ln\left(\frac{N}{4(1-Y)}\right)} + \frac{c-b}{a} \quad \text{if } \beta_p > \beta_n, \tag{40}$$

$$V_{DD\min} = \frac{\sigma_{pn}}{a}\sqrt{\frac{\pi}{2}\ln\left(\frac{N}{4(1-Y)}\right)} + \frac{c+b}{a} \quad \text{if } \beta_p < \beta_n. \tag{41}$$

The expression of V_{DDmin} in (37), (40), and (41) indicates that 1) V_{DDmin} is a function of the square-root of logarithm of the number of inverters (N), 2) the slope is proportional to σ_{pn}, which is the standard deviation of the within-die V_{TH} difference variation defined in (20), 3) the balance of the strength of PMOS and NMOS transistors, which is expressed as the parameter b in (40) and (41), affects the intercept. The parameter b is fluctuated due to die-to-die V_{TH} variation.

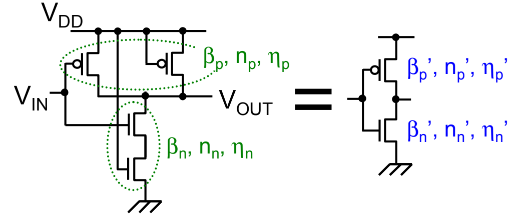

Figure 5. NAND2 gate can be considered equivalent inverter with characterized parameters.

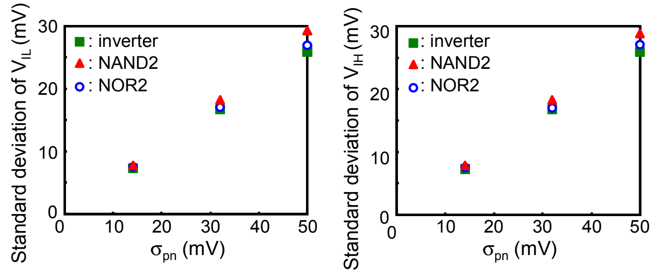

Figure 6. Standard deviations of variations in logical threshold voltages V_{IL} and V_{IH} obtained by Monte Carlo SPICE simulations. σ_{pn} is standard deviation of within-die V_{TH} difference variation defined in (20).

Prior works [2,4] proposed the technique that makes the strength of PMOS and NMOS transistors well-balanced in order to attain ultra-low voltage operation. This technique is beneficial to reduce the parameter b, whereas they have no effects on the slope in (40) and (41). This indicates that the rise in V_{DDmin} caused by within-die V_{TH} variation become much larger as N increases and cannot be mitigated by the conventional technique, which could be a critical problem in large-scale circuits as shown in Fig. 1.

2.2 VDDmin of NAND and NOR Chains

The previous section has focused on the V_{DDmin} of an inverter chain. The closed-form expression in (37), (40), and (41) can be extended to NAND and NOR gates by considering them equivalent inverters as shown in Fig. 5. While Alioto et al. only adjust the transistor strength β [5], this paper characterizes n and η in addition to β. The logical threshold voltage can be calculated by applying these characterized parameters to (9), (10), (12), and (13).

In addition, σ_{pn} of the equivalent inverter is necessary to calculate V_{DDmin}. Figure 6 depicts the standard deviation of the variations in V_{IL} and V_{IH} of an inverter, a two-input NAND2 gate, and a NOR2 gate obtained by SPICE Monte Carlo simulations (10,000 tries). It is assumed that the gate lengths and widths of transistors contained in the NAND2 and NOR2 gates are equal to those of the inverter. This figure indicates that the variations in V_{IL} and V_{IH} of the NAND2 and NOR2 are nearly identical to those of the inverter. This is because one of stacked/paralleled transistors is always pulled-up to V_{DD} or pulled-down to V_{SS}, and hence the influences of those transistors are relatively small. Therefore, the closed-form model can be applied to NAND and NOR gates with the characterized parameters and the same σ_{pn} as an inverter.

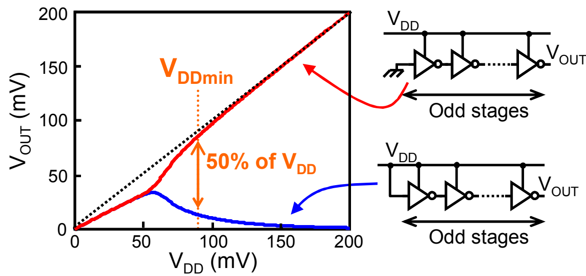

Figure 7. V_{DDmin} of inverter chain obtained by SPICE simulations. V_{DDmin} of NAND, and NOR chains can be obtained in the same manner.

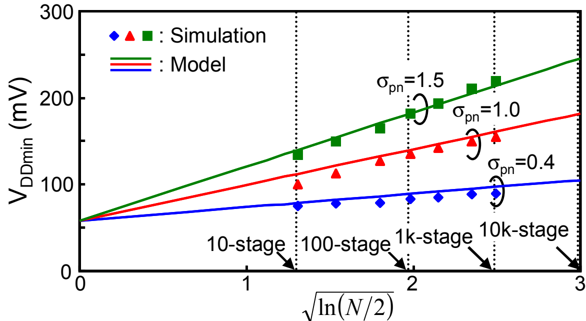

Figure 8. V_{DDmin} of inverter chain as a function of the number of stages (N) in 65nm CMOS process.

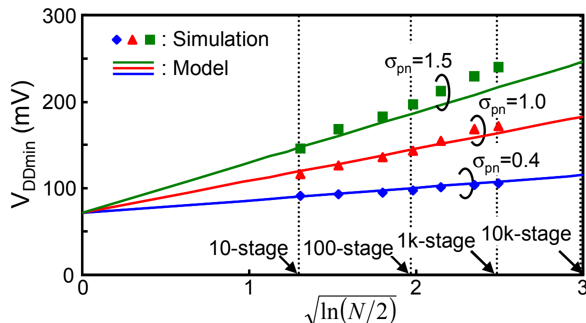

Figure 9. V_{DDmin} of inverter chain as a function of the number of stages (N) in 40nm CMOS process.

3. MODEL VERIFICATION

3.1 Simulation Setup

Various-stage gate chains up to 1001 stages are used for SPICE Monte Carlo simulations to obtain V_{DDmin} as shown in Fig. 7. V_{DD} is swept from 0 V. When V_{DD} is lower than V_{DDmin}, V_{OUT} at V_{IN} = 0 V is equal to V_{OUT} at V_{IN} = V_{DD}. As the supply voltage increases, the difference between the output voltages at V_{IN} = 0 V and at V_{IN} = V_{DD} becomes larger. In this paper, V_{DDmin} is defined as the supply voltage at which the voltage difference reaches 50% of V_{DD}. 100 Monte Carlo simulations are performed with within-die V_{TH} variation. Consequently, V_{DDmin} distribution is obtained. In this paper, V_{DDmin} of the circuit is defined as the median of the distribution, which means the yield is 50%.

3.2 Comparison of Model with Simulation

In this section, V_{DDmin} calculated by the closed-form model in (37), (40) and (41) is compared with V_{DDmin} obtained by the Monte Carlo SPICE simulations explained in Section 3.1. Figure 8 shows V_{DDmin} of the inverter chain as a function of the number of stages

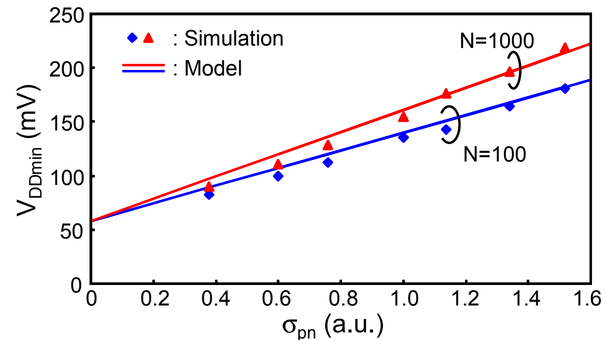

Figure 10. V_{DDmin} of inverter chain as a function of standard deviation of within-die V_{TH} difference variation (σ_{pn}) defined in (20) in 65nm process.

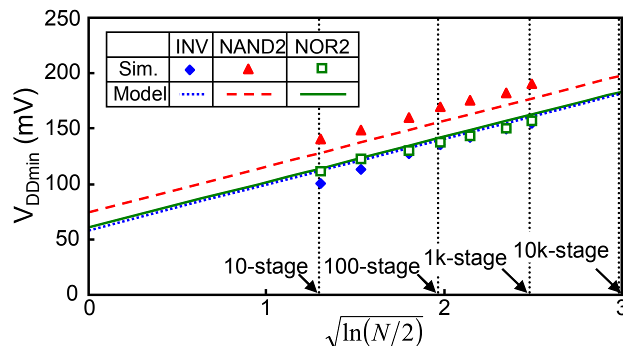

Figure 11. V_{DDmin} of inverter, NAND, and NOR chains as a function of the number of stages (N) in 65nm process.

with various conditions of within-die V_{TH} variation in a 65nm CMOS process. σ_{pn}, which is the standard deviation of the within-die variation in the V_{TH} difference between PMOS and NMOS transistors as defined in (20), is normalized by the nominal value in this process. V_{DDmin} can be well estimated by the model within 11% error. The model does not depend on manufacturing technologies, because the model is derived from the subthreshold characteristics of MOSFET. V_{DDmin} of the inverter chain in a 40nm CMOS process is shown in Fig. 9. V_{DDmin} is also obtained by the model with less than 11% error.

The closed-form expression in (37), (40) and (41) indicates that V_{DDmin} is proportional to σ_{pn}. Figure 10 illustrates V_{DDmin} of the inverter chain as a function of σ_{pn}. This figure indicates that V_{DDmin} obtained by the simulations agrees with the model.

Figure 11 depicts V_{DDmin} of the NAND2 and NOR2 chains in a 65nm CMOS process. V_{DDmin} of the NAND2 and NOR2 chains can be calculated within 10% and 5% errors, respectively. Since $\beta_p > \beta_n$, i.e. PMOS transistors are stronger than NMOS in this process, the NAND2 gate is more unbalanced than the NOR2 gate (|b| in (40) and (41) of the NAND2 is larger than that of the NOR2), which results in higher V_{DDmin} of the NAND2 chains than V_{DDmin} of the NOR2 chains. It should be noted that the slopes of simulated V_{DDmin} of the inverter, NAND2, and NOR2 chains are almost same as shown in Fig. 11, since they have the identical σ_{pn} as described in Section 2.2.

Next, chains consisting of various gates are examined. Let $P_{INV}(V_{DD})$ and $P_{NAND2}(V_{DD})$ be the probabilities to satisfy the condition (23) at V_{DD} of a inverter and an NAND2, respectively.

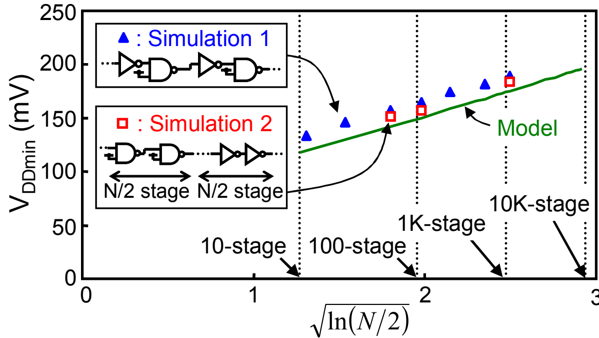

Figure 12. V_{DDmin} of circuits consisting of inverters and NAND's as a function of the number of stages (N).

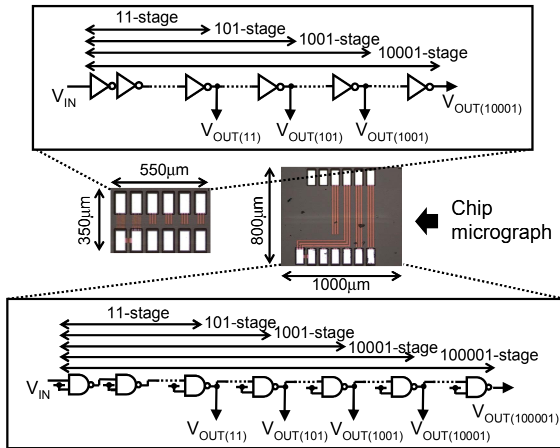

Figure 13. Structure of inverter and NAND chains to measure V_{DDmin} and chip micrograph in 65nm process.

According to (29), V_{DDmin} of the chain consisting of N_1 inverters and N_2 NAND2 gates can be expressed as

$$[P_{INV}(V_{DD\min})]^{N_1} \cdot [P_{NAND2}(V_{DD\min})]^{N_2} = Y, \qquad (42)$$

where Y is the yield.

Figure 12 shows V_{DDmin} of circuits consisting of inverters and NAND2 gates. V_{DDmin} is obtained by (42) with numerical calculations and by the following two simulations; 1) inverters and NAND2's are placed alternately, and the total number of the gates is N, 2) N/2 inverters follow N/2 NAND2 gates. Figure 12 indicates that the difference between V_{DDmin} obtained by the simulations 1 and 2 is small. This is because V_{DDmin} is determined only by the kind and the number of logic gates and V_{DDmin} does not depend on the order of the gates as indicated by (42). This implies that V_{DDmin} of gate chains is equivalent to V_{DDmin} of any combinational circuits consisting of the same kind and number of logic gates.

4. COMPARISON WITH MEASUREMENT

An inverter and a NAND chain to measure V_{DDmin} were fabricated in a 65nm CMOS process. As shown in Fig. 13, those chains are implemented such that V_{DDmin} of various stage chains can be observed in one chain. 20 dies for the inverter chain and 14 dies for the NAND chain were measured. Figure 14 illustrates the measured V_{DDmin}, which is defined as the median of the measured V_{DDmin} distribution. The balance between the strength of PMOS and NMOS transistors (expressed as b in (40) and (41)) of the measured chip is unknown. Thus, the parameter b is determined by fitting the calculated V_{DDmin} to the measured V_{DDmin} of the inverter chain. Using the fitted parameter b, V_{DDmin} of the NAND chain is calculated by the model. Figure 14 indicates that the proposed model also agrees with the measurement results.

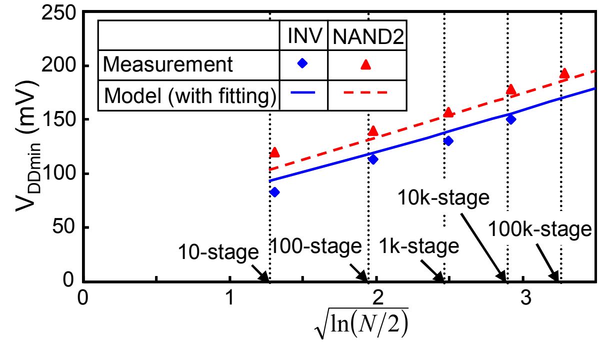

Figure 14. Measured V_{DDmin} of inverter and NAND2 chains in 65nm process, and comparison with model.

5. CONCLUSION

The closed-form expression in (37), (40) and (41) for estimating V_{DDmin} of CMOS logic gates was proposed. V_{DDmin} of logic gates can be expressed as a linear function of the square-root of logarithm of the number of logic gates and its slope and intercept depend on within-die and die-to-die V_{TH} variations, respectively. The proposed model is verified with Monte Carlo simulations using various gate chains. It is revealed that V_{DDmin} of inverter chains can be estimated by the proposed model with less than 11% error. The proposed model is also verified with the silicon measurements and the model is consistent with the measurements.

6. ACKNOWLEDGMENTS

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