

A Voltage-Reference-Free Pulse Density Modulation (VRF-PDM) 1-V Input Switched-Capacitor 1/2 Voltage Converter with Output Voltage Trimming by Hot Carrier Injection and Periodic Activation Scheme

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Abstract

A 1-V input, 0.45-V output switched-capacitor (SC) 2:1 voltage converter is developed in 65-nm CMOS. A proposed voltage-reference-free pulse density modulation (VRF-PDM) increased the efficiency from 17% to 73% at 50- μ A output current by reducing the pulse density and eliminating the voltage reference circuit. An output voltage trimming by the hot carrier injection to a comparator and a periodic activation scheme of the SC converter are also proposed to solve the problems attributed to VRF-PDM.

Introduction

Fig. 1 shows an example of block diagram of an energy efficient SoC. The power supply voltage (V_{DD}) of 1V is converter to a 0.5-V energy efficient near threshold logic circuit by a 1/2 voltage converter, while V_{DD} of 1V is directly supplied to analog/RF and I/O circuits. Instead of a buck converter, a switched-capacitor (SC) converter is developed, because the SC converter has a potential to be fully integrated on a chip. Target of this paper is to develop a 1-V input 1/2 voltage converter with the output current (I_{OUT}) from 50 μ A to 10mA. The design challenges of the 1/2 voltage converter are (1) the degraded efficiency at low I_{OUT} and (2) the implementation of 0.5-V voltage reference circuit (VREF) and the power penalty due to VREF. Note that VREF is often omitted in the previous works [1-7] by simply using an off-chip bias. In addition, design of sub-1V VREF [8] is difficult, because typical VREF operates above 1V. In order to solve the problems, a voltage-reference-free pulse density modulation (VRF-PDM) is proposed to increase the efficiency at low I_{OUT} by reducing the pulse density and eliminating VREF.

Voltage-Reference-Free Pulse Density Modulation

Fig. 2(a) shows a conventional SC 1/2 voltage converter with a constant pulse density (CPD) [2-4] clock. CPD suffers from severe efficiency degradation when I_{OUT} decreases due to excessive clock pulses. Fig. 2(b) shows an other conventional SC 1/2 voltage converter, which rely on VREF and a comparator for pulse density modulation (PDM) [5-7]. VREF has above-mentioned problems. Figs. 2(c) and 3 show a block diagram and a timing chart of the proposed VRF-PDM converter, respectively. The key concept of VRF-PDM is to replace the reference voltage in Fig. 2(b) with the past output voltage (V_{OUT}), thereby eliminating VREF. V_{OUT} is sampled as V_{NOW} and V_{PAST} at each falling edge of CK and CK_{UPDATE} , respectively. Then V_{NOW} and V_{PAST} are compared by a comparator with an offset voltage of ΔV . When $V_{PAST} - V_{NOW}$ is larger than ΔV , a pulse of SC_enable is generated by the comparator to drive the switch matrix. ΔV determines both the pulse density and V_{OUT} .

VRF-PDM, however, has a risk of V_{OUT} to decrease to 0V, because V_{PAST} may decrease to 0V due to the leakage current of the sampling capacitor when I_{OUT} and the pulse density are very small. In order to avoid the abnormal V_{OUT} lowering, a periodic activation scheme (PAS) of the SC converter is proposed. Fig. 4 shows a concept of PAS in VRF-PDM in comparison with the conventional CPD (Fig. 2 (a)) and PDM (Fig. 2 (b)). 3 dots in Fig. 4 correspond to Fig. 3. In PAS, even if COMP_out is always low, SC_enable pulse is generated at every 32 clock cycles as shown in Fig. 3 (c). Because the SC_enable pulse activates the switch matrix in Fig. 2 (c), V_{OUT} goes to $V_{IN}/2$. After that CK_{UPDATE} is

generated and V_{PAST} is refreshed to V_{OUT} . In this way, PAS prevents the abnormal V_{OUT} lowering problem.

Output Voltage Trimming by Hot Carrier Injection

In the proposed VRF-PDM converter, V_{OUT} is determined by ΔV . In order to enable V_{OUT} tuning and the compensation for the random mismatch of the comparator without the fuse trimming, a novel trimming method with a hot carrier injected (HCI) comparator is proposed. Fig. 5 shows a schematic of the HCI comparator. Transistors (M3-M5) are added to a clocked comparator to trim the offset between M1 and M2. Fig. 6 shows a flowchart of the trimming with the HCI comparator using a tester and Table I shows bias conditions for Fig. 6. The goal of the trimming is to make the comparator to flip at $IN1=IN2+\Delta V$. At first, the comparator trip point is checked at $IN1=IN2+\Delta V$. Depending on the comparator output (OUT), threshold voltage (V_{TH}) of M1 or M2 is increased using HCI by applying a high voltage to 1.2-V 65-nm CMOS transistors. Until the trimming is finished, HCI is repeated. In this way, V_{OUT} trimming is achieved without the fuse.

Experimental Results

The VRF-PDM converter is fabricated with a 65-nm CMOS. Fig. 7 shows the die micrograph. Off-chip capacitors C1 and C2 in Fig. 2(c) of 4.7nF are used. Fig. 8 shows the measured dependence of the pulse density, V_{OUT} , and the output ripple on I_{OUT} . In VRF-PDM, the pulse density decreases with the reduced I_{OUT} . ΔV of 25mV is observed in VRF-PDM. Compared with CPD, 3-mV ripple increase is observed in VRF-PDM due to PDM. Fig. 9 shows the measured waveforms of V_{OUT} and SC_enable at different I_{OUT} . As I_{OUT} decreases, the pulse density of SC_enable also decreases, which shows the PDM operation and corresponds to Fig. 8(a). Fig. 10 shows the measured trimming of the offset voltage of the HCI comparator and the retention characteristics for 6 dies. The offset voltage linearly changes with the stress time, which indicates a good controllability. The retention is good for 1 week. Fig. 11 shows the measured dependence of efficiency on I_{OUT} . The efficiency of conventional SC converter with PDM is calculated based on the measured efficiency of the proposed scheme, with subtraction of the power consumed by state-of-the-art low voltage and low power (14 μ W) BGR [8]. Severe efficiency degradation is observed on the conventional scheme with CPD at less than 3-mA output current. In contrast, the VRF-PDM converter achieves above 73% efficiency over I_{OUT} range from 50 μ A to 10mA, with a peak value of 86% at 3mA. Compared with the conventional scheme with CPD, an efficiency increases from 17% to 73% at 50- μ A I_{OUT} . Table II shows the performance summary.

Acknowledgment

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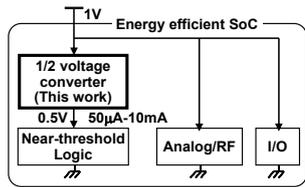


Fig. 1. Block diagram of energy efficient SoC.

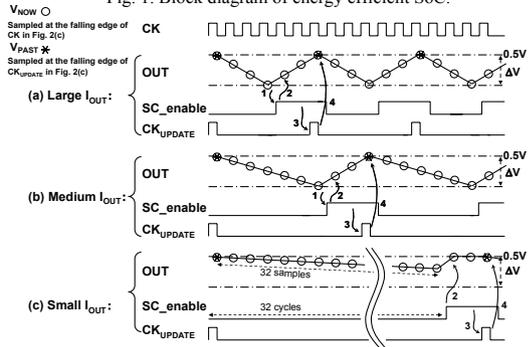


Fig. 3. Timing diagram of proposed SC converter with VRF-PDM.

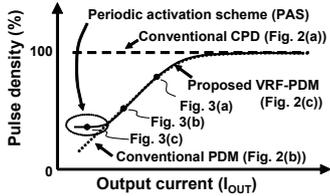


Fig. 4. Concept of periodic activation scheme (PAS) in VRF-PDM.

TABLE I Bias conditions for Fig. 6

Mode	Compare @IN1=IN2+ΔV	Increase V_{TH} of M1 (HCI to M1 for 5s)	Increase V_{TH} of M2 (HCI to M2 for 5s)
V_{DD} (V)	1	2.5	2.5
IN1 (V)	$0.5 + \Delta V$	2.5	0
IN2 (V)	0.5	0	2.5
Trim_enable	L	H	H
CK1		H	H
CK2		L	L
IN1_sel	X	H	L
IN2_sel	X	L	H

Fig. 7. Chip micrograph.

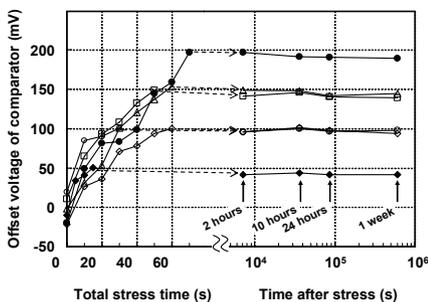


Fig. 10. Measured trimming of offset voltage of HCI comparator and the retention characteristics for 6 dies.

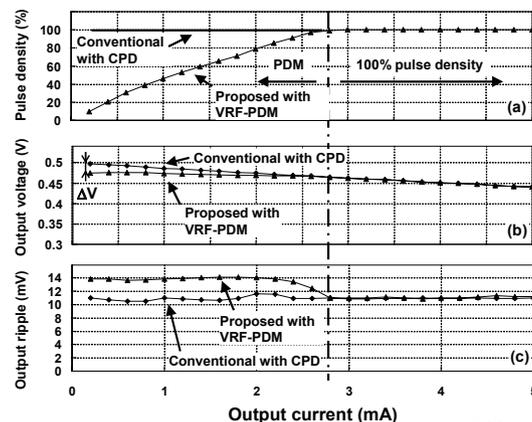


Fig. 8. Measured results of conventional SC converter with CPD and proposed SC converter with VRF-PDM: (a) output voltage (b) pulse density (c) output ripple.

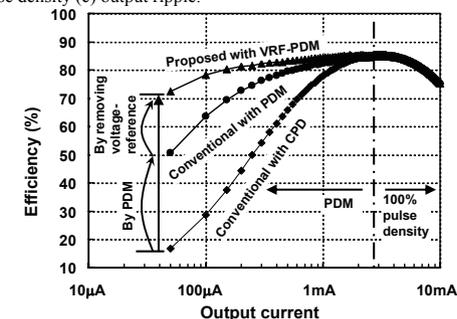


Fig. 11. Efficiency of (1) conventional SC converter with CPD (measured), (2) conventional SC converter with PDM (calculated from (1)), and (3) proposed SC converter with VRF-PDM (measured).

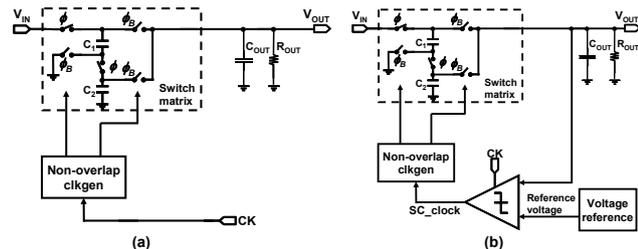


Fig. 2. (a) Conventional SC converter with constant pulse density (CPD). (b) Conventional SC converter with pulse density modulation (PDM). (c) Proposed SC converter with voltage-reference-free pulse density modulation (VRF-PDM).

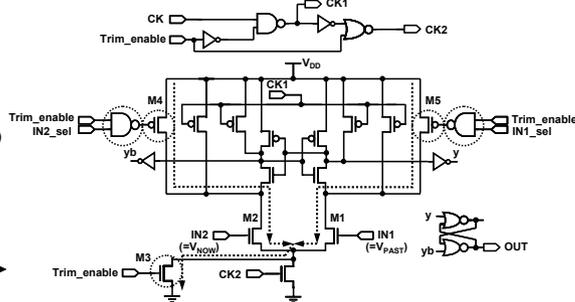


Fig. 5. Comparator with offset trimming by hot carrier injection (HCI).

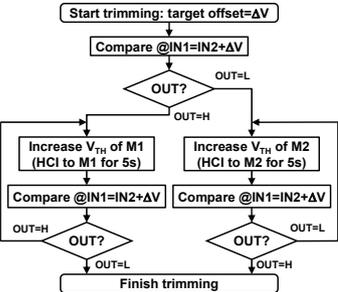


Fig. 6. Flowchart of trimming with HCI comparator using a tester.

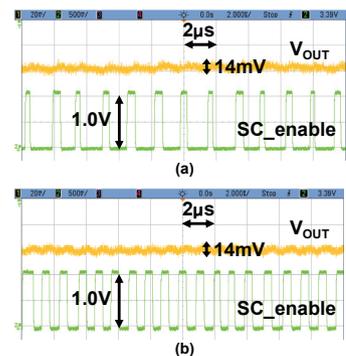


Fig. 9. Measured waveform of V_{OUT} and SC_{enable} . (a) $I_{OUT}=0.5mA$, pulse density=26%. (b) $I_{OUT}=1mA$, pulse density=47%.

TABLE II Performance summary

Process	65-nm CMOS
Input voltage	1.0V
Output voltage	0.45V
Output current	50μA-10mA
Max. output ripple	14mV
Max. power efficiency	86% at 3mA
Frequency	10MHz
Active area	0.079mm ²