12.7-times Energy Efficiency Increase of 16-bit Integer Unit by Power Supply Voltage (V_{DD}) Scaling from 1.2V to 310mV Enabled by Contention-less Flip-Flops (CLFF) and Separated V_{DD} between Flip-Flops and Combinational Logics

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***Abstract*— Contention-less flip-flops (CLFF's) and separated power supply voltages (V_{DD}) between flip-flops (FF's) and combinational logics are proposed to achieve a maximum energy efficiency operation. The proposed technologies were applied to a 16-bit integer unit (IU) for media processing in a 65-nm CMOS process. Measurement results of fabricated chips show that the proposed CLFF reduces the minimum operating voltage of IU's by 64mV on average. By scaling V_{DD} from 1.2V to 310mV with the proposed CLFF, the maximum energy efficiency of 1835GOPS/W and the highest energy efficiency increase of 12.7 times are achieved.**

Keywords -flip-flop, subthreshold circuit, variations

I. INTRODUCTION

Energy efficient LSI's including media processors are strongly required with the growing market of mobile devices such as smart phones. A lot of sub/near-threshold logic circuits are reported [1-5], because reducing the power supply voltage (V_{DD}) increases the energy efficiency of the logic circuits. Low power (LP) CMOS process with low leakage current is used for LSI's in the battery-powered mobile devices. LP CMOS with high threshold voltage (V_{TH}), however, brings a new design challenge for the energy efficient sub/near-threshold logic circuits.

Fig. 1 shows simulated V_{DD} dependence of the energy efficiency of 31-stage fan-out-4 2NAND ring oscillators in 2 types of 65nm CMOS with V_{TH} difference of 0.2V. Maximum energy efficiency operation (MEEO) is achieved at V_{DD} between 300mV and 400mV [1-4]. In this paper, an energy efficiency improvement factor (EEIF) is defined as the maximum energy efficiency normalized by the energy efficiency at nominal V_{DD} of 1.2V. EEIF is 9.1 in the high performance (HP) CMOS process with low V_{TH}, which is consistent with [1]. In contrast, EEIF of LP CMOS is 11.4, which is higher than that of HP CMOS. Minimum operating voltage (V_{DDmin}) of LP CMOS, however, is higher than that of HP CMOS, because V_{DDmin} increases with increasing V_{TH}. In LP CMOS, therefore, MEEO can't be achieved, because V_{DDmin} is higher than MEEO V_{DD} of 310mV.

In this paper, contention-less flip-flops (CLFF) and separated V_{DD} between flip-flops (FF's) and combinational logics are proposed in order to realize MEEO in LP CMOS. The proposed technologies are applied to a 16-bit integer unit (IU) for media processing, and the highest EEIF of 12.7 is achieved by reducing V_{DD} from 1.2V to 310mV.

The remainder of this paper is organized as follows. Section II describes the structure of the developed IU and the proposed CLFF. Measurement results are shown in Section III. Finally, Section IV concludes this paper.

II. INTEGER UNIT (IU) AND CONTENTION-LESS FLIP-FLOP (CLFF)

A. Integer Unit (IU)

Fig. 2 shows a block diagram of the developed 16-bit IU which has implemented popular media processing commands as shown. In this paper, (1) the proposed CLFF and (2) separated V_{DD} between the combinational logic ($V_{DD(LOGIC)}$) and the FF's ($V_{DD(FF)}$) are implemented in IU. Two types of IU's with the conventional FF's and the proposed CLFF's are developed for comparison in a 65-nm CMOS process. The chip micrograph is shown in Fig. 3. The area penalty of the separated V_{DD} is 6%.

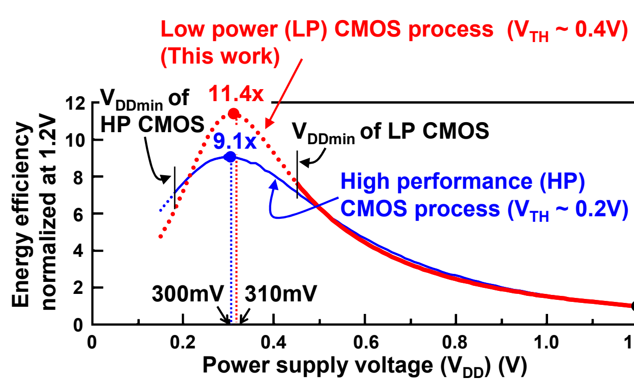


Figure 1. Simulated V_{DD} dependence of energy efficiency of 31-stage ring oscillators in two types of 65nm CMOS with V_{TH} difference of 0.2V.

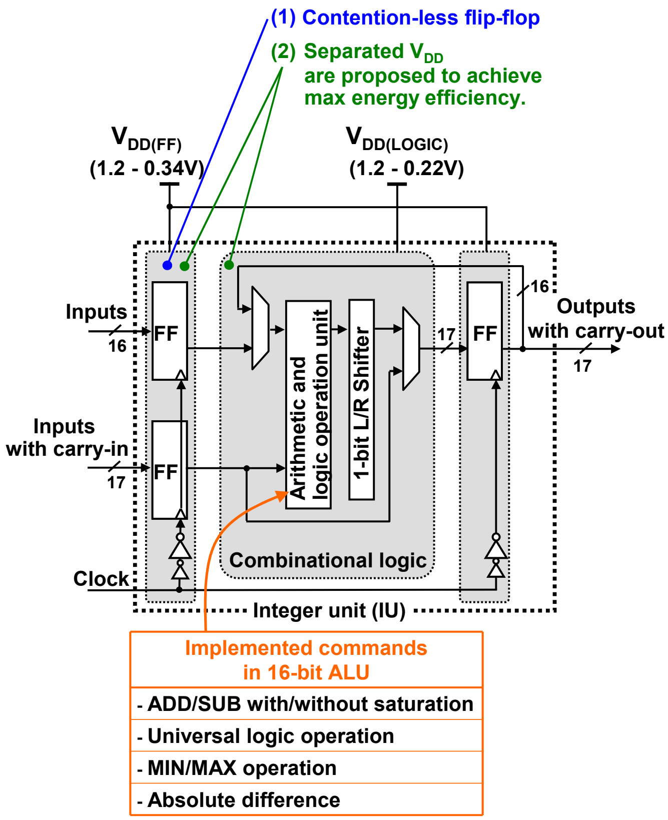


Figure 2. Block diagram of developed 16-bit integer unit (IU) implemented with the proposed flip-flops and separated V_{DD}.

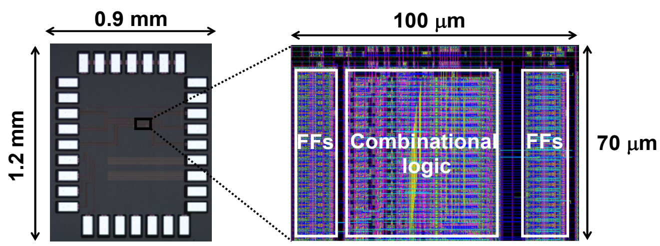
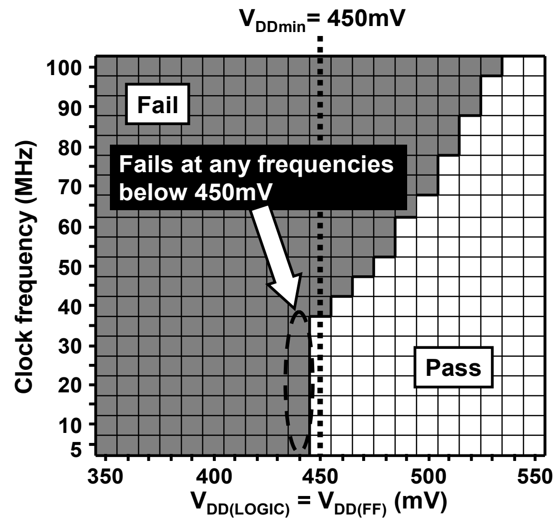
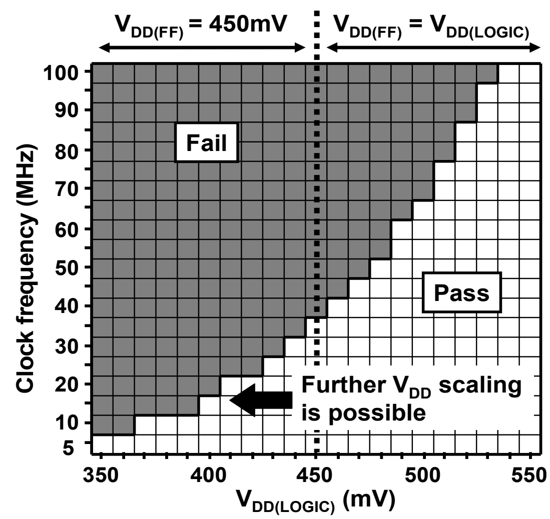


Figure 3. Chip micrograph. Two types of IU's with the conventional FF's and the proposed CLFF's are implemented.



(a) $V_{DD(FF)}$ is equal to $V_{DD(LOGIC)}$



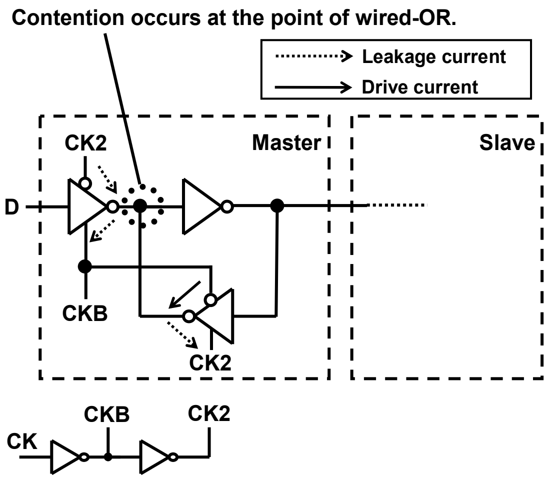
(b) $V_{DD(FF)}$ and $V_{DD(LOGIC)}$ are separated.

Figure 4. Measured shmoo plot of IU with the conventional flip-flops (TBFF in Fig. 5 (a)) fabricated in 65-nm CMOS.

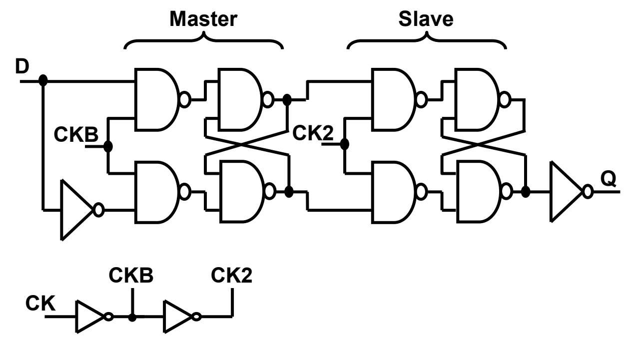
Fig. 4 (a) shows the measured shmoo plot of the IU with the conventional FF's. $V_{DD(FF)}$ is equal to $V_{DD(LOGIC)}$ in Fig. 4 (a), while $V_{DD(FF)}$ and $V_{DD(LOGIC)}$ are separated in Fig. 4 (b). In Fig. 4 (a), the IU does not operate correctly below 450mV even if the clock frequency is reduced from 35MHz to 10kHz, which indicates that V_{DDmin} of IU is 450mV. In this case, MEEO can not be achieved, because MEEO V_{DD} is less than 450mV. V_{DDmin} is determined by the combinational logic or the FF's. In Fig. 4 (b), in order to identify which circuit, the combinational logic or the FF's, determines V_{DDmin}, $V_{DD(FF)}$ is fixed to 450mV and only $V_{DD(LOGIC)}$ is reduced when $V_{DD(LOGIC)}$ is less than 450mV. In this case, Functional $V_{DD(LOGIC)}$ is reduced to 350mV, which indicates that V_{DDmin} of IU is determined by the FF's. Therefore, reducing V_{DDmin} of FF's is required to achieve MEEO.

B. *Contention-Less Flip-Flop (CLFF)*

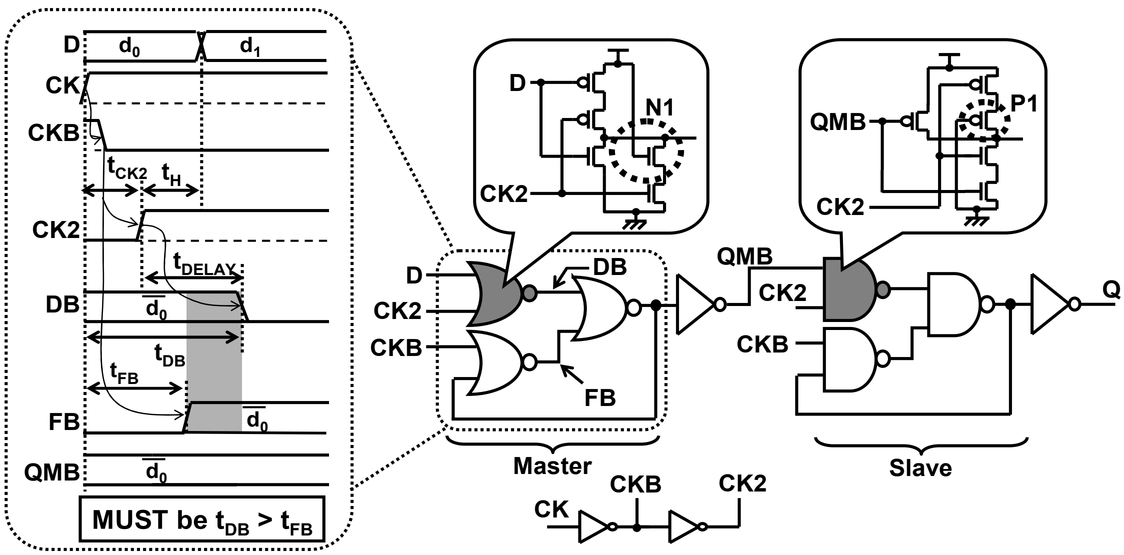
Fig. 5 (a) shows a schematic of a conventional tri-state buffer based FF (TBFF) used in Fig. 4. V_{DDmin} of TBFF is high, because the outputs of the two tri-state buffers are wired-OR and the contention between the tri-state buffers will induce functional errors [5]. Eliminating the wired-OR in TBFF is required to reduce V_{DDmin}, and a classical NAND latch based flip-flop (NLFF) shown in Fig. 5 (b) is one of the candidates. The number of transistors in NLFF, however, increases by 67% compared with TBFF and the corresponding area penalty is not acceptable.



(a) Conventional tri-state buffer based FF (TBFF).



(b) Classical NAND latch based flip-flop (NLFF).



(c) Proposed contention-less flip-flops (CLFF). N1 and P1 are added to mitigate the racing problem

Figure 5. Three types of flip-flops to compare V_{DDmin}.

In order to solve the problems, this paper proposes an area-efficient CLFF shown in Fig. 5 (c) with low V_{DDmin} by eliminating the contention. CLFF has master-slaved latches which are implemented with NOR-type and NAND-type 2:1 multiplexers. When CK=0, the master latch accepts the input data (D) and the slave latch retains data of the previous cycle. In contrast, when CK=1, the master latch retains the latest data and the slave latch accepts it. CLFF has smaller area than NLFF, because 8 2NAND-gates in NLFF are replaced with 6 2NOR/2NAND-gates in CLFF.

However, reducing the gates creates a racing problem. It is explained in the timing chart about the master latch of CLFF in Fig. 5 (c). After the rising edge of CK, the inverted data on DB is written to the feedback node (FB). Therefore, t_{DB} should be larger than t_{FB}, because a write-error occurs if $t_{DB} < t_{FB}$. In an ideal case without delay variations, t_{DB} is larger than t_{FB}, because t_{DB} - t_{FB} equals to the delay of an inverter. In contrast, in reality with the large transistor delay variations at low V_{DD}, t_{DB} may be smaller than t_{FB} and the write-error occurs. In order to increase t_{DB} - t_{FB}, t_{CK2} or t_{DELAY} should be increased. Increasing t_{CK2} is not a good choice, because the hold margin (t_H) is decreased. Therefore, t_{DELAY} is increased to alleviate the racing problem by adding an nMOS (N1) in the 2NOR shown in gray in Fig. 5 (c) and increasing the propagation delay from rising CK2 to falling DB.

In the same way, a pMOS (P1) is added in the slave latch. N1 and P1 do not increase the switching power of CLFF, because they are normally ON transistors. As a result, compared with TBFF, the number of the transistors, total gate width, and the area of the proposed CLFF is 1.4x, 3.9x, and

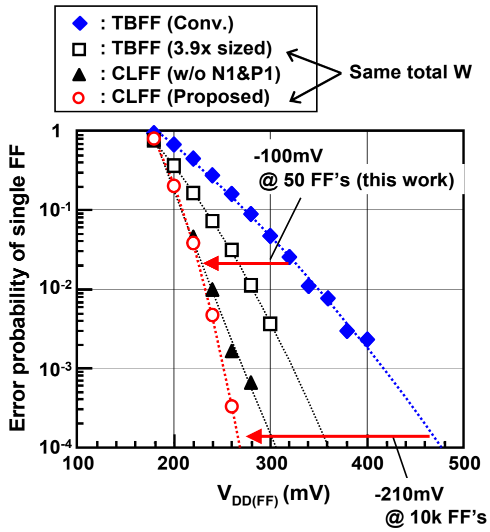


Figure 6. Simulated $V_{DD(FF)}$ dependence of error probability of single FF. In order to compare V_{DDmin} among various flip-flops, 3000 times Monte Carlo SPICE simulations were performed with random V_{TH} variations. V_{DDmin} of the proposed CLFF is improved compared with V_{DDmin} of the CLFF without N1 and P1, since adding N1 and P1 alleviates the racing problem.

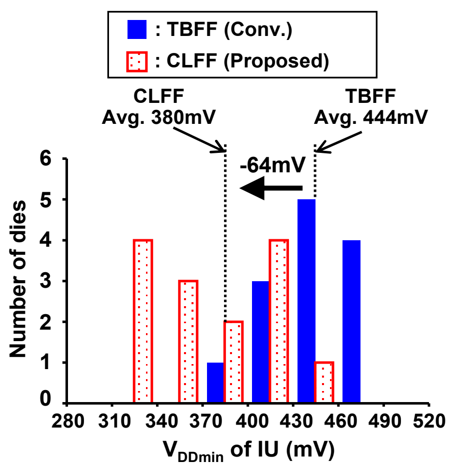


Figure 7. Measured die-to-die V_{DDmin} distributions of IU's with TBFF and CLFF derived as shown in Fig. 4 (a).

2.8x, respectively. Compared with NLFF, the number of the transistor of CLFF is reduced by 15%.

In order to compare V_{DDmin} between TBFF and CLFF, Fig. 6 shows the simulated $V_{DD(FF)}$ dependence of the error probability of single FF. 3000 times Monte Carlo SPICE simulations were performed with the random V_{TH} variations. In order to check the effect of circuit topology of FF's and the newly added transistors (N1 and P1) in CLFF, TBFF with the same total gate width as the proposed CLFF and CLFF without N1 and P1 are also included for the comparison. Compared with TBFF, V_{DDmin} of CLFF is reduced by 100mV and 210mV at the error probability of 0.02 (= 50 FF's which is included in IU in Fig. 2) and 10^{-4} (= 10k FF's), respectively, which indicates the V_{DDmin} reduction is more effective at larger scale digital circuits. At the same total gate width, V_{DDmin} of CLFF is lower than that of TBFF, which proves the superiority of the circuit topology of CLFF over TBFF. In addition, V_{DDmin} of the proposed CLFF (with added transistors N1 and P1) is reduced by 40mV at the error probability of 10^{-4} compared with V_{DDmin} of the CLFF without N1 and P1, which implies N1 and P1 mitigate the racing problem and improve the robustness to the transistor variations.

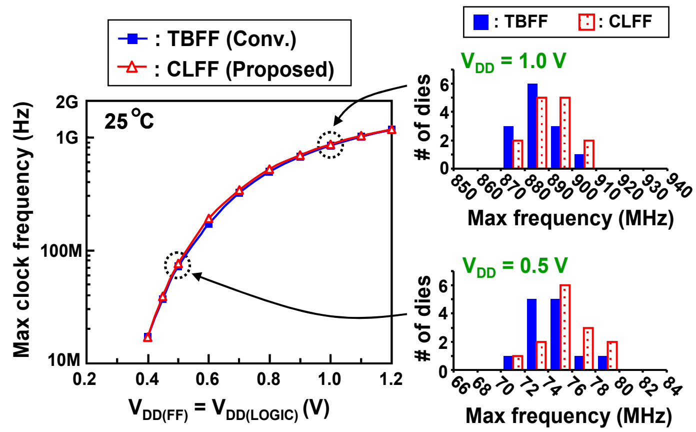


Figure 8. Measured V_{DD} dependence of maximum clock frequency of IU's with TBFF and CLFF, and measured die-to-die maximum clock frequency distributions of IU's with TBFF and CLFF at 1.0V and 0.5V.

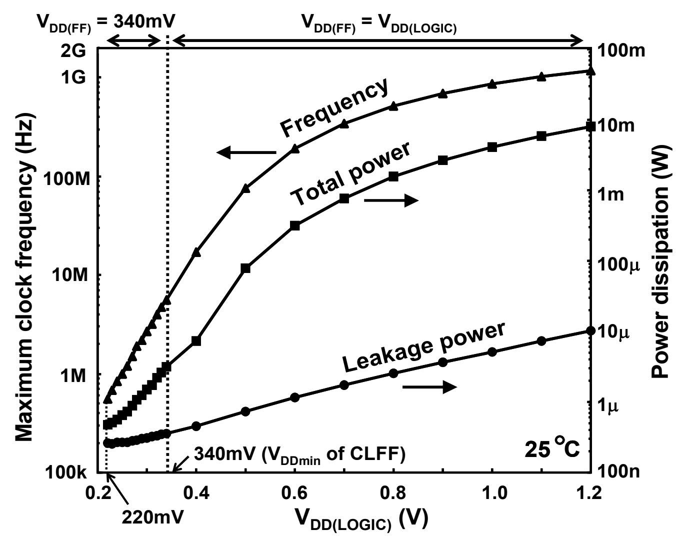


Figure 9. Measured $V_{DD(LOGIC)}$ dependence of maximum clock frequency, total power, and leakage power of IU with CLFF. V_{DDmin} of CLFF is 340mV.

III. Measurement Results

Fig. 7 shows the measured die-to-die V_{DDmin} distributions of IU's with TBFF and CLFF derived as shown in Fig. 4 (a). By replacing TBFF with CLFF in IU, the average V_{DDmin} is reduced by 64mV.

Fig. 8 illustrates the measured V_{DD} dependence of maximum clock frequency of IU's with TBFF and CLFF. Measurement results of die-to-die maximum clock frequency distributions of IU's with TBFF and CLFF at 1.0V and 0.5V are also depicted. Fig. 8 indicates that CLFF has no speed penalty over TBFF.

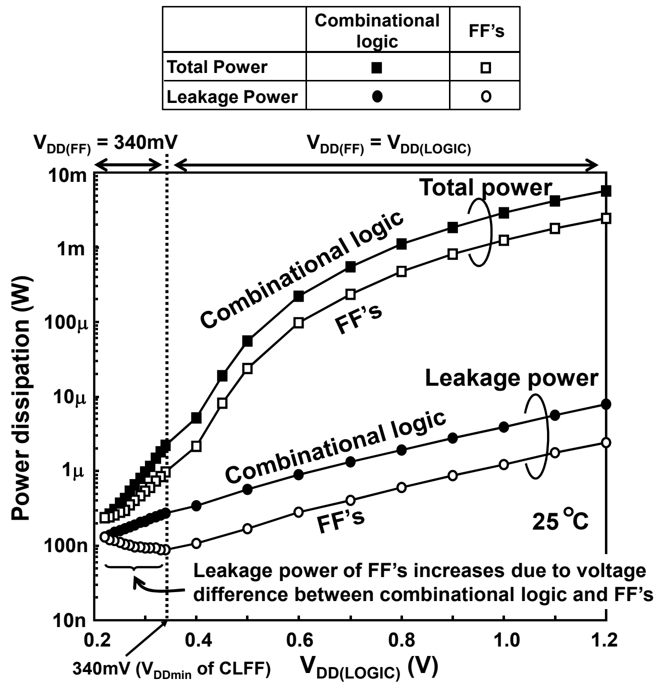


Figure 10. Measured $V_{DD(LOGIC)}$ dependence of breakdown of total power and leakage power of IU with CLFF. IU consists of the combinational logic and FF's as shown in Fig. 2. V_{DDmin} of CLFF is 340mV.

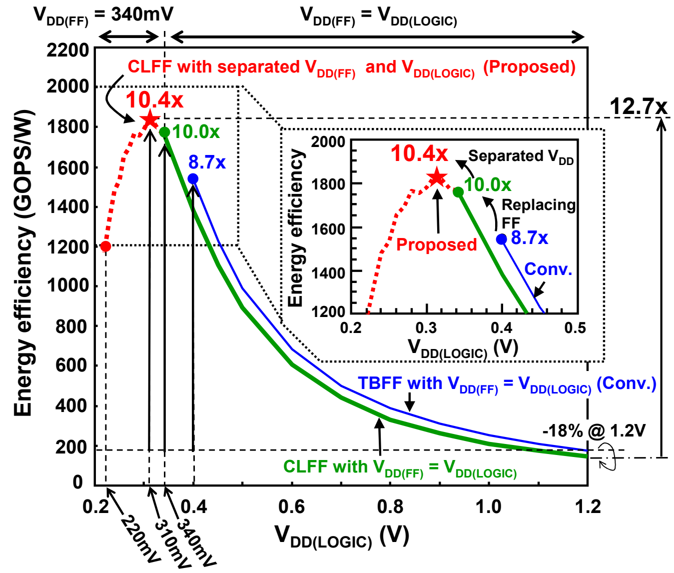


Figure 11. Measured $V_{DD(LOGIC)}$ dependence of the energy efficiency of IU's with TBFF and CLFF. By combining the proposed CLFF and the separated V_{DD}, MEEO is realized at $V_{DD(LOGIC)}$=310mV and $V_{DD(FF)}$=340mV, and 1835GOPS/W (1.7μW and 3.2MHz) and the highest EEIF's of 10.4 and 12.7 based on 1.2-V IU's with TBFF and CLFF are successfully achieved, respectively.

Fig. 9 shows the measured $V_{DD(LOGIC)}$ dependence of the maximum clock frequency, the total power, and the leakage power of IU with CLFF. The total power dissipation was obtained when the add operation with random input patterns was performed. Fig. 10 shows the measured $V_{DD(LOGIC)}$ dependence of breakdown of total power and leakage power of IU with CLFF. IU consists of the combinational logic and FF's as shown in Fig. 2. Fig. 10 indicates that the power dissipation of the combinational logic is larger than that of FF's and the leakage power of FF's increases with decreasing $V_{DD(LOGIC)}$ due to the increase in the voltage difference between $V_{DD(FF)}$ and $V_{DD(LOGIC)}$ when $V_{DD(LOGIC)}$ is less than 340mV. The total leakage power shown in Fig. 9, however, decreases as $V_{DD(LOGIC)}$ is lowered. Therefore, the leakage power of FF's due to the separate V_{DD} is not a serious problem.

Fig. 11 shows the measured $V_{DD(LOGIC)}$ dependence of the energy efficiency of IU's with TBFF and CLFF. IU with TBFF can not achieve MEEO due to 400-mV V_{DDmin}, and EEIF is 8.7. By replacing TBFF with CLFF, V_{DDmin} of CLFF is reduced to 340mV at the cost of the 18% reduction of the energy efficiency at 1.2V, because the power consumption of CLFF is larger than that of TBFF. IU with CLFF, however, can not achieve MEEO and EEIF of 10.0 based on IU with TBFF (176.4GOPS/W, 6.5mW, and 1.15GHz at 1.2V). In order to achieve MEEO, separated $V_{DD(FF)}$ and $V_{DD(LOGIC)}$ is proposed. In IU with CLFF, when $V_{DD(LOGIC)}$ is less than 340mV, $V_{DD(FF)}$ is fixed to 340mV and only $V_{DD(LOGIC)}$ is reduced. By combining the proposed CLFF and the separated V_{DD}, MEEO is realized at $V_{DD(LOGIC)}$=310mV and $V_{DD(FF)}$=340mV, and 1835GOPS/W (1.7μW and 3.2MHz) and the highest EEIF's of 10.4 and 12.7 based on 1.2-V IU's with TBFF and CLFF are successfully achieved, respectively.

TABLE I. COMPARISON WITH THE PUBLISHED SUB/NEAR-THRESHOLD LOGIC CIRCUITS.

Reference		[1]	[2]	[3]	[4]	This work
CMOS technology		65nm	65nm	45nm	32nm	65nm
V_{DD}	Nominal (V)	1.2	1.2	1.1	1.0	1.2
	Min. energy (mV)	320	400	300	340	310
	Min. functional (mV)	230	N.A.	230	260	220
Energy efficiency improvement factor (EEIF)*		9.6x	8.3x	8x	5.7x	12.7x (**) 10.4x (***)
Circuit type		Motion estimation accelerator	DCT & quantization	SIMD vector processing accelerator	Re-configurable arrays	Integer unit

(*) Energy efficiency improvement factor (EEIF) = (Energy efficiency @ Min. Energy V_{DD}) / (Energy efficiency @ Nominal V_{DD})
(**) EEIF based on 1.2-V IU with proposed CLFF
(***) EEIF based on 1.2-V IU with conventional TBFF

Table I shows a comparison with the published sub/near-threshold logic circuits. Developed IU achieved the highest EEIF.

IV. CONCLUSION

In this paper, contention-less flip-flop (CLFF) and separated V_{DD} between FF's and combinational logics were proposed. The proposed technologies were applied to a 16-bit integer unit (IU) for media processing. Two types of IU's with the conventional FF's and with proposed CLFF's were fabricated in a 65-nm CMOS process. Measurement results revealed that the proposed CLFF can reduce the average V_{DDmin} of IU's by 64mV compared with the conventional FF's, and the maximum energy efficiency of 1835GOPS/W (1.7μW and 3.2MHz) at $V_{DD(LOGIC)}$=310mV and $V_{DD(FF)}$=340mV is achieved by combining the proposed CLFF and the separated V_{DD}. Consequently, IU with CLFF accomplished the highest energy efficiency increase of 12.7 times.

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