Reduction of Minimum Operating Voltage (V_{DDmin}) of CMOS Logic Circuits with Post-Fabrication Automatically Selective Charge Injection

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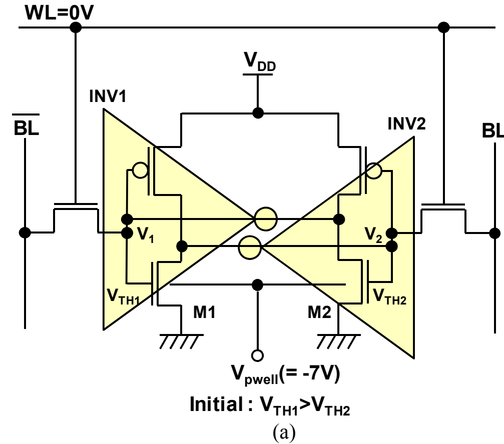
***Abstract*— In order to reduce minimum operating voltage (V_{DDmin}) of CMOS logic circuits, a new method reducing the within-die random threshold (V_{TH}) variation of transistors by a post-fabrication automatically selective charge injection using substrate hot electrons (SHE) is proposed along with novel circuitry to utilize this. In the new circuit, switches are added to combinational logic circuits in order to turn them into latch loops. In order to reduce V_{DDmin}, design guides on the optimal (1) loop topology, (2) number of stages in a loop, (3) V_{TH} shift per charge injection, and (4) number of charge injection trials are explored through simulations. By applying the proposed scheme to 96-stage inverter chain fabricated in 65-nm CMOS, the measured reduction of V_{DDmin} from 94mV to 74mV is successfully demonstrated for the first time.**

I. Introduction

Energy efficient operation of CMOS logic circuits enabled by reducing the power supply voltage (V_{DD}) is strongly required and a lot of sub/near-threshold logic circuits are reported [1-5]. The V_{DD} scaling, however, is hindered by the minimum operating voltage (V_{DDmin}) [6] of CMOS logic gates. V_{DDmin} is the minimum power supply voltage when the circuits operate without function errors. Timing errors are not considered in this paper. V_{DDmin} increases with increasing number of logic gates and CMOS technology down-scaling, because V_{DDmin} is determined by the random transistor variations [6]. The trend of increasing V_{DDmin} is a serious problem in the design of future ultra low voltage (V_{DD} < 0.4V) logic circuits. A straightforward method to reduce the random transistor variations is to increase the size of transistors, which is not practical. An alternative post-fabrication self-convergence scheme for suppressing the random variability is proposed in [7-8]. The threshold voltage (V_{TH}) variation is reduced by the substrate hot electron (SHE) stress [7] or BTI stress [8] for SRAM cells and the drain avalanche hot carrier (DAHC) stress for logic transistors [7], respectively. SHE or BTI stress is effective only for two inverter latch in the SRAM cell and is not effective for logic circuits, because it is difficult to form the two inverter latch in random logic circuits. DAHC is not practical for logic circuits, because DAHC requires half V_{DD} DC biasing to the gate of all transistors in logic circuits and DAHC has large DC current during the stress.

In this paper, in order to reduce V_{DDmin} of CMOS logic circuits, a new method reducing the within-die random V_{TH} variation of transistors by a post-fabrication automatically selective charge injection using SHE is proposed along with novel circuitry to utilize this.



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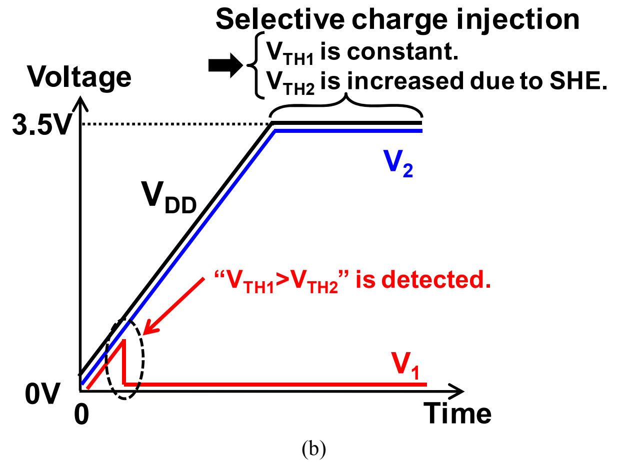

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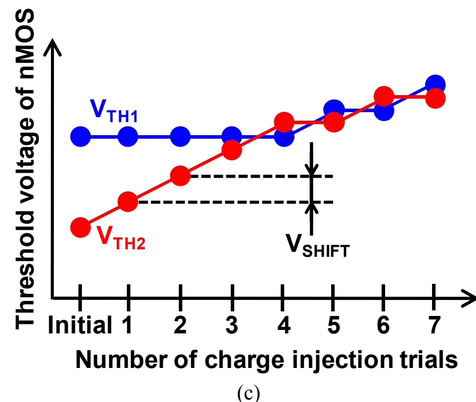


(c)

Fig. 1 Automatically selective charge injection scheme in SRAM cell. (a) Schematic of SRAM cell. (b) Waveforms applied to SRAM cell for automatically selective charge injection scheme. (c) Dependence of V_{TH1} and V_{TH2} on number of charge injection trials.

The remainder of this paper is organized as follows. Section II presents the concept of the proposed post-fabrication automatically selective charge injection scheme and the proposed circuit. Section III presents design guides for the proposed circuit on the optimal (1) loop topology, (2) number of stages in a loop, (3) V_{TH} shift per charge injection, and (4) number of charge injection trials. Section IV describes the details of the fabricated 96-stage inverter chain test chips in 65-nm CMOS and the measured reduction of V_{DDmin}. Finally, Section V concludes this paper.

II. PROPOSED POST-FABRICATION AUTOMATICALLY SELECTIVE CHARGE INJECTION SCHEME

Original concept of automatically selective charge injection scheme in SRAM cell is explained. Then, the concept is expanded to logic circuit applications.

A. Original Concept of Automatically Selective Charge Injection Scheme for SRAM Cell

Fig. 1(a) shows a schematic of an SRAM cell and Fig. 1(b) shows waveforms applied to the SRAM cell for the automatically selective charge injection scheme [7]. A negative (e.g. -7V) p-well bias (V_{pwell}) is applied to M1 and M2. Then, V_{DD} is increased from 0V to a high voltage (e.g. 3.5V) and the high voltage is kept for a while (e.g. 1 min). When V_{TH} of M2 (V_{TH2}) is lower than V_{TH} of M1 (V_{TH1}), V_1 goes to 0V during the ramp of V_{DD}, thereby only V_{TH2} is increased due to the SHE stress, because 3.5V is applied to V_2 instead of V_1. This is the concept of automatically selective charge injection, because either M1 or M2 with lower V_{TH} is automatically selected and V_{TH} of the transistor with the lower V_{TH} is increased by the charge injection due to the SHE stress. The V_{TH} shift due to the charge injection is nonvolatile. As shown in Fig. 1(c), by repeating the charge injection process, the mismatch between V_{TH1} and V_{TH2} is reduced [8].

B. Proposed Automatically Selective Charge Injection Scheme for Logic Circuits

Fig. 2(a) shows a schematic of a normal logic circuit. In order to apply the concept of automatically selective charge injection scheme for SRAM cell into the logic circuit, latch loops should be introduced in the logic circuit. Figs. 2(b) and (c) show schematics of the proposed logic circuit with the automatically selective charge injection scheme, where switches are added to combinational logic circuits in order to turn them into latch loops. Fig. 2(b) shows a normal logic operation mode and Fig. 2(c) shows a latch mode for automatically selective charge injection scheme. Ideally, all logic gates should be included in the latch loops. The inputs of each latch loop should be adequately clamped to V_{DD} or V_{SS} in order to achieve the latch operation. For example, the input of 2NAND is clamped to V_{DD} and the input of 2NOR is clamped to V_{SS}. How to exhaustively add the switches to random combinational logic circuits in order to form the latch loops is out of the scope of this paper. By repeating the charge injection process as shown in Figs. 1(b) and (c), the within-die random V_{TH} variation is reduced, thereby reducing V_{DDmin} of the logic circuit. The charge injection could be performed at pre-shipment test, because the charge injection is nonvolatile.

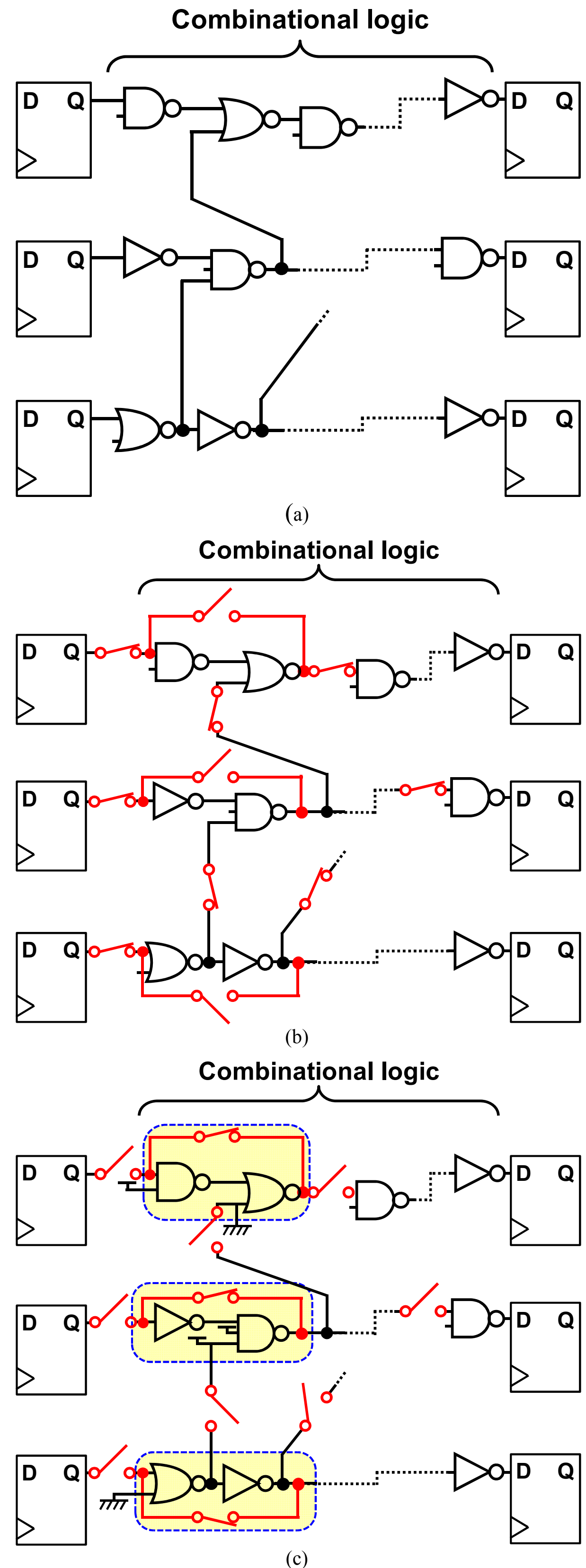


Fig. 2 Schematic of a logic circuit. (a) Normal logic circuit. (b) Proposed logic circuit with automatically selective charge injection scheme in normal logic operation mode. (c) Proposed logic circuit in latch mode.

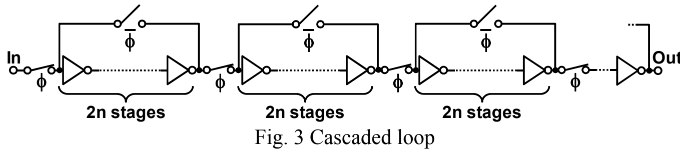


Fig. 3 Cascaded loop

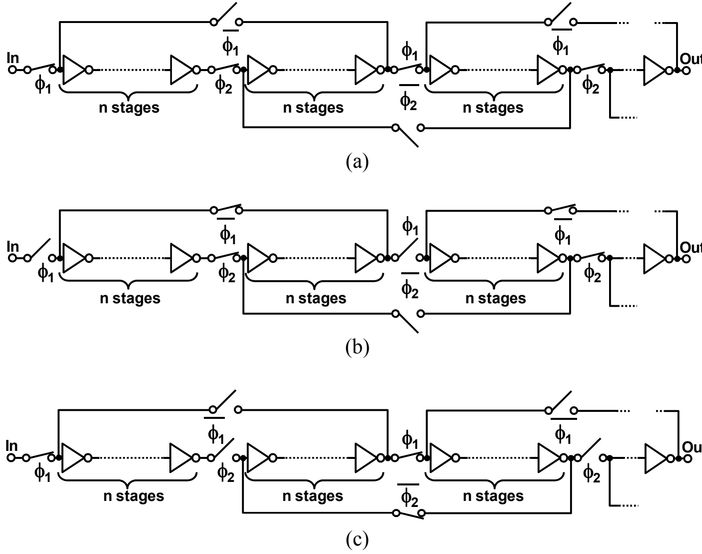


Fig. 4 Staggered loop topology. (a) Normal logic operation mode. (b) Odd-loop latch mode. (c) Even-loop latch mode.

Because the high voltages shown in Fig. 1(b) would be supplied from a tester, high voltage generators are not required.

III. Optimal Implementation of Automatically Selective Charge Injection Scheme

In this section, in order to effectively reduce V_{DDmin}, design guides on the optimal (1) loop topology, (2) number of stages in a loop, (3) V_{TH} shift per charge injection, and (4) number of charge injection trials are explored through simulations.

Two loop topologies for the charge injection scheme are compared. Fig. 3 shows a cascaded loop topology and Fig. 4 shows a staggered loop topology. 2n-stage inverters are included in each latch loop. In Figs. 3 and 4, the combinational logic circuit is simplified to an inverter chain. In Fig. 3, each latch loop is serially connected and the cascaded loop has only one latch mode. In contrast, the staggered loop in Fig. 4 has two latch modes. Fig. 4(a) shows a normal logic operation mode, Fig. 4(b) shows an odd-loop latch mode, and Fig. 4(c) shows an even-loop latch mode.

In order to investigate the V_{DDmin} reduction by the charge injection scheme, V_{TH} variation of nMOS is simulated with a Monte Carlo simulation using Matlab. Reducing V_{TH} variation of either nMOS or pMOS is enough, because V_{DDmin} of each logic gate is determined by the balance between nMOS and pMOS transistors in each logic gate [9]. Therefore, the automatically selective charge injection is applied to only nMOS transistors. Fig. 5 shows simulated distributions of V_{TH} of nMOS with different number of charge injection trials (m) in a staggered loop with n=1. The normal distribution is assumed for the initial distributions of V_{TH}. The initial and current

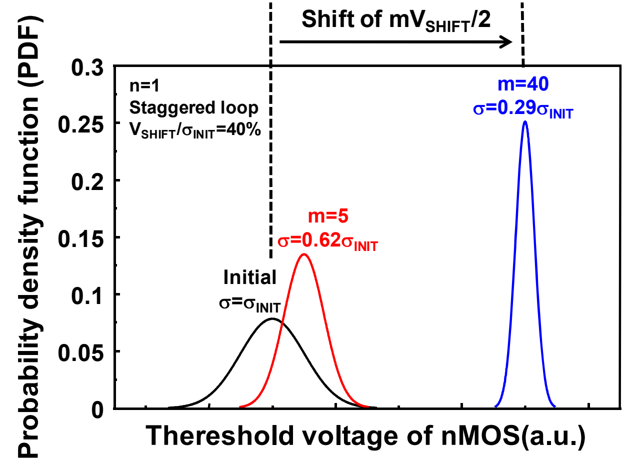


Fig. 5 Simulated distributions of V_{TH} of nMOS with different number of charge injection trials (m) in staggered loop with n=1 and V_{SHIFT}/σ_{INIT} =40%.

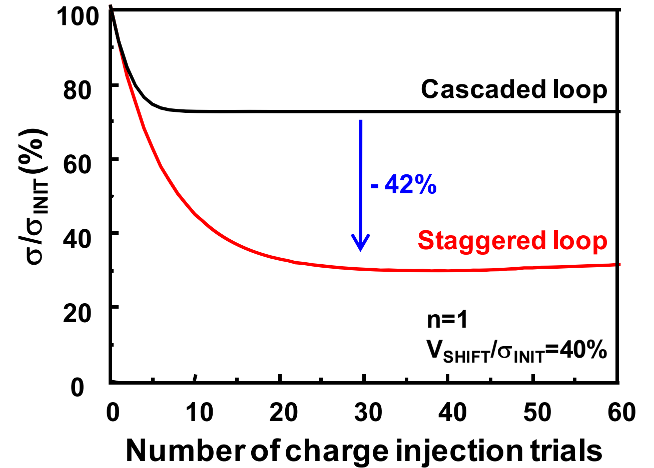


Fig. 6 Simulated dependence of σ/σ_{INIT} on number of charge injection trials of the cascaded loop and the staggered loop at n=1 and V_{SHIFT}/σ_{INIT} =40%.

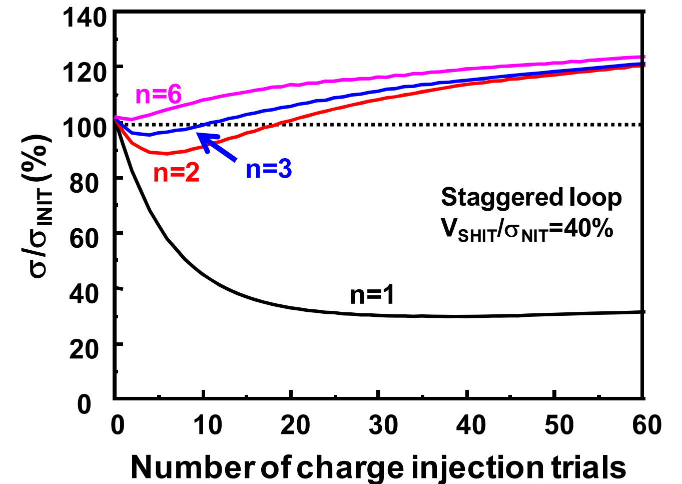
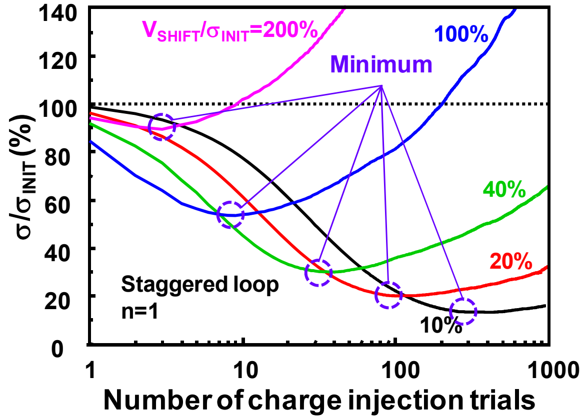
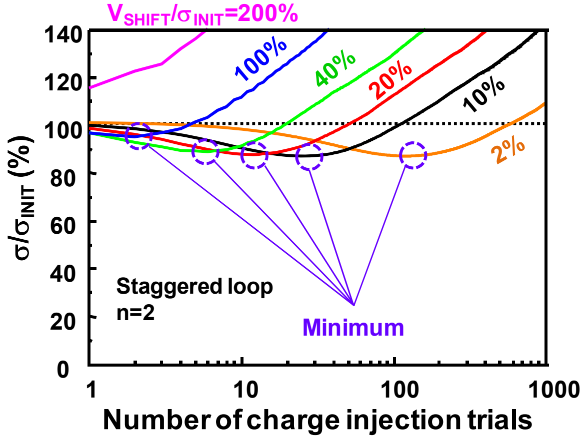


Fig. 7 Simulated dependence of σ/σ_{INIT} on number of charge injection trials with different n at V_{SHIFT}/σ_{INIT} =40%.



(a)



(b)

Fig. 8 Simulated dependence of σ/σ_{INIT} on number of charge injection trials with different $V_{SHIFT}/\ \sigma_{INIT}$. (a) n=1. (b) n=2.

standard deviation of V_{TH} is defined as σ_{INIT} and σ, respectively. As shown in Fig. 1(c), V_{TH} shift per charge injection is defined as V_{SHIFT} and $V_{SHIFT}/\ \sigma_{INIT}$ =40% is assumed in Fig. 5. The simulation steps to calculate the distributions of V_{TH} using Matlab are: (1) 10k random numbers are generated, (2) the random numbers are divided into groups including 2n numbers, (3) the minimum number in the 2n numbers is selected in each group, and (4) the minimum number and the every other numbers are increased by V_{SHIFT}. In Fig. 5, σ is successfully reduced by increasing m, while average V_{TH} increases by $mV_{SHIFT}/2$. In the proposed charge injection scheme, the average V_{TH} increase is compensated by the forward body bias to nMOS.

Fig. 6 shows the simulated dependence of σ/σ_{INIT} on number of charge injection trials of the cascaded loop and the staggered loop at n=1 and $V_{SHIFT}/\ \sigma_{INIT}$ =40%. The σ/σ_{INIT} of the staggered loop is reduced by 42% compared with that of the cascaded loop, because the cascaded loop can not compensate for an inter-loop mismatch. Therefore, only the staggered loop is used in the rest of this paper.

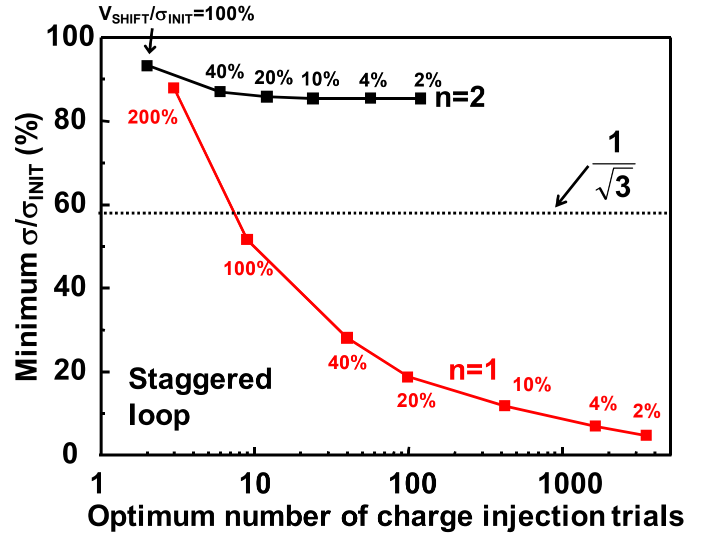


Fig. 9 Simulated dependence of minimum σ/σ_{INIT} on optimum number of charge injection trials with different $V_{SHIFT}/\ \sigma_{INIT}$ at n=1 and n=2.

Fig. 7 shows the simulated dependence of σ/σ_{INIT} on number of charge injection trials with different n at $V_{SHIFT}/\ \sigma_{INIT}$ =40%. The minimum σ/σ_{INIT} at n=1 is 29%, while the minimum σ/σ_{INIT} at n=2, 3, and 6 are 87%, 94%, and 99%, respectively. The large difference between n=1 and 2 is investigated in details. Fig. 8 shows the simulated dependence of σ/σ_{INIT} on number of charge injection trials with different $V_{SHIFT}/\ \sigma_{INIT}$ at n=1 (Fig. 8(a)) and n=2 (Fig. 8(b)). In order to clarify the difference between n=1 and 2, the minimum σ/σ_{INIT} point is extracted from Fig. 8 and plotted in Fig. 9. Fig. 9 shows the simulated dependence of minimum σ/σ_{INIT} on optimum number of charge injection trials with different $V_{SHIFT}/\ \sigma_{INIT}$ at n=1 and n=2. The minimum σ/σ_{INIT} reduces with decreasing V_{SHIFT} at n=1. The minimum σ/σ_{INIT} is 6.2% at $V_{SHIFT}/\ \sigma_{INIT}$ = 2%, while the optimum number of charge injection trials is 3515, which is not practical because large number of charge injection trials increases the pre-shipment test cost. Therefore, The minimum σ/σ_{INIT} of 52% at $V_{SHIFT}/\ \sigma_{INIT}$ = 100% and the number of trials of 9 or the minimum σ/σ_{INIT} of 29% at $V_{SHIFT}/\ \sigma_{INIT}$ = 40% and the number of trials of 40 will be a practical choice. In contrast, at n=2, the minimum σ/σ_{INIT} is more than 80% even if $V_{SHIFT}/\ \sigma_{INIT}$ is 2%, because the mismatch within each loop is not completely compensated at n=2. Therefore, n=1 is used in the rest of this paper.

IV. MEASUREMENT RESULTS

The proposed automatically selective charge injection scheme is verified with measurements. Fig. 10 shows measured dependence of drain current on gate voltage of nMOS transistor in 1.2V 65nm CMOS process before and after the charge injection by SHE. ΔV_{TH} of 36mV was obtained at the charge injection condition of V_{GS}=3.5V, V_{DS}=0V, V_{pwell}= -7V, and 5 min.

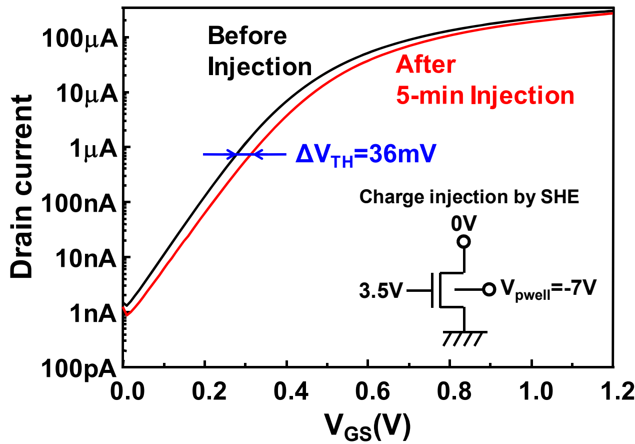


Fig. 10 Measured dependence of drain current on gate voltage of nMOS transistor of 1.2V 65nm CMOS process before and after the charge injection by SHE.

Fig. 11 shows a schematic of a fabricated 96-stage inverter chain with the staggered loop. When both ϕ_1 and ϕ_2 are "H", the circuit operates in the normal logic operation mode as shown in Fig. 4(a). When ϕ_1 is "H" and ϕ_2 is "L", the circuit operates in the odd-loop latch mode as shown in Fig. 4(b). When ϕ_1 is "L" and ϕ_2 is "H", the circuit operates in the even-loop latch mode as shown in Fig. 4(c). The charge injection is applied at V_{DD}=3.2V, V_{pwell}= -7V, and 1 min per injection. 191 CMOS transfer gates to make the staggered loop are added to original 96 inverters for the chain. Area penalty due to the proposed circuit for the automatically selective charge injection scheme is discussed. The area of the proposed circuit is about three times of that of the original 96-stage inverter chain, because the number of logic gates increase from 96 to 287. According to the Pelgrom plot, σ/σ_{INIT} is reduced to $1/\sqrt{3}$ (= 0.58) by tripling the transistor area. Therefore, the proposed charge injection scheme makes sense when σ/σ_{INIT} is less than $1/\sqrt{3}$. As shown in Fig. 9, σ/σ_{INIT} less than $1/\sqrt{3}$ is achieved at the optimum number of charge injection trials larger than 9. Thus, the proposed charge injection scheme is more effective in reducing σ than simply increasing the transistor area.

The chip micrograph and core layout of the 96-stage inverter chain shown in Fig. 11 are shown in Fig. 12. The test chip was implemented in 1.2V 65-nm CMOS process. The size of core is 32μm by 8μm.

Fig. 13 shows measured dependence of V_{DDmin} of the inverter chain shown in Fig. 11 on V_{pwell}. The number of charge injection trials is varied. Charge injection trials of odd-loop latch mode and even-loop latch mode are performed alternately. V_{DDmin} is defined as the minimum operating V_{DD} whether 1-Hz rectangular wave is observed or not from the output of the inverter chain. To compensate for the global variation between pMOS and nMOS, V_{pwell} is tuned to find the minimum V_{DDmin}. V_{pwell} of the minimum V_{DDmin} is increased as the numbers of trials increases, because the average V_{TH} of nMOS is increased.

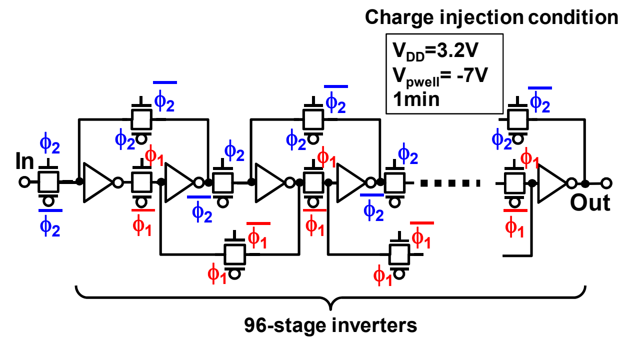


Fig. 11 Fabricated 96-stage inverter chain with the staggered loop. 191 CMOS transfer gates are added to original 96 inverters for the chain.

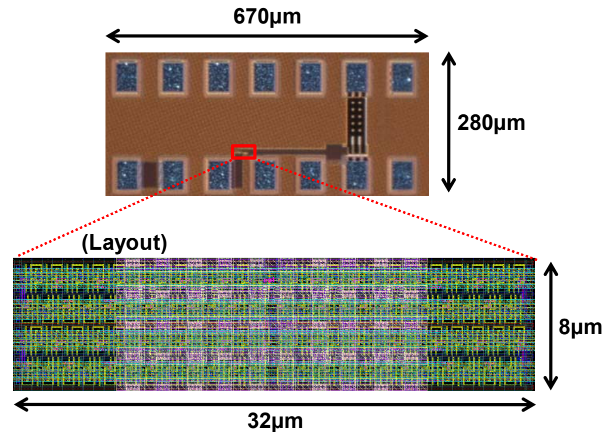


Fig. 12 The chip micrograph and core area layout of the 96-stage inverter chain.

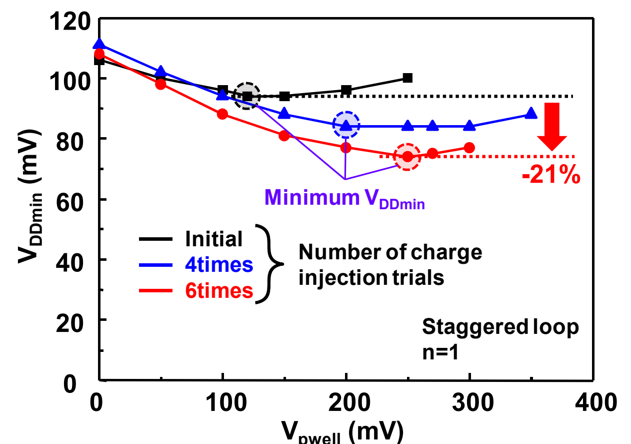


Fig. 13 Measured V_{DDmin} of the inverter chain with various number of charge injection trials.

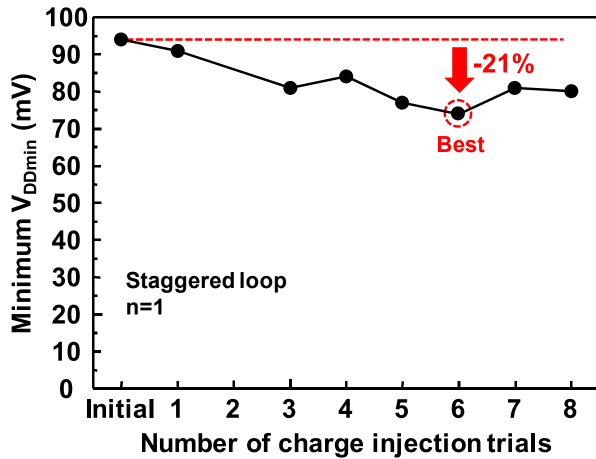


Fig. 14 Measured dependence of minimum V_{DDmin} on number of charge injection trials. The minimum V_{DDmin} points are extracted from Fig. 13.

In order to clarify the trend of the minimum V_{DDmin}, the minimum V_{DDmin} point is extracted from Fig. 13 and plotted in Fig. 14. In Fig. 13, all the measured points are not shown for simplicity. Fig. 14 shows the measured dependence of minimum V_{DDmin} on number of charge injection trials. The minimum V_{DDmin} is the lowest at 6-time charge injection trials. The initial minimum V_{DDmin} is 94mV when V_{pwell} is 120mV. After 6-time charge injection trials, the minimum V_{DDmin} is 74mV when V_{pwell} is 250mV. Therefore, V_{DDmin} is reduced by 21% from 94mV to 74mV.

V. Conclusion

In order to reduce minimum operating voltage (V_{DDmin}) of CMOS logic circuits, a new method to reducing the within-die random threshold (V_{TH}) variation of transistors by the post-fabrication automatically selective charge injection using substrate hot electrons (SHE) is proposed along with novel circuitry to utilize this. The charge injection could be performed at pre-shipment test. The circuit with the staggered loop topology and n=1 is the best implementation for the automatically selective charge injection scheme. The minimum σ/σ_{INIT} of 29% at V_{SHIFT}/σ_{INIT} = 40% and the number of trials of 40 is one of a practical design choices. By applying the proposed scheme to 96-stage inverter chain fabricated in 65-nm CMOS, the measured V_{DDmin} is successfully reduced by 21% from 94mV to 74mV.

Acknowledgment

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References

[1] J. Kwong, Y. Ramadass, N. Verma, M. Koesler, K. Huber, H. Moormann, and A. Chandrakasan, “A 65 nm sub-Vt microcontroller with integrated SRAM and switched capacitor DC-DC converter,” IEEE J. Solid-State Circuits, vol. 44, pp. 115-126, Jan. 2009.

[2] Y. Pu, J.P. Gyvez, H. Corporaal, and H. Yajun, “An ultra-low-energy/frame multi-standard JPEG co-processor in 65nm CMOS with sub/near-threshold power supply,” International Solid-State Circuits Conference (ISSCC), pp. 146-147, Feb. 2009.

[3] A. Agarwal, S.K. Mathew, S.K. Hsu, M.A. Anders, H. Kaul, F. Sheikh, R. Ramanarayanan, S. Srinivasan, R. Krishnamurthy, and S. Borkar, “A 320mV-to-1.2V on-die fine-grained reconfigurable fabric for DSP/media accelerators in 32nm CMOS,” International Solid-State Circuits Conference (ISSCC), pp. 328-329, Feb. 2010.

[4] N. Lotze and Y. Manoli, “A 62mV 0.13µm CMOS standard-cell-based design technique using schmitt-trigger logic,” International Solid-State Circuits Conference (ISSCC), pp. 340-341, Feb. 2011.

[5] M. Seok, D. Jeon, C. Chakrabarti, D. Blaauw, and D. Sylvester, “A 0.27V 30MHz 17.7nJ/transform 1024-pt complex FFT core with super-pipelining,” International Solid-State Circuits Conference (ISSCC), pp. 342-343, Feb. 2011.

[6] T. Niiyama, P. Zhe, K. Ishida, M. Murakata, M. Takamiya, and T. Sakurai, “Increasing minimum operating voltage (VDDmin) with number of CMOS logic gates and experimental verification with up to 1Mega-stage ring oscillators,” International Symposium on Low Power Electronics and Design (ISLPED), pp. 117-122, Aug. 2008.

[7] M. Suzuki, T. Saraya, K. Shimizu, T. Sakurai, and T. Hiramoto, “Post-fabrication self-convergence scheme for suppressing variability in SRAM cells and logic transistors,” IEEE Symposium on VLSI Technology, pp.148-149, June, 2009.

[8] J. Wang, S. Nalam, Z. Qi, R. Mann, M. Stan, and B. Calhoum, “Improving SRAM Vmin and yield by using variation-aware BTI stress,” IEEE Custom Integrated Circuits Conference (CICC), pp. 5-8, Sep, 2010.

[9] H. Fuketa, S. Iida, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, “A closed-form expression for estimating minimum operating voltage (V_{DDmin}) of CMOS logic gates,” ACM Design Automation Conference, Session 53.1, June 2011.