12.1 A 95mV-Startup Step-Up Converter with V_{TH}-Tuned Oscillator by Fixed-Charge Programming and Capacitor Pass-On Scheme

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Harvesting energy from the environment by using a thermoelectric generator (TEG) or photovoltaic cells provides a solution for battery-free sensor networks or electronic healthcare systems. In these systems, the harvested energy is supplied at a very low voltages, requiring a low-startup-voltage power circuit for kick-start from low voltage. A previous sub-100mV-startup-voltage boost converter [1] was implemented by using a mechanically assisted step-up process that needs vibration at startup and the application is rather limited. In this paper, a 95mV startup voltage step-up converter without any mechanical stimulus extends the applicability of energy harvesting. The circuit converts a 100mV input to a 0.9V output with 72% conversion efficiency without any external clocks or mechanical switches. A capacitor pass-on scheme eliminates an additional external output capacitor that functions only at the startup.

The minimum startup voltage of a step-up DC-DC converter in standard CMOS technology is limited by the oscillator since a clock signal is required for a charge pump (CP). Practically, the minimum supply voltage of an oscillator (V_{DDMIN}) is limited by PMOS-NMOS V_{TH} unbalance caused by within-die and die-to-die V_{TH} variations. The within-die V_{TH} variation issue can be solved by increasing the channel width and thus it is easily solved in this application. The problem is the die-to-die variation, which can usually be adjusted by controlling the body bias of the MOSFET. In the startup circuit, however, the body-biasing circuit is not functional since the body-biasing circuit needs another oscillator, which does not function below V_{DDMIN}. To solve this problem, post-fabrication V_{TH} programming is applied to the oscillator.

Figure 12.1.1 compares the conventional and our step-up converter architectures. In the conventional approach, two external capacitors are required. One (C_{OUT1}) is used in the charge-pumping startup circuit and the other (C_{OUT2}) is for the boost converter. C_{OUT1} is needed to separate the boost converter from the CP at the start-up. Otherwise the start-up CP needs to drive the boost converter control circuit, which is seen as leakage current (I_{Leak}) for the CP. In our scheme, C_{OUT1} is eliminated by using the output capacitor of the booster, C_{OUT2}, as the charge buffer of the CP as shown in Fig. 12.1.1(b). Once the C_{OUT} is charged without leakage, C_{OUT} is "passed on" with its charge inside to the boost converter. By doing so, the large external capacitor of C_{OUT1} is eliminated.

The detailed block diagram of the proposed step-up converter and the timing chart are shown in Fig. 12.1.2. The capacitor pass-on controller contains a CP for PMOS super cut-off (PSC) and two voltage detectors D1 and D2. The CP for PSC provides the overdrive voltage to the gate of PMOS switch and reduces the leakage current. At startup, C_{OUT} is charged by the CP and V_{START} rises. When V_{CP1} (=V_{START}) is pumped to the preset trip voltage of D1, the node Y changes from low to high to pass on the C_{OUT} to the boost converter and C_{OUT} becomes the output capacitor of the boost converter. The charge stored in C_{OUT} activates the clock generator for the boost converter and start driving the boost converter. If the load is connected at the same time when the capacitor is passed on, the charge stored in C_{OUT} drains out and boost converter fails to start up. To overcome this problem, a voltage detector D2 with 60mV higher trigger voltage comparing to D1 is added to delay the load connection timing a bit. This ensures the output switch M2 to turn on after the boost converter starts working and the output is boosted smoothly.

Since the detector D1 has to be connected to C_{OUT} at startup, it acts as the load of the CP. Thus the power consumption of the detectors should be minimized. The circuit schematic of the voltage detector and its simulated waveforms are shown in Fig. 12.1.3. It consumes less than 1.6nW when $V_{SENSE} < V_{Trigger}$. To reduce the power consumption, the gate of M_{D3} is connected to its source and only off-current flows. V_{DETECT} changes sharply from low to high when drain current of M_{D1} and M_{D2} get larger than off-current of M_{D3} exponentially. The trigger voltage can be written as (1) in Fig. 12.1.3, which can be tuned by designing the size of M_{D2} and M_{D3}. M_{D1} is applied to almost double the trigger voltage without using unreasonable size ratio of M_{D2} and M_{D3}.

To make sure the circuit functions even under the die-to-die process variation, the V_{TH} of transistors in the ring oscillator, which generates the CP clocks, are trimmed by fixed-charge programming, as shown in Fig. 12.1.4. The upper part shows the detailed circuit schematic when post-fabrication V_{TH} programming is in progress. Since the V_{TH} of NMOS, V_{TN}, was higher than that of PMOS, V_{TP}, in the measured chips, V_{TP} is increased to reduce the V_{DDMIN} of the oscillator here. The V_{TP} is programmed by applying the high reverse body bias to all PMOSFETs (V_{NWELL}=8.5V, V_{PWELL}=0) when the ring oscillator is oscillating under 1V power supply. If V_{TN} programming is required, the high reverse voltage to V_{PWELL} and 1V supply to V_{NWEL} can be applied. In the PMOS programming, holes are injected into the gate oxide and the fixed charge changes V_{TP}. To verify V_{DDMIN} improvement by this post-fabrication V_{TH}-trimming, three test chips of 15-stage ring oscillators are measured. Figures 12.1.4(b) and 12.1.4(c) show V_{DDMIN} change under stress and after stress. V_{DDMIN} is improved (decreased) by 34% compared with the initial value. In Fig. 12.1.4(c), the measured dependence of V_{DDMIN} after stress is shown. The change is as small as 1mV after 3 days of stress and gets stable.

The step-up converter containing the startup circuit with V_{TH}-trimmed oscillator is realized in 65nm CMOS technology. The chip micrograph is shown in Fig. 12.1.7 with 0.17mm^2 active area. Fig. 12.1.5(a) shows measured waveforms of the step-up converter with the capacitor pass-on mechanism. The circuit is measured under 95mV input voltage without any external clocks or mechanical switches. The CP for startup pumps up the 10nF external capacitor C_{OUT} and passes on the capacitor to the boost converter after 262ms. The power efficiency versus the current delivered to the load under 100mV input is shown in Fig. 12.1.5(b). It provides maximum efficiency of 72% at 1.5mA output current with 0.9V output voltage.

The performance comparison between our circuit and the state-of-the-art step-up converters applying startup mechanism is shown in Fig. 12.1.6. The proposed circuit achieves the lowest startup voltage except for reference [1]. which requires mechanical vibration to assist the startup. The proposed circuit also demonstrates the feasibility of countermeasures for the process variation that limits the minimum startup voltage of an on-chip ring oscillator.

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This work was carried out as a part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO).

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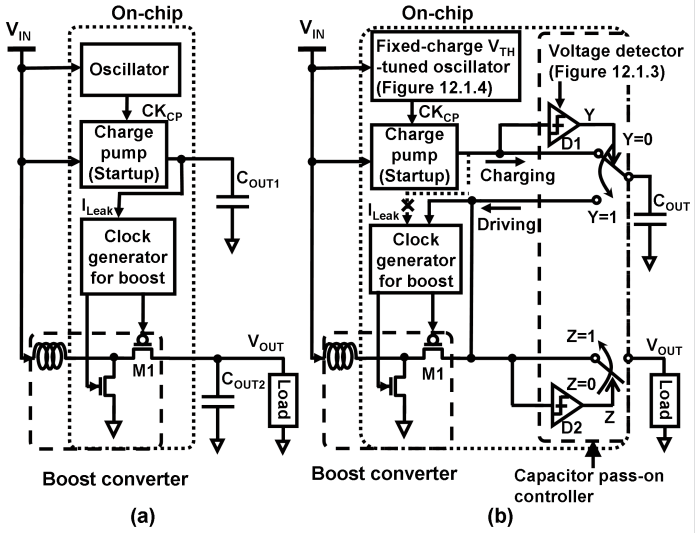

Figure 12.1.1: The system architecture of (a) the conventional and (b) the proposed startup mechanism in step-up DC-DC converter.

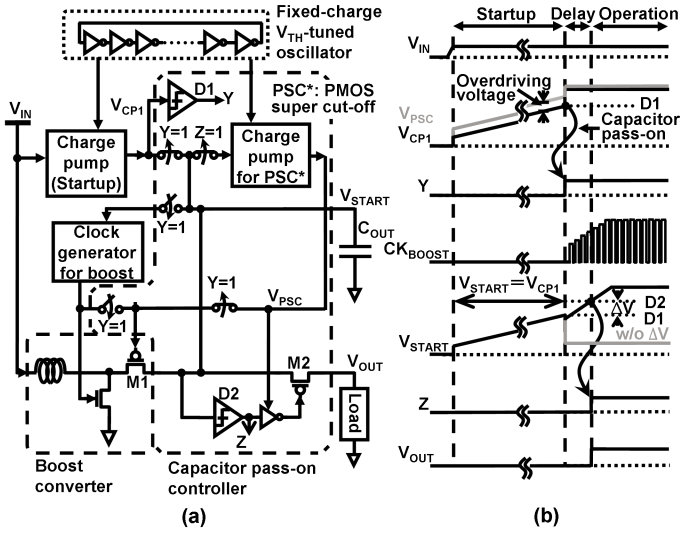

Figure 12.1.2: (a) The detailed block diagram of the proposed step-up converter. (b) Timing chart illustrating the circuit operation sequences.

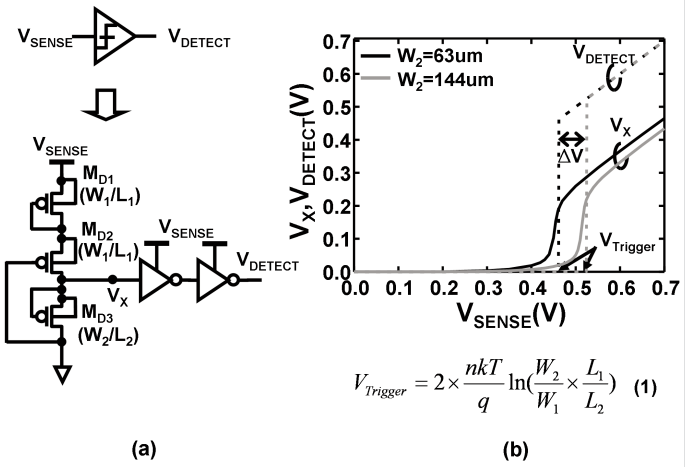

Figure 12.1.3: (a) Circuit schematic of 1.6-nW voltage detector (b) Simulated waveforms of the proposed voltage detector.

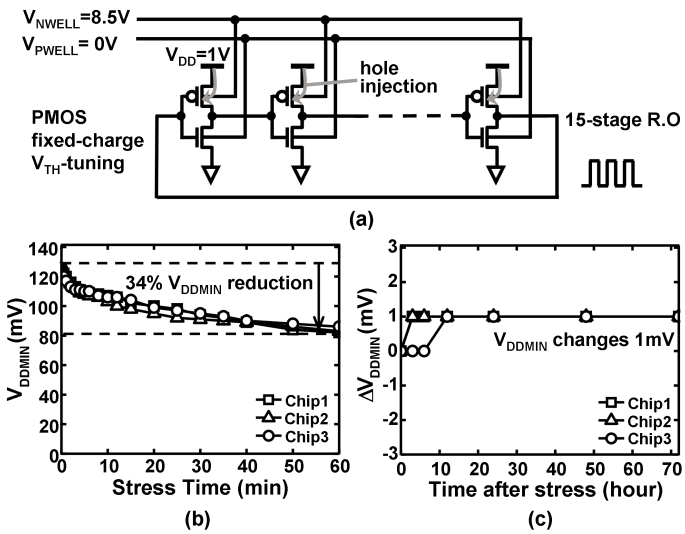

Figure 12.1.4: (a) Circuit schematic of V_{TH}-tuned oscillator. (b) Measured V_{DDMIN} change under stress. (c) Measured V_{DDMIN} change after stress.

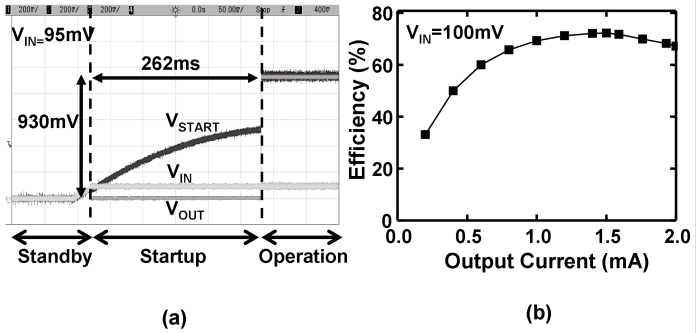

Figure 12.1.5: (a) Measured startup waveforms of the proposed step-up converter. (b) Measured conversion efficiency versus output current.

	Startup mechanism	Min. Startup Voltage	Typical Input Voltage (V_{IN})	Output Voltage @V_{IN}	Peak Efficiency @V_{IN}	Process
[1]	Mechanical switch	35mV	50mV	1.8V	58%	350-nm CMOS
[2]	External Voltage	650mV	100mV	1V	75%	130-nm CMOS
[3]	Charge pump	180mV	180mV	0.74V	N/A	65-nm CMOS
[4]	Charge pump	360mV	500mV	7V	82%	350-nm SOI-BCD
This Work	Charge pump with V_{TH}–tuned oscillator	95mV	100mV	0.9V	72%	65-nm CMOS

Figure 12.1.6: Comparison of recently published step-up converter applying startup mechanism.

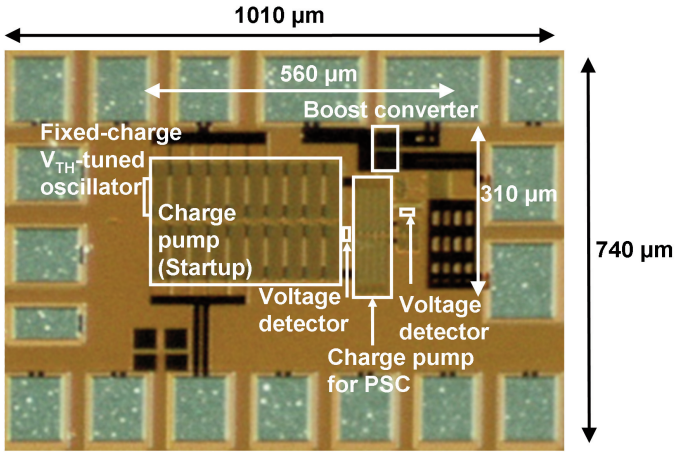

Figure 12.1.7: Chip micrograph of the proposed step-up converter.

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