12% Power Reduction by Within-Functional-Block Fine-Grained Adaptive Dual Supply Voltage Control in Logic Circuits with 42 Voltage Domains

Atsushi Muramatsu*, Tadashi Yasufuku†, Masahiro Nomura*, Makoto Takamiya†,
Hirofumi Shinohara* and Takayasu Sakurai†
*Semiconductor Technology Academic Research Center, Japan
†University of Tokyo, Japan

***Abstract*— Within-functional-block fine-grained adaptive dual supply voltage control (FADVC) is proposed to reduce the power of CMOS logic circuits. Both process and design variations within a functional block are compensated by the fine-grained supply voltage (V_{DD}) control to minimize power at fixed clock frequency. In the 40-nm test chips, the layout of a data encryption core is divided into 6x7 voltage domains. Both high V_{DD} (V_{DDH}) and low V_{DD} (V_{DDL}) are supplied to each power domain and either V_{DDH} or V_{DDL} is adaptively selected according to the setup error warning signals generated by canary flip-flops. Compared with the conventional single V_{DD} operation, the proposed FADVC reduced the power by 12% at 1-MHz clock in the measurement.**

I. Introduction

Adaptive voltage control (AVC) is an important scheme to reduce the power consumption of a system-on-chip (SoC). Fig. 1 shows a block diagram of a conventional core-by-core AVS [1]. The power supply voltage (V_{DD}) is adaptively controlled according to a timing error warning signal. Conventional AVC schemes, however, do not take into account within-die (WID) process variation. Eireiner et al. [2] proposed an AVC scheme with a timing error detector such as Razor flip-flops [3]. Their proposal can detect timing error caused by WID variation. But this method can not control supply voltage optimally, because this method changes not only supply voltage of error path but also that of the entire core.

To achieve an extremely low-power operation, reducing V_{DD} to the threshold voltage is effective. The delay variation due to random transistor variation, however, increases at low V_{DD}. For example, Gammie et al. [4] discussed the delay of standard library cells in 28-nm CMOS process. The delay distribution due to WID variation at 0.5V is 15 times larger than that at 1.0V.

Previous work [5] proposed a method of AVC which cancels the WID variation. In their proposal, the original logic block is transformed into low voltage parallel blocks. V_{DD} is independently controlled in each block. However, the original circuits need to be divided into parallel blocks at system-level design. This means the most fine-grained block of AVC is one function block. When a chip has large random logic blocks that cannot be separated into small blocks, the logic block must be placed into one power domain.

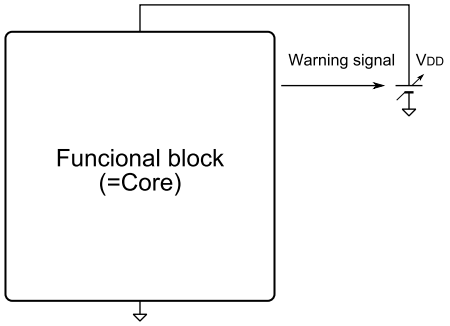

Fig. 1. Conventional adaptive voltage control (AVC).

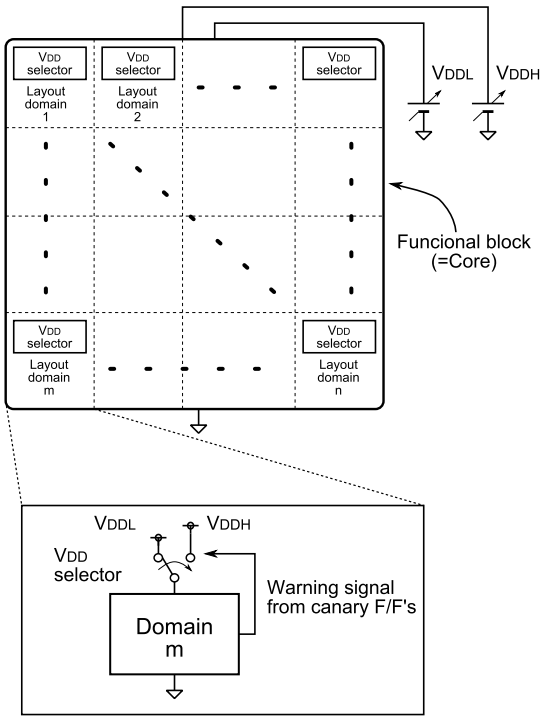

Fig. 2. Proposed within-functional-block fine-grained adaptive dual supply voltage control (FADVC)

978-1-4577-0704-9/11/$26.00 ©2011 IEEE

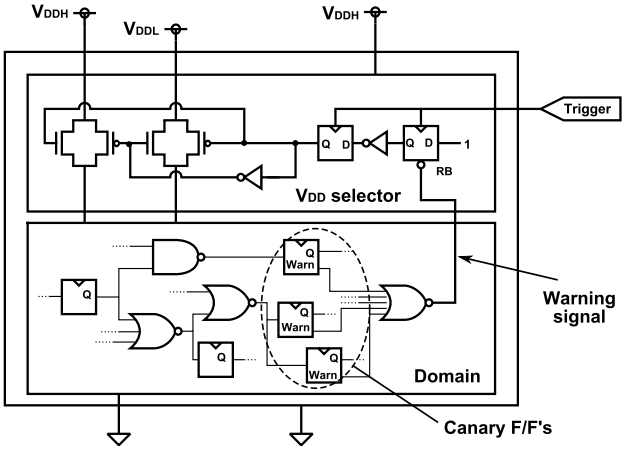

Fig. 3. Circuit schematic of each domain in FADVC.

In order to reduce the power consumption by compensating the systematic design variation, Nakamura et al. [6] proposed a within-functional-block fine-grained body-bias control. In their works, a chip is divided into 8 body-bias domains and each body-bias is optimized to minimize the power consumption at a fixed clock frequency with a simulated-annealing algorithm. This post-fabrication tuning approach can reduce the leakage power, but can not reduce the dynamic power. And the body-bias optimization requires more than 20 functional test loops, thereby increasing the test cost. In order to reduce the power by compensating the systematic design variation and WID variation without increasing the test cost, within-functional-block fine-grained adaptive dual supply voltage control (FADVC) is proposed in this paper.

II. Proposed Within-Functional-Block Fine-Grained Adaptive Dual Supply Voltage Control (FADVC)

Fig. 2 shows a block diagram of the proposed FADVC. In FADVC, the layout of a functional logic block including clock distribution networks is divided into many square tiles (= domains) by using a standard place-and-route tool. In our implementation, data encryption circuits using the Date Encryption Standard (DES) algorithm is embedded as the functional logic block. The area of each tile is around $100 \times 100\mu\mathrm{m}^2$.

Fig. 3 shows a circuit schematic of each domain in FADVC. At each domain, either high V_{DD} (V_{DDH}) or low V_{DD} (V_{DDL}) is supplied by a V_{DD} selector. Each domain includes canary flip-flops (F/F's) [7] in order to generate setup error warning signals and the warning signals is delivered to the V_{DD} selector of each domain. At first, V_{DDL} is selected in all domains. When a warnings signal is generated, V_{DD} of the warning domain is switched from V_{DDL} to V_{DDH} to correct the setup error. In contrast, when no warning signal is generated, V_{DD} remains V_{DDL}. In this way, within-functional-block fine-grained dual V_{DD} control is adaptively achieved by utilizing the canary F/F's and the V_{DD} selectors, thereby reducing the test cost.

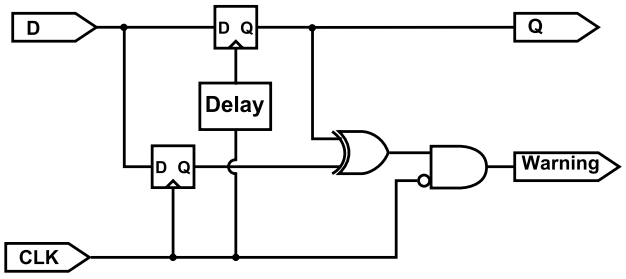

Fig. 4. Circuit schematic of canary F/F.

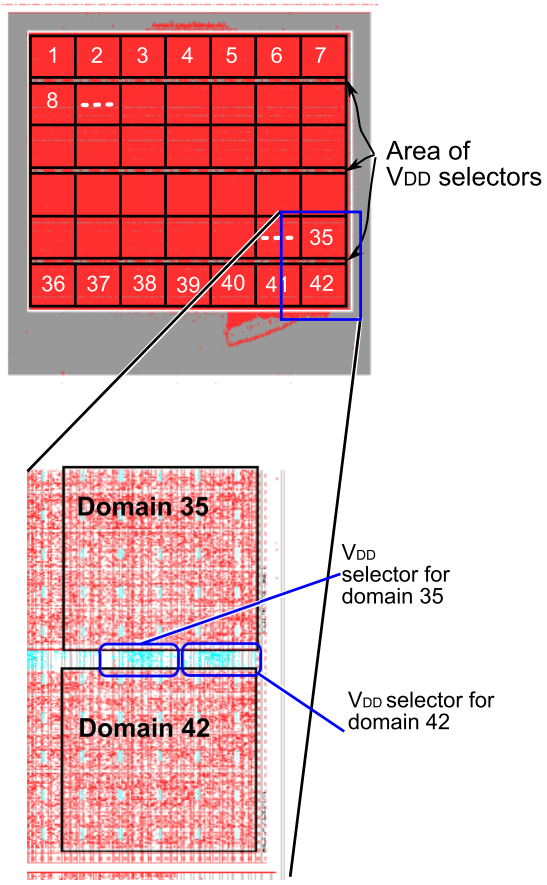

Fig. 5. Layout of fabricated test chip. DES core is divided into 6×7 voltage domains.

Fig. 4 shows a circuit schematic of the canary F/F. Canary F/F's are used in top 2k critical paths among 10k paths for detecting the setup error warning. Warning signal pins of each canary F/F are not connected in the placement and the clock tree synthesis stage of the chip design. After the clock tree synthesis, the warning signal pins of each canary F/F are connected to the V_{DD} selectors.

Fig. 5 shows a layout of the fabricated test chip in 40-nm CMOS process. DES core is divided into 6×7 voltage domains. No level-shifters between the 42 voltage domains are inserted. The layout is designed using a standard automatically place-and-route tool. Each tile (=domain) size is $119 \times 113\mu\mathrm{m}^2$ and the supply voltage is selected separately from two voltages

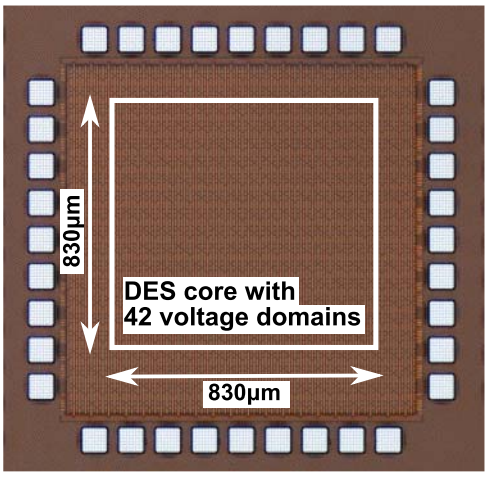

Fig. 6. Microphotograph of test chip in 40-nm CMOS process including a DES core divided into 6×7 voltage domains.

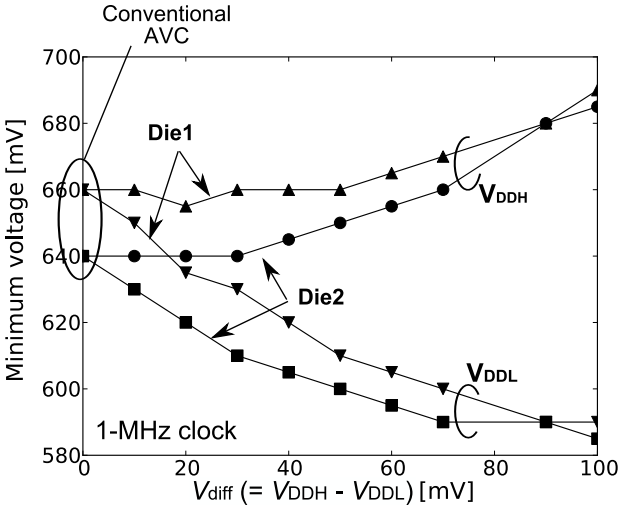

Fig. 7. Measured dependence of minimum supply voltage on $V_{\rm diff}$.

by using the $\rm V_{DD}$ selectors.

The $\rm V_{DD}$ selectors are placed at the side of each domain. The $\rm V_{DD}$ selectors collect warning signals from the canary F/F's and $\rm V_{DDH}$ or $\rm V_{DDL}$ is selected at each domain. The clock signal of the $\rm V_{DD}$ selectors is asynchronous to the DES core circuit. These $\rm V_{DD}$ selectors are placed between each power domains, and the $\rm V_{DD}$ is fixed to $\rm V_{DDH}$. The area overhead by replacing normal F/F's with canary F/F's is 8% and the area overhead due to the $\rm V_{DD}$ selectors is 5%. Therefore, the total area overhead in FADVC is 13%.

Fig. 6 is a microphotograph of a test chip in 40-nm CMOS process including a DES core divided into 6×7 voltage domains. The core size is $830\mu\rm m \times 830\mu m$ and the die size is $1.2\rm mm \times 1.2mm$.

III. Measurement results

In this section, the power reduction factor thanks to the proposed FADVC over the conventional AVS is measured in detail. $V_{\rm diff}$ (=$\rm V_{DDH} - V_{DDL}$) is an important parameter that determines the power reduction in FADVC. The measurement steps are as follows. At first, the warning signals from all the canary F/F's and registers in the $\rm V_{DD}$ selector were reset. Then the DES core circuits operated. When the timing warning signal is generated from the canary F/F's, the warning signals were stored in each $\rm V_{DD}$ selector and $\rm V_{DDH}$ or $\rm V_{DDL}$ is adaptively selected at each domain according the warning signals. Finally, the DES core circuits operated again and we determined whether the output data of the chip were correct or not.

Figs. 7 and 8 show the measured dependence of minimum supply voltage and power consumption on $V_{\rm diff}$, respectively. Two dies are measured to investigate the die-to-die variation. The clock frequency of the DES core was fixed to 1MHz. Both $\rm V_{DDH}$ and $\rm V_{DDL}$ with the difference of $V_{\rm diff}$ were reduced from 700mV to 500mV with a 5-mV step and the function of the DES core was checked at each $\rm V_{DDH}$ and $\rm V_{DDL}$. The minimum functional $\rm V_{DDH}$ and $\rm V_{DDL}$ are shown in Fig. 7. In

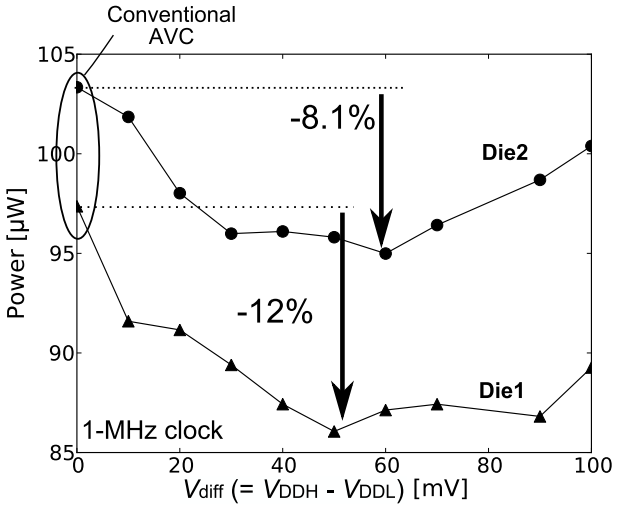

Fig. 8. Measured dependence of power consumption on $V_{\rm diff}$.

Figs. 7 and 8, $V_{\rm diff} = 0$ means the conventional AVC scheme shown in Fig. 1. Fig. 7 shows that proposed FADAC scheme can reduce $\rm V_{DDL}$ compared with the conventional AVC. As $V_{\rm diff}$ is increased in Fig. 8, the power decreases at $V_{\rm diff} <$ 50–60mV while the power increases at $V_{\rm diff} >$ 50–60mV. Therefore, the power is minimum at $V_{\rm diff}$ of 50mV and 60mV in die1 and die2, respectively. In die1, the power is reduced by 12% at $\rm V_{DDH}$ = 660mV and $\rm V_{DDL}$ = 610mV. In die2, the power is reduced by 8.1% at $\rm V_{DDH}$ = 655mV and $\rm V_{DDL}$ = 595mV. The minimum voltages of die 2 is lower than that of die 1, while the power of die 2 is larger than that of die 1. This will be because the threshold voltage of die2 is lower than that of die1 and the leakage power of die2 is larger than that of die1. The power decrease at $V_{\rm diff} <$ 50–60mV derives from the power reduction by reducing $\rm V_{DDL}$. In contrast, the power increase at $V_{\rm diff} >$ 50–60mV derives from the inter-domain

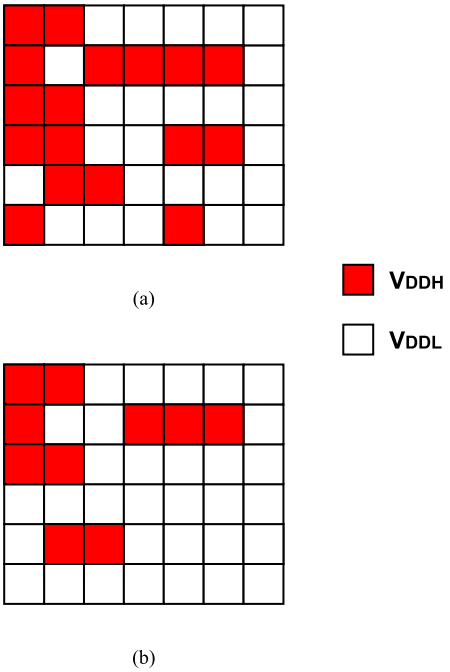

Fig. 9. Measured distributions of V_{DDH} and V_{DDL} among 42 voltage domains at minimum power conditions of (a) die1 and (b) die2.

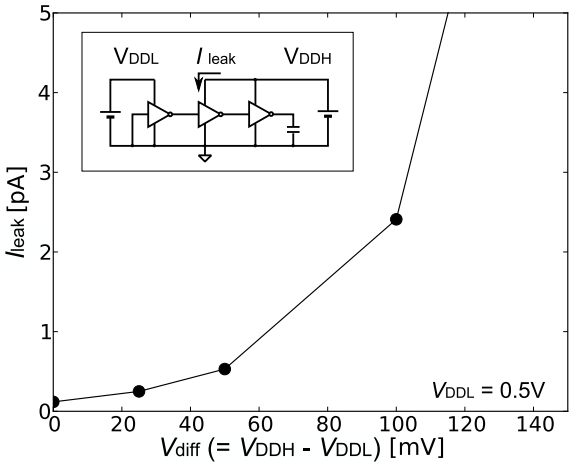

Fig. 10. Simulated dependence of leakage current between two domains with V_{diff} difference.

leakage increase. The inter-domain leakage issue is discussed later in Fig. 10.

Fig. 9 shows measured distributions of V_{DDH} and V_{DDL} among 42 voltage domains at the minimum power conditions of die1 and die2. 10 V_{DDH} domains of die2 is included in 17 V_{DDH} domains of die1. The 10 common domains will derive from the systematic design variation and the 7 non-common domains will derive from die-to-die and WID process variation.

Finally, the inter-domain leakage issue in FADVC is discussed. In the implementation of FADVC, no level-shifters between the 42 voltage domains are inserted, because the power, delay, and area overhead of the level-shifters is large in the fine-grained voltage control. The inter-domain leakage issue, however, increases the total power when V_{diff} is large. In order to quantitatively check the inter-domain leakage, Fig. 10 shows the SPICE simulated dependence of leakage current between two domains with V_{diff} difference. V_{diff} less than 50mV will be a practical design choice, because the leakage current rapidly increases as V_{diff} is increased.

IV. Conclusion

FADVC is proposed to reduce the power of CMOS logic circuits. Both process and design variations within a functional block are compensated by the fine-grained supply voltage (V_{DD}) control to minimize power at fixed clock frequency. In the fabricated test chips in 40-nm CMOS process, layout of a data encryption core is divided into 6x7 voltage domains. Both high V_{DD} (V_{DDH}) and low V_{DD} (V_{DDL}) are supplied to each power domain and either V_{DDH} or V_{DDL} is adaptively selected according to the setup error warning signals generated by canary flip-flops. The total area overhead in FADVC is 13%. Compared with the conventional single V_{DD} operation, the proposed FADVC reduced the power by 12% at V_{DDH} = 660mV, V_{DDL} = 610mV, and 1-MHz clock.

Acknowledgments

This work was carried out as a part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO).

References

[1] S. Dighe, S. Vangal, P. Aseron, S. Kumar, T. Jacob, K. Bowman, J. Howard, J. Tschanz, V. Erraguntla, N. Borkar, V. De and S. Borkar, "Within-Die Variation-Aware Dynamic-Voltage-Frequency Scaling Core Mapping and Thread Hopping for an 80-Core Processor," *International Solid-State Circuits Conference*, pp. 174–175, Feb. 2010.

[2] M. Eireiner, S. .Henzler, G. Georgakos, J. Berthold and D. Schmitt-Landsiedel, "In-Situ Delay Characterization and Local Supply Voltage Adjustment for Compensation of Local Parametric Variation," *IEEE Journal of Solid-State Circuits*, pp. 1583–1592, Jul. 2007.

[3] D. Blaauw, S. Kalaiselvan, K. Lai, W.-H. Ma, S. Pant, C. Tokunaga, S. Das and D. Bull, "Razor II: In Situ Error Detection and Correction for PVT and SER Tolerance," *International Solid-State Circuits Conference*, pp. 400–401, Feb. 2008.

[4] G. Gammie, N. Ickes, M. E. Sinangil, R. Rithe, J. Gu, A. Wang, H. Mair, S. Datla, B. Rong, S. Honnavara-Prasad, L. Ho, G. Baldwin, D. Buss, A. P. Chandrakasan and U. Ko, "A 28nm 0.6V Low-Power DSP for Mobile Applications," *International Solid-State Circuits Conference*, pp. 132–133, Feb. 2011.

[5] N. Azizi, M. M. Khellah, V. K. De and F. N. Najm, "Variations-Aware Low-Power Design and Block Clustering with Voltage Scaling," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, pp.746–757, Jul. 2007.

[6] Y. Nakamura, D. Levacq, L. Xiao, T. Minakawa, T. Niiyama, M. Takamiya and T. Sakurai, "1/5 Power Reduction by Global Optimization based on Fine-Grained Body Biasing," *Proc. Custom Integrated Circuits Conference*, pp.547–550, Sep. 2008.

[7] T. Sato and Y. Kunitake, "A Simple Flip-Flop Circuit for Typical-Case Designs for DFM," *Proc. 8th International Symposium on Quality Electronic Design*, pp.539–554, 2007.