Capacitively Coupled Non-Contact Probing Circuits for Membrane-Based Wafer-Level Simultaneous Testing

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***Abstract*—A capacitively coupled probing circuit with a novel de-skewer, a low-pass filter and a high-sensitivity receiver is proposed to realize a membrane-based wafer-level simultaneous testing robustly. The de-skewer can be designed by only digital core transistors and has stable feed-forward architecture. The receiver with the low-pass filter can suppress the undesirable ringing caused by the complex wiring structure in the probe card. A probe chip and a 300 mm DUT-wafer are fabricated in a 1.2 V 90 nm technology and the measured power consumption of RX core is 0.5 mW at 1 Gbps operation. The BER is improved below 10^{-12} over almost all UI range when the de-skewing function is turned on.**

***Index Terms*—Wafer test, capacitive coupling, crosstalk, receiver, de-skewer.**

I. Introduction

THE development of three-dimensional system in package (3D-SiP) technologies has been accelerated to improve the LSI performance. In the 3D-SiP, many dies are stacked and if the yield of die is low, the yield of 3D-SiP falls dramatically. Thus it is important to obtain the Known Good Die (KGD) effectively. Wafer-level simultaneous testing (WLST) where all chips on a wafer are tested and burned in at the same time is preferable in reducing the cost of selecting KGDs. At present, however, it is difficult to realize the WLST because a huge load is required for the stable contact of all test pins on the wafer. Recently, a low-cost membrane-based wafer-level testing technique has been disclosed which makes use of the atmospheric pressure and 700 kg of force can be uniformly distributed over a 300 mm wafer [1]. Yet, assuming that one bump needs 4 g of force to make a stable contact, the probing equipment has to distribute 1.2 ton of force over the 300 mm wafer uniformly as shown in Fig. 1. One promising technique to reduce the required load from 1.2 ton to 700 kg is the combination use of the contacting bumps for power supply and the non-contact interfaces such as the capacitively coupled interfaces (CCIs) [2]–[6], the inductively coupled interfaces (ICIs) [7]–[9] and the RF interfaces (RFIs) [10]–[12] for digital pins. Non-contact probing techniques for the WLST [7], [11], [12] have been proposed, but they are costly because they need probing chips built specific to a certain product.

In this paper, we propose the capacitively coupled non-contact probing circuit for the low-cost membrane-based WLST. Section II compares the non-contact interfaces for the WLST and discusses the effect of cross talk. Section III describes the proposed WLST with the CCI. Section IV explains the novel de-skewer and shows simulation results. Section V presents the details of the receiver circuit. Section VI summarizes experimental results, and Section VII concludes the paper.

II. Non-Contact Interfaces for WLST

Fig. 2 compares non-contact interfaces for the WLST. The required number of pads per channel is two for the ICI, and one for the RFI and the CCI. Considering the interconnect congestion in the probe card and the pad-limited nature of the chip, the RFI and the ICI are prohibitive. This situation also hinders the use of differential signaling [5]. Although the RFI and the ICI can be implemented in the chip, they need probing chips built specific to a certain product and cannot be adopted for the low-cost WLST.

The CCI has the advantage of being able to use the bonding pads for a part of the non-contact interface and a coupling pad can be made by just a metal plate, so a fine process is not needed. On the other hand, the RFI and the ICI require special antennas and coils, respectively. These facts also indicate that the area overhead of the CCI in the device-under-test (DUT) will be nil when the TX and RX can be made under the bonding pads, but the RFI and the ICI need extra footprints for a pair of TX and RX, e.g., 0.13 mm^2 [10] and 0.03 mm^2 [8], because they require special antennas and coils, respectively.

All interfaces have achieved the data rate over 1 Gbps, which is sufficient to cover the at-speed test for most of the next-generation SoC's for mobile and/or consumer digital applications.

The only disadvantage of the CCI is its short transmission distance. In the proposed WLST, however, the distance between the pads is almost zero as described in Section III, so the transmission distance does not become a problem. Moreover, the almost-zero-distance pads make the CCI tolerant to cross talk.

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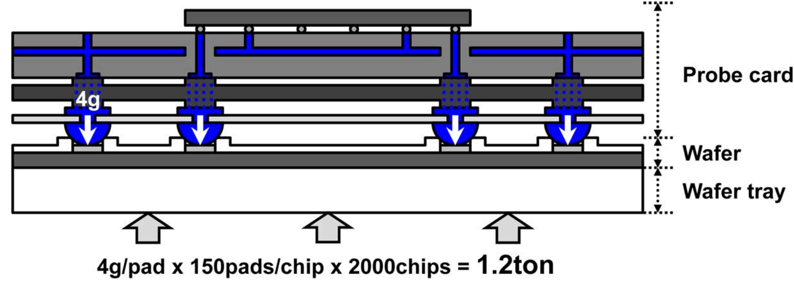


Fig. 1. Conventional membrane-based wafer-level testing technique.

	RF	Inductive	Capacitive
# of pads / channel	1	2	1
Bonding pad sharing	No	No	Yes
Fine process requirement	Yes	Yes	No
Area Overhead in DUT	~0.13mm^2	~0.03mm^2	~0mm^2
Data Rate	> 1Gbps	> 1Gbps	> 1Gbps
Transmission distance	< 100mm	< 100µm	< 10µm

Fig. 2. Comparison of non-contact interfaces.

Fig. 3(a) illustrates the simplified interface models of the ICI and the CCI. The parameter d is the coupling distance between the interfaces which have the base length L and the height h. The parameter s is the separation distance between adjacent interfaces. In the ICI, assuming only the magnetic field coupling for simplicity, the signal transfer S21 and the cross talk S31 and S41 are approximated as

$$S21 \approx \frac{2N_1N_2L^2\mu}{Z_1}\frac{1}{\pi\sqrt{(L/2)^2+d^2}}f \tag{1}$$

$$S31 \approx \frac{N_1N_3L^2\mu}{Z_1}\frac{1}{2\pi(L/2+\mathrm{s})}f \tag{2}$$

$$S41 \approx \frac{N_1N_4L^2\mu}{Z_1}\frac{1}{2\pi\sqrt{d^2+(L/2+s)^2}}f \tag{3}$$

where N_1, N_2, N_3 and N_4 are the number of turns, Z_1 is the output impedance and f is the transmission signal frequency. In the CCI, assuming that the parasitic capacitance C_P is much larger than the coupling capacitance, the signal transfer S21 and the cross talk S31 and S41 are approximated as

$$S21 \approx \frac{1}{C_P}\varepsilon\frac{L^2}{d} \tag{4}$$

$$S31 \approx \frac{1}{C_P}\varepsilon\frac{Lh}{s} \tag{5}$$

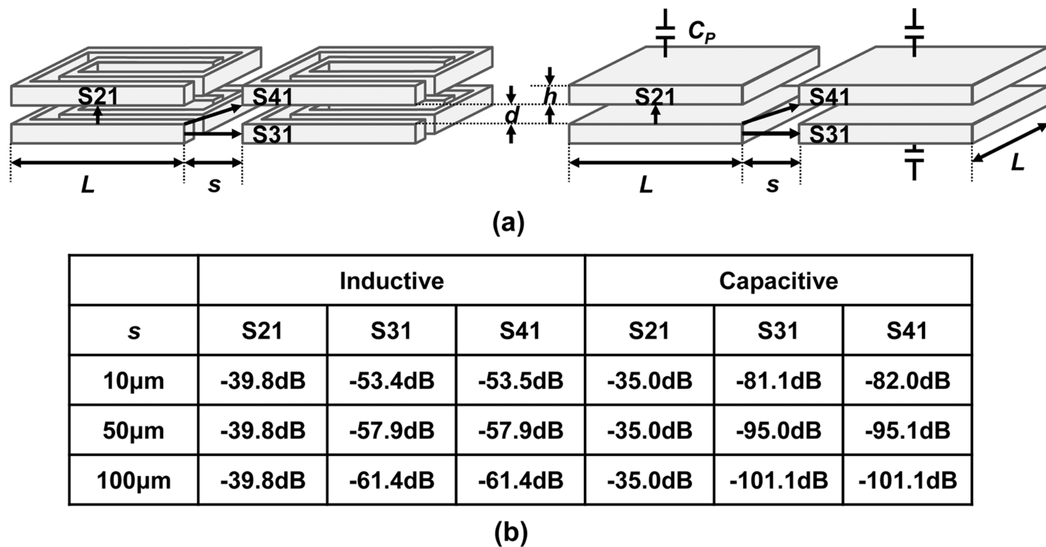
$$S41 \approx \frac{1}{C_P}\varepsilon\frac{Lh}{\sqrt{d^2+s^2}}. \tag{6}$$

The calculation results are shown in Fig. 3(b) with the typical parameters ($L = 100\ \mu$m, $d = 5\ \mu$m and $h = 1\ \mu$m) for the WLST. The differences between S21 and S31 in the ICI and the CCI are 13 dB and 46 dB when the separation distance is 10 μm, respectively. It is sufficient to ignore the effect of cross talk for the CCI. These results show that the CCI can place pads more closely and is more area-efficient for the WLST than the ICI.

III. Wafer-Level Simultaneous Testing

The probe card for the proposed WLST consists of five layers including a main board, anisotropic conductive elastomers (ACE1, ACE2), an interposer and a polyimide membrane as shown in Fig. 4. The tester chips and the probe chips are mounted on the main board. The tester chip implements simple tester functions and the probe chip has CCI. ACE1 and ACE2 can remove the differences in level between the main board and the interposer and between the interposer and the polyimide membrane, respectively. The polyimide membrane is very thin film which has the thickness of 25 μm, and has contacting bumps and non-contact pads. The contacting bumps can be used not only for power supply but also for testing ultra-high speed interfaces and analog and RF functions if needed. The expensive main board is common to all products and the inexpensive organic interposer and polyimide membrane are to be re-designed and built when a product under test is changed, and thereby the total cost of the probe card for WLST can be kept low.

To ensure the stable non-contact probing, a two-stage depressurization technique is developed. Pumping the air out of the space between the probe card and the wafer, the probe card is pressed to the wafer by 10 N/cm^2 of the atmospheric pressure. This technique makes it possible to distribute 700 kg of force



	Inductive			Capacitive		
s	S21	S31	S41	S21	S31	S41
10µm	-39.8dB	-53.4dB	-53.5dB	-35.0dB	-81.1dB	-82.0dB
50µm	-39.8dB	-57.9dB	-57.9dB	-35.0dB	-95.0dB	-95.1dB
100µm	-39.8dB	-61.4dB	-61.4dB	-35.0dB	-101.1dB	-101.1dB

Fig. 3. (a) Simplified interface models and (b) calculation results with $L = 100\ \mu\text{m}$, $d = 5\ \mu\text{m}$ and $h = 1\ \mu\text{m}$.

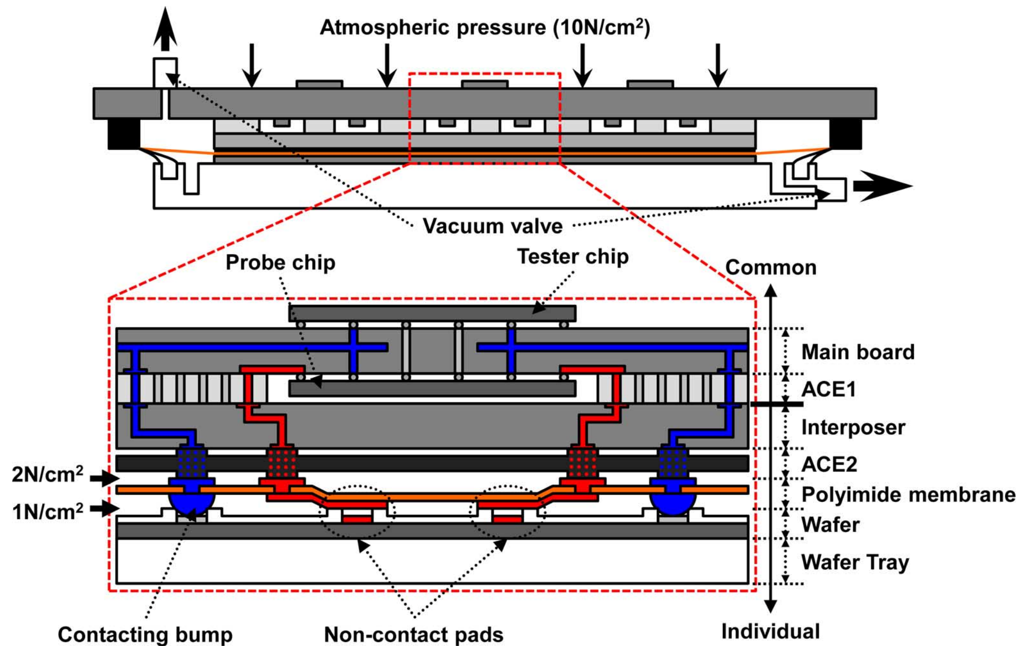


Fig. 4. Proposed wafer-level simultaneous testing technique with the capacitively coupled interface.

over the 300 mm wafer uniformly [1]. When the spaces between the interposer and the polyimide membrane and between the polyimide membrane and the wafer are equally depressurized to 1 N/cm^2, non-contact pads on the membrane stay away from the pads on the wafer. As turning the vacuum valve to depressurize the space between the interposer and the polyimide membrane to 2 N/cm^2, the polyimide membrane adheres to the wafer. Then the distance between the non-contact pads becomes almost zero, but the surface oxide of the wafer prevents them from connecting electrically. Since the almost all force is distributed to the contacting bumps, the non-contact pads are pressed softly to the wafer and have no reliability issue.

Fig. 5 shows the system block diagram of the proposed WLST. The tester chips implement simple tester functions including timing and control signal generation, test pattern buffing and test results compression, reducing the power and cost of communication between the main tester equipment and the probing system. The tester chip also has power-supply disconnecting functions for breakdown chips. The TXs on the probe chip and the DUT-wafer are simple CMOS drivers to share the bonding pads with the normal I/Os. The pads on the polyimide membrane and the DUT-wafer form the coupling capacitance. The signals travel between the probe chip and the DUT-wafer through the complex wiring structure depicted in Fig. 4. The total length of the wiring ranges around 20 mm and diverse reflections occur at interfaces among layers. Consequently, de-skewing function should be implemented for each digital channel.

Fig. 5. System block diagram of proposed WLST.

Fig. 6. Block diagram of feed-forward all-digital de-skewer.

IV. Feed-Forward All-Digital De-Skewer

To remove the skews between channels, a low-power and small-area de-skewing circuit, namely, Feed-forward All-digital De-skewer (FAD) in Fig. 6 is proposed. The FAD has two advantages over conventional de-skewing methods such as a clock data recovery [13]. One is that the FAD can be designed using only digital core transistors and the other is the feed-forward

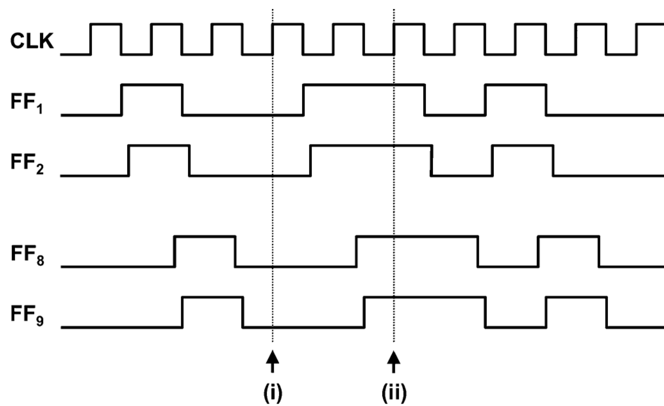


Fig. 7. Output waveforms of flip-flops in FAD.

architecture which makes the FAD fast and stable. The FAD is based on a time-to-digital converter [14], and uses delay elements not only detecting the phase error but also delaying the timing of input data to remove the skews between channels. The delay element is constantly adjusted to show one eighth of a clock cycle by a simple delay-locked loop. A bubble error corrector and a third order moving average filter are implemented to mitigate the effect of undesired signals by accidental errors.

For a certain channel, if the rising edges of delayed $\mathrm{D_{IN}}$ and CLK match at Flip-Flop "$\mathrm{FF_5}$", $\mathrm{D_{IN}}$ is considered to rise about a half clock cycle before the CLK rising edge, because the delay element is constantly adjusted to show one eighth of a clock cycle. Then, $\mathrm{D_{IN}}$ should be delayed about a half clock cycle to maximize the margin in synchronization which occurs at Flip-Flop "$\mathrm{FF_O}$" by using CLK bar. Thus, after the bubble error corrector and the third order moving average digital filter, the LUT-based adaptive switch selector selects the switch "$\mathrm{SW_5}$" and $\mathrm{D_{FADout}}$ is delayed a half clock cycle for $\mathrm{D_{IN}}$ by the delay elements. On the other hand, if $\mathrm{D_{IN}}$ rising edge comes a bit earlier (later), the matching edge is captured at location "$\mathrm{FF_2}$"("$\mathrm{FF_7}$ ") and the switch "$\mathrm{SW_2}$"("$\mathrm{SW_7}$") is selected. Thus, the rising edge of $\mathrm{D_{FADout}}$ is always delayed a half clock cycle for the rising edge of the CLK. When the FAD receives continuous same data streams like "00 . . ." or "11 . . . ", the switch "$\mathrm{SW_1}$" or "$\mathrm{SW_8}$" is incorrectly selected, because all Flip-Flops output 0 or 1 as shown at the timing (i) or (ii) in Fig. 7, respectively. To avoid such a consequence, Flip-Flop "$\mathrm{FF_9}$" is added. Since the delay element is constantly adjusted to show one eighth of a clock cycle, there is one clock cycle delay between the data at Flip-Flops "$\mathrm{FF_1}$" and "$\mathrm{FF_9}$". Therefore when the same data is captured at the location "$\mathrm{FF_1}$" and "$\mathrm{FF_9}$", $\mathrm{D_{IN}}$ is considered to be the continuous same data. Then the third order moving average digital filter does not capture the output of the bubble error corrector and the correct switch is kept selecting.

SPICE simulations have been performed to verify the effectiveness of the proposed de-skewing circuit using the three different delayed data such as -350 ps, 0 ps and 350 ps, as shown in Fig. 8. At first, $\mathrm{D_{OUT}}$ shows the same delay as $\mathrm{D_{IN}}$. After a few cycles, the edges at $\mathrm{D_{OUT}}$ become almost same, which means that the skews between data are removed. Fig. 8 also indicates the advantages of the FAD that the FAD does not needs the special calibration patterns to remove the skews and the adequate output switch can be selected quickly.

V. Receiver Circuit

Another point of difficulty in the membrane-based CCI over a chip-to-chip interface lies in the transmission nature of wiring and the smaller received signal due to the large capacitance of the transmission line up to 2 pF. To overcome the issue, a low-pass filter (LPF), which consists of the poly resistor and the capacitance of the electrostatic discharges (ESDs), is inserted before a preamplifier as shown in Fig. 9. The LPF can suppress the undesirable ringing caused by the diverse reflections because the frequencies of the reflections are usually higher than the signals in the proposed WLST. A DC-cutting capacitor is inserted to eliminate the interference between precharger1 and precharger2 even if the precharge levels are different due to process variations.

A high-sensitivity receiver circuit is introduced, denoted as weak-feedback receiver in Fig. 9. The previously reported receiver in [4] is robust but needs intermittent resetting of circuits which is difficult to implement in the test environment. In the proposed RX circuit, the feed-back node is not connected directly to the signal path compared to the conventional RX which has the direct feed-back path [6] as shown in Fig. 10. So the effect of the feed-back in the proposed RX becomes weaker. The minimum receivable input amplitude of the proposed RX is smaller than the conventional inverter cross-coupled RX, that is, the proposed RX has the higher sensitivity over large PVT variations. While receiving a same signal continuously, the node N2 of RX in Fig. 9 comes close to VDD or VSS and the sensitivity degrades at the next data change. The inverter connected an input with an output makes the voltage of N2 to leave slightly away from VDD or VSS and improves the sensitivity at such situation. As a result, the minimum receivable amplitude of the proposed RX is 50 mV.

VI. Experimental Result

Fig. 11 shows a full view of the proposed WLST. A 300 mm wafer is loaded under the probe card from a cassette and then pads on the wafer and the polyimide membrane are automatically aligned. When test is running, the probe card is put on the wafer and is pressed by the atmospheric pressure. For the sake of the flexible evaluation, FPGAs are mounted on the probe card as a substitute for tester chips.

The probe chip and the DUT-wafer are fabricated with a 90 nm 1.2 V CMOS technology. Two types of pad are implemented as shown in Fig. 12: one is an uncovered pad and the other is an insulator covered pad both of which worked successfully. Two versions of pad size, 80 μm $\times$ 80 μm and 160 μm $\times$ 160 μm, are tried but turned out that 80 μm $\times$ 80 μm is sufficient even with the maximum alignment error which is less than ± 5 μm over the whole 300 mm wafer. The probe chip has the pseudo-random bit sequence (PRBS) generator and the

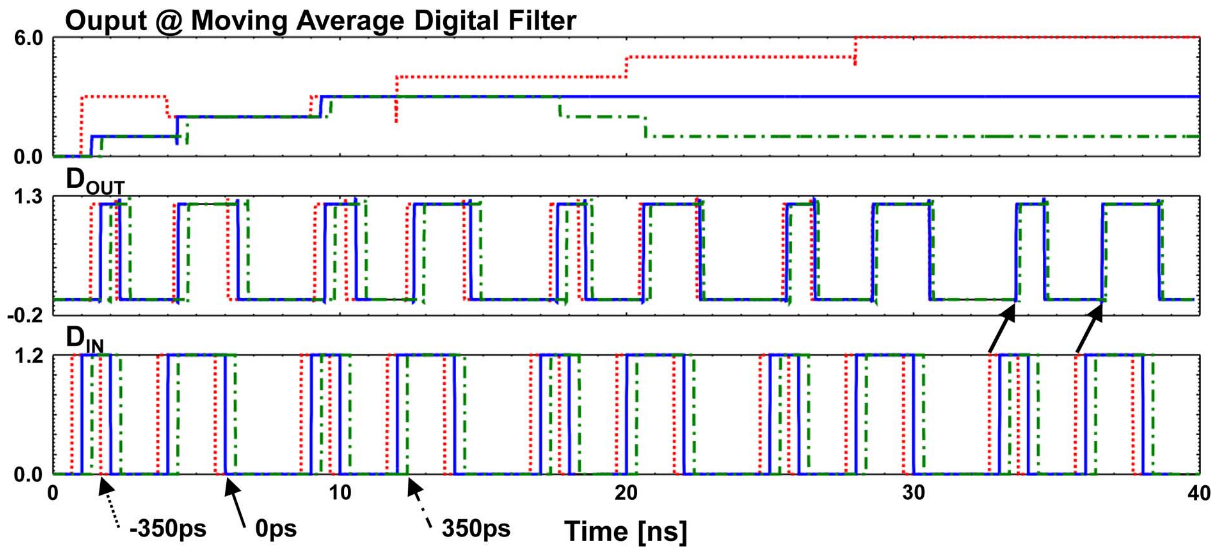


Fig. 8. Simulation result of FAD.

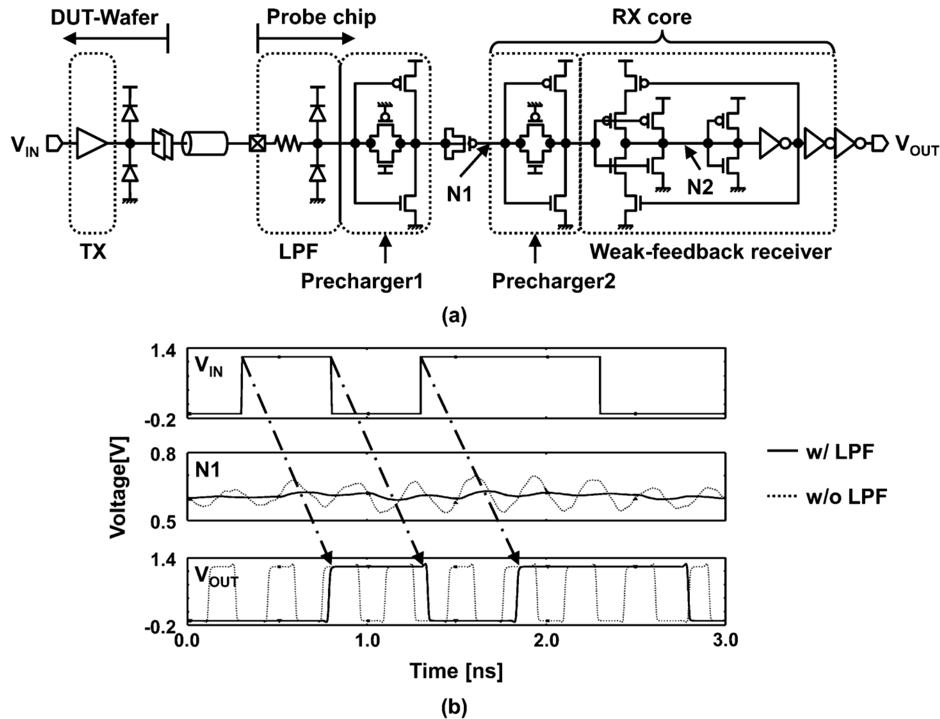


Fig. 9. (a) Proposed receiver circuit and (b) Simulation results.

bit error-rate (BER) tester for the high-speed signal test and the DUT-wafer has a simple function for the loop-back test.

Fig. 13 shows the measured output waveforms of the proposed receiver which indicate that the circuit can receive up to 1 GHz clock and 1 Gbps data. The 4-channel 1 Gbps data can be received successfully without cross talk between channels. In the single-ended interface, the power line noise is transformed into the RX input noise and degrades the BER. To avoid such situation, a large amount of on-chip and off-chip decoupling capacitors is placed in this prototype WLST. In the production environment, since there is little space to place the decoupling capacitors, the technique to make the RX insensitive to the power line noise and the scheme to decrease the power line impedance will be necessary.

The power consumption is 0.5 mW/channel for a RX core at 1.2 V 1 Gbps operation as shown in Fig. 14.

Two transmission lines which have the different lengths of 10 mm and 20 mm are implemented in the probe card to confirm the effectiveness of the FAD as shown in Fig. 15. When signals bypass the FAD, there is about 150 ps skew between signals (A) and (D). On the other hand, when signals go through the FAD, the skew between signals (B) and (C) is removed successfully. Fig. 16 shows the measurement results of the BER at 1 Gbps operation. When the de-skewing function (FAD) is turned off,

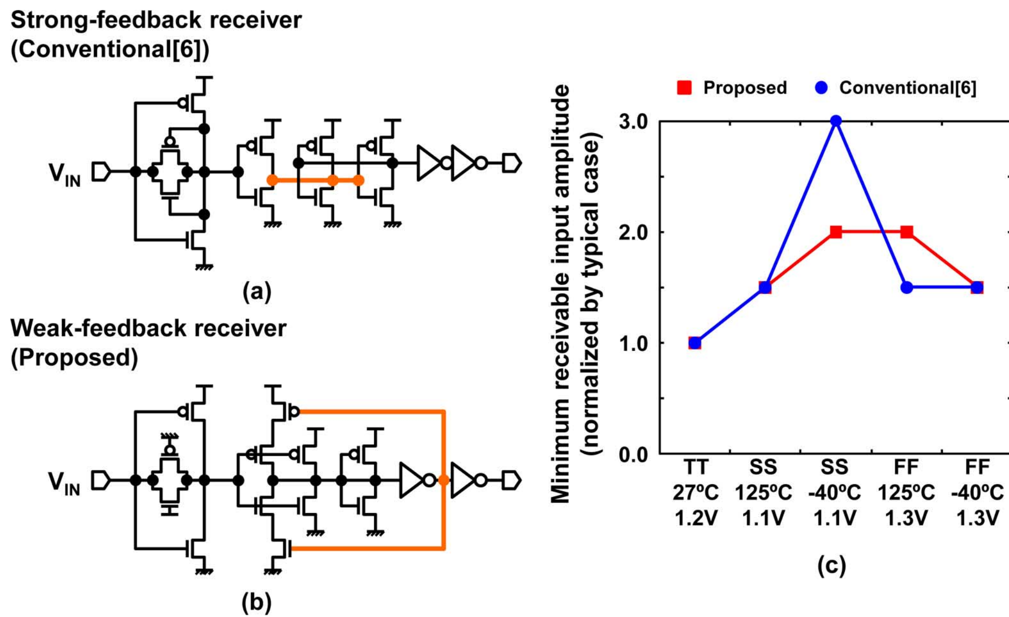


Fig. 10. Comparison of RX cores. (a) Conventional RX, (b) Proposed RX, and (c) Minimum receivable input amplitude for PVT variations.

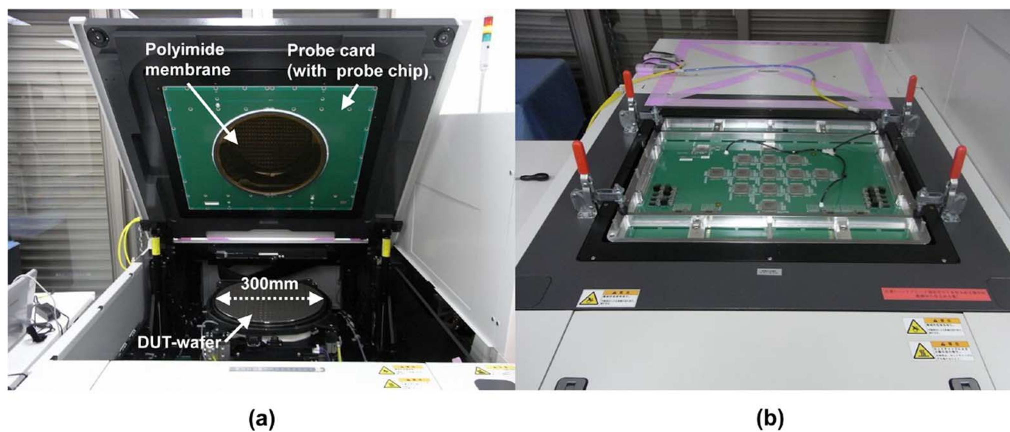


Fig. 11. Full view of proposed WLST. (a) Head plate open and (b) Head plate close.

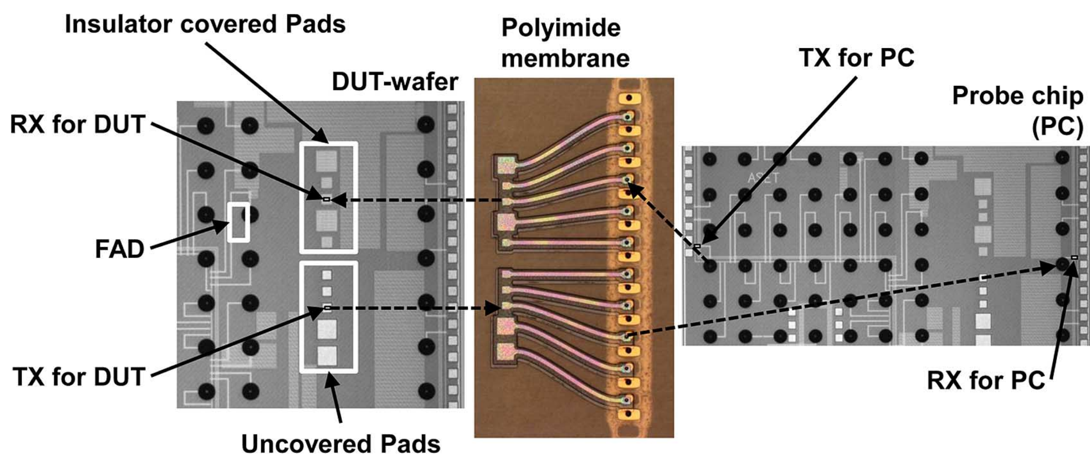


Fig. 12. Microphotographs of probe chip, DUT-wafer and polyimide membrane.

the BER is measured to be larger than 10^{-6} but the BER is improved below 10^{-12} over almost all unit-interval (UI) range when the FAD is turned on. Fig. 16 indicates that the FAD can also enhance the jitter tolerance.

Table I shows the performance summary. The power consumption of the proposed RX at 1 Gbps operation is 0.7 mW for the probe chip and 0.5 mW for the DUT-wafer. RX for DUT is smaller in size than RX for a probe chip because the

Fig. 13. Measured output waveforms of proposed receiver.

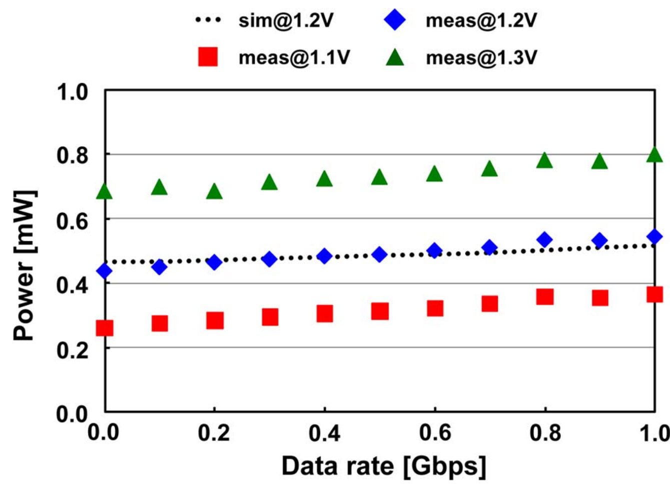
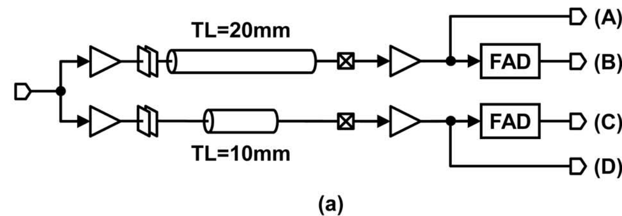


Fig. 14. Measured power consumption.



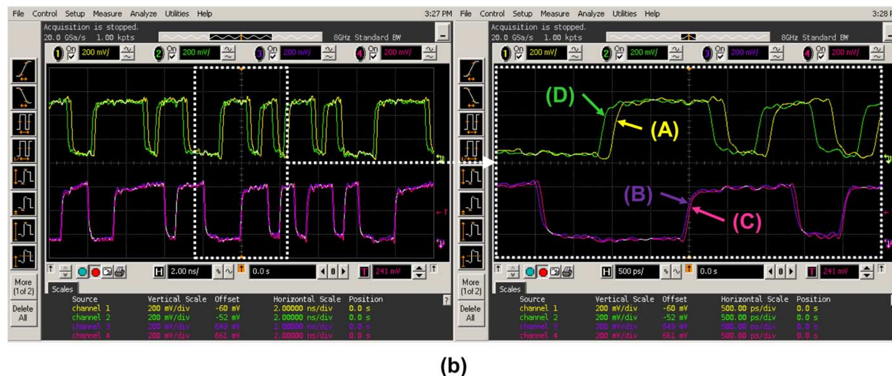


Fig. 15. (a) Block diagram of test setup and (b) Measured waveforms at 1 Gbps operation.

LPF is not needed for the latter since there is no long interconnect after the coupling capacitor. Since all functions are realized by digital core transistors and the feed-forward control is employed, the area is as small as 0.004 mm^2/channel and the measured power is 1.2 mW/GHz/channel, which should be compared with 0.3 mm^2/channel of area and 6.4 mW/GHz/channel of estimated power achieved by a previously-reported DLL-based clock de-skewer [15].

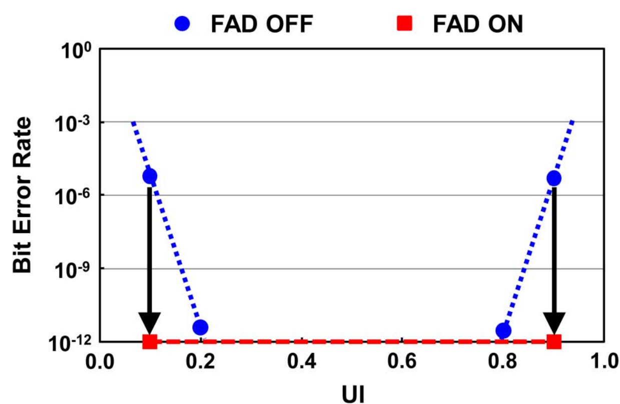


Fig. 16. Measured bit error rate at 1 Gbps operation.

TABLE I
PERFORMANCE SUMMARY

Technology		90nm CMOS
Supply voltage		1.2V
Data rate		1Gbps
Bit Error Rate		$< 10^{-12}$
Power@1Gbps	RX for probe chip	0.7mW
	RX for DUT-wafer	0.5mW
	FAD	1.2mW
Area size	RX for probe chip	$270\mu m^2$
	RX for DUT-wafer	$128\mu m^2$
	FAD	$4000\mu m^2$

VII. CONCLUSION

The proposed wafer-level simultaneous testing system has two features. One is the low-cost membrane based probing technique with use of the atmospheric pressure and the other is the capacitively coupled non-contact probing circuit. The FAD consumes 1.2 mW/GHz/channel and the BER is improved below 10^{-12} over almost all UI range when the FAD is turned on. The weak-feedback receiver with the LPF has higher sensitivity over large PVT variations and consumed 0.5 mW/channel at 1.2 V 1 Gbps operation. The overhead area of the DUT-wafer for using the proposed non-contact scheme is only 128 μm^2/channel because the bonding pad can be used for the signaling.

The proposed techniques make it possible to test all chips on the wafer simultaneously and reduce the test cost dramatically. Yet the power supply requires the contacting bumps and the further work will focus on developing the capacitively coupled non-contact power supply.

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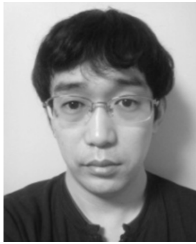
In 1980 he joined the Semiconductor Research Laboratory, Matsushita Electric Industrial Co., Ltd. (now Panasonic Corporation), Osaka, Japan, where he was engaged in research on the reliability of MOS devices. Since 1989 he has been engaged in the development of high-density CMOS memory devices. Since 1994 he has been engaged in the research and development of WLBI technology. In 1999 he introduced 8-inch WLBI system to semiconductor factory. In 2002 he developed and introduced 300 mm WLBI system to the factory. Since 2007, he has been with the Association of Super-Advanced Electronics Technologies, Yokohama, Japan, where he is engaged in the research and development of wafer level test and burn-in technology.

Satoshi Sasaki received the B.S. degree in electronics engineering from Chiba University, Japan, in 1988.

From 1988 to 1991, he was with Uniden Corporation, Chiba, Japan, where he was engaged in the development of pagers, satellite tuners, and cordless telephones. From 1991 to 1998, he was with Sumitomo Metal Mining Co., Ltd., where he was engaged in production engineering and development of the PZT IR detector. From 1998 to 2004, he was with Matsusita Communication Industrial Co., Ltd., where he was engaged in the research and development of WLBI technology. From 2005 to 2008, he was with Matsushita Electric Industrial Co., Ltd., Osaka, Japan, where he was engaged in the development of the Production facility of the plasma display panel. Since 2008, he has been with the Association of Super-Advanced Electronics Technologies, Yokohama, Japan, where he is engaged in the research and development of full-wafer level test and burn-in technology.



Hiroyuki Gomyo received the B.S. and M.S. degrees in electronic engineering from the University of Tokyo, Tokyo, Japan, in 1999 and 2001, respectively.

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Yoshio Komoto is a Researcher of the Association of Super-Advanced Electronics Technologies (ASET), Yokohama, Japan. He has researched the test system with wireless interconnect technology at ASET. Also, he has been engaged in the development of test systems at Advantest Corporation.

Kunihiko Iizuka (M'94) received the B.S. and M.S. degrees in mathematics from Osaka University, Osaka, Japan, in 1979 and 1981, respectively. He continued his study of mathematics as a postgraduate at Osaka University from 1981 to 1984. Later, he was enrolled in a postgraduate course of electronic engineering at the Tokyo Institute of Technology, Tokyo, Japan, from 2006 to 2009, and received the Ph.D. degree from the same university in 2009 on the subject of RF and analog integrated circuits for television broadcast receivers.

In 1984, he joined Sharp Corporation, Japan, where he was involved in the research of computer simulation systems. From 1991 to 1993, he was at the Center for Adaptive Systems, Boston University, Boston, MA, as a visiting researcher, working on neural network systems. Since 1993, he has been working on research and development of analog and mixed signal LSI circuits for high precision ADCs, vision systems, and wireless systems with Sharp Corporation.

Dr. Iizuka was a member of the ISSCC program committee from 2001 to 2008 and was the ISSCC Far East regional subcommittee chair for ISSCC 2005 and 2006. He has been a member of the A-SSCC program committee since 2006. Currently, he is the chair of the A-SSCC data converter subcommittee and the chair of IEEE SSCS Kansai Chapter.

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Dr. Sakurai is the executive committee chair for VLSI Symposia and a steering committee chair for the IEEE A-SSCC. He served as a conference chair for the Symp. on VLSI Circuits, and ICICDT, a vice chair for ASPDAC, a TPC chair for the A-SSCC and VLSI Symposium, an executive committee member for ISLPED and a program committee member for ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He is a recipient of 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, 2010 and 2011 IEEE Paul Rappaport award, 2010 IEICE Electronics Society award, 2009 IEICE achievement award, 2005 IEEE ICICDT award, 2004 IEEE Takuo Sugano award and 2005 P&I patent of the year award and four product awards. He has given keynote speeches at more than 50 conferences including ISSCC, ESSCIRC, and ISLPED. He was an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS distinguished lecturer. He is an IEICE Fellow and IEEE Fellow.