12.2 100V AC Power Meter System-on-a-Film (SoF) Integrating 20V Organic CMOS Digital and Analog Circuits with Floating Gate for Process-Variation Compensation and 100V Organic PMOS Rectifier

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A smart meter is essential for realizing the smart grid. In order to further reduce the energy loss in the power grid, an extremely fine-grain power monitoring system is desirable and it will require an enormous number of low-cost power meters. Existing power meters, however, do not meet the cost and size requirements. On the other hand, organic devices on flexible films have great potential to realize low-cost power meters. In this paper, a 100-V AC power meter based on System-on-a-Film (SoF) concept is demonstrated.

Figure 12.2.1 shows the photograph of the proposed 100-V AC power meter on a flexible film, including: (a) analog circuits composed of a 20-V organic CMOS opamp for AC current sensing, (2) logic circuits composed of a 20-V organic CMOS frequency divider for integrating the measured current, (3) AC-to-DC power converter composed of a 100-V organic PMOS rectifier to generate 20-V DC power for the power meter, (4) an OLED [1] bar indicator, and (5) an AC connector inserted between the power plug and the AC outlet are fully integrated on a 200×200mm^2 flexible film. The entire sheet can be folded and the total size of the proposed AC power meter can be shrunk to 70×70mm^2. In this work, the system dimensions are mainly determined by the design-rule of the organic transistors and can be further reduced by scaling of the design-rule. Figure 12.2.2 shows the block diagram of the proposed 100-V AC power meter. The measured 100V 50Hz AC load current i_L is first converted into the sense voltage (v) by means of the sense resistor (R). The converted sense voltage v is then amplified by the amplifier and rectified into V_{SENSE}, which is compared with the triangular waveform (V_{TRI}) by the comparator. The output of the comparator enables or disables the 10-bit counter. five most-significant bits in the counter are connected to the OLED bar indicator. To get the accumulated results, the maximum integration time of the power meter is designed to be 43min. The 0.05-Hz clock for the input of the triangular waveform generator and the 0.4-Hz clock for the counter are generated by a 10-bit frequency divider, for which the clock is generated by a half-wave rectifier from 100-V 50-Hz AC signal. The required DC power for the power meter is provided by converting the 100-V 50-Hz AC power into 20-V DC power by the full-wave rectifier.

We implement a full-wave rectifier using 100-V organic PMOS. The current consumption of the system, mainly consumed by the 5-digit OLED bar indicator, is around 2mA. Since the driving capability of organic NMOS is weaker than that of PMOS by an order, we choose an all-PMOS full-wave rectifier. In a typical rectifier as shown in Fig. 12.2.3(a), each PMOS operates at the pinch-off region. To increase the output current of the rectifier, two PMOS diodes are replaced with a pair of cross coupled PMOS operating in the linear region as shown in Fig. 12.2.3(b). Both two rectifiers are implemented by PMOSs with gate length and width of 20μm and 100mm, respectively, which can supply up to 2-W DC power, the highest power level ever reported. Figure 12.2.3 (c) shows the comparison of the rectifiers. While the PMOS diode rectifier supplies 2.1-mA output current at 20V, the cross-coupled PMOS rectifier can increase the output current by 24%. Figure 12.2.3(d) shows the measured waveform of the 21.9-V output voltage of the cross-coupled PMOS rectifier.

In our 20-V CMOS, DNTT-based PMOS has 8 times higher carrier mobility than NTCDI-based NMOS [2, 3]. In addition, our CMOS inverter gain was only 3.2 at 20V and this leads to functional errors in the large scale logic circuits. To solve the problem, we designed the frequency divider with high-gain Pseudo-CMOS inverters [4]. The Pseudo-CMOS inverter uses only PMOS. The gain of 148, static noise-margin of 6.7V, and 156-Hz oscillation frequency of a 3-stage ring-oscillator can be achieved at 20V supply voltage. Figure 12.2.4 shows the schematics and measured waveform of the Pseudo-CMOS inverter and the proposed frequency divider. In the divider, NMOSs are used only for transmission gates, in which high gain is not required. Thanks to high gain Pseudo-CMOS, the divider successfully operates at 50Hz and 20V. In the frequency divider, the dynamic slave latch, which consists of only an inverter and the parasitic capacitance as the charge keeper, is used to reduce the number of transistors.

A major challenge in organic analog circuit design is to compensate for large process variations. The offset voltage in the differential pair of the amplifier due to the device mismatch should be reduced to lower than the sense voltage generated by the sense resistor R in Fig. 12.2.2. Some variation compensation techniques using back gate biasing [5, 6] were presented. However, the back gate voltages of each organic device should be biased throughout the operation time. To tackle this problem, we employ floating gate (FG) PMOS technology [7] to compensate for the process variations in the input stage of the opamp. The cross section of the device with FG is shown in Fig. 12.2.5(a). By applying -60V 100ms-width pulses to the gate terminal as shown in Fig. 12.2.5(b), holes can be injected into FG, which increases V_{TH} of the FG-PMOS. The key advantages include: 1) the variation compensation can be carried out by single high voltage source with the fixed voltage, 2) the controllability is provided by varying the voltage pulse width and the number of pulses, and 3) once the variation compensation is completed, no external DC voltage sources are required throughout the operation time. As shown in Fig. 12.2.5(c), the input differential pair of the opamp is composed of two PMOS (M1, M2) with FG and five IO pads are added for the use of mismatch compensation.

Figure 12.2.6 shows measured results of the variation compensation. Figure 12.2.6(a) shows I_D-V_{GS} characteristics of M1 and M2 in Fig. 12.2.5(c). V_{TH} of M1 is monotonically shifted toward V_{TH} of M2 by increasing the compensation time. As the result, V_{OUT}-V_{IN} characteristics of the opamp can be modified as shown in Fig. 12.2.6(b). Figure 12.2.6(c) shows the dependence of differential voltage gain at $V_{INP} = V_{INN} = 15V$ on the compensation time derived from Fig. 12.2.6(b). The initial gain of 2.7 can be raised to 4.9 by applying 2 pulses (=200ms). Figure 12.2.6(d) shows the dependence of V_{OUT} on the compensation time. V_{OUT} is shifted from 8.4V to 12.5V by applying 2 pulses. In this way, the performance of the opamp can be optimized. Figure 12.2.7 shows the photographs of organic circuits and summarizes key features. The AC power meter consists of 609 transistors and the total area excluding AC connector is 200 × 200mm^2 (unfolded form) or 70 × 70mm^2 (using form).

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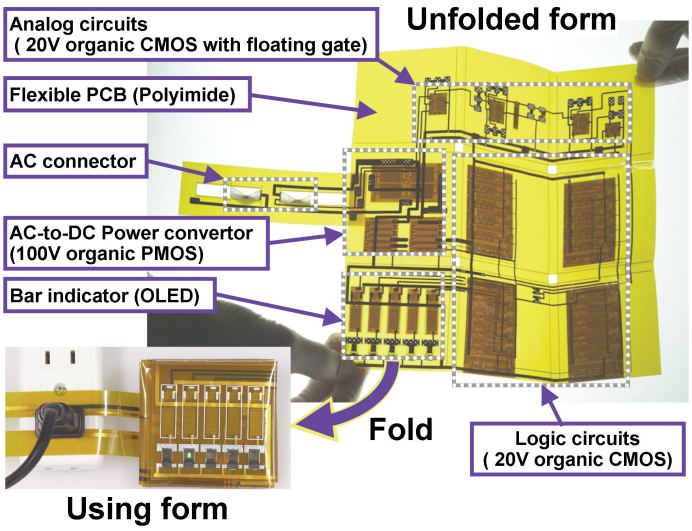


Figure 12.2.1: Prototype of 100V AC power meter on a folded film.

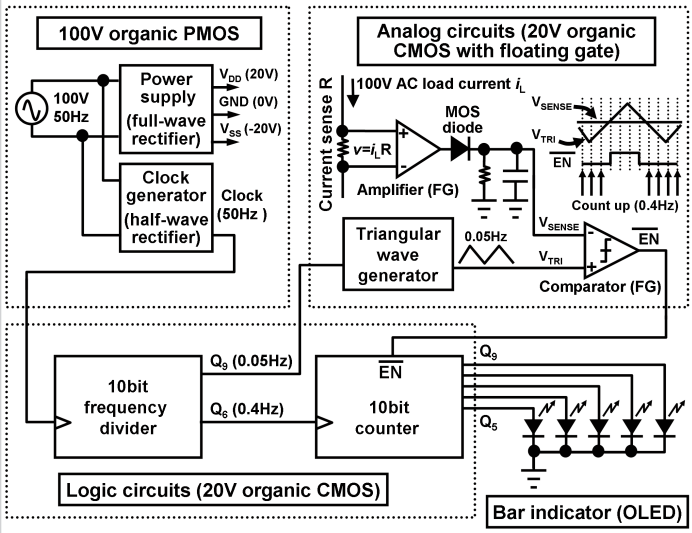


Figure 12.2.2: System block diagram of the AC power meter.

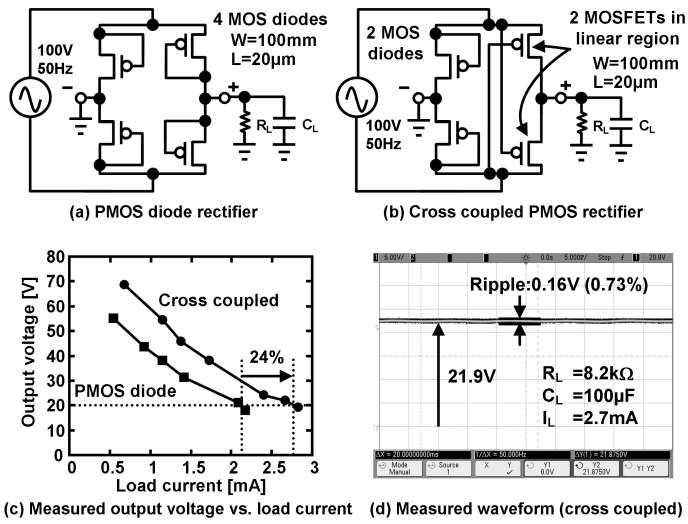


Figure 12.2.3: 100V organic PMOS rectifier.

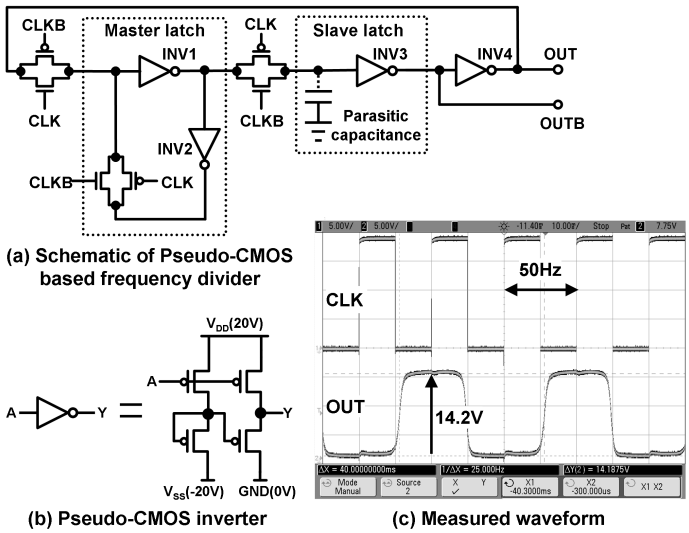


Figure 12.2.4: 20V organic Pseudo-CMOS based frequency divider.

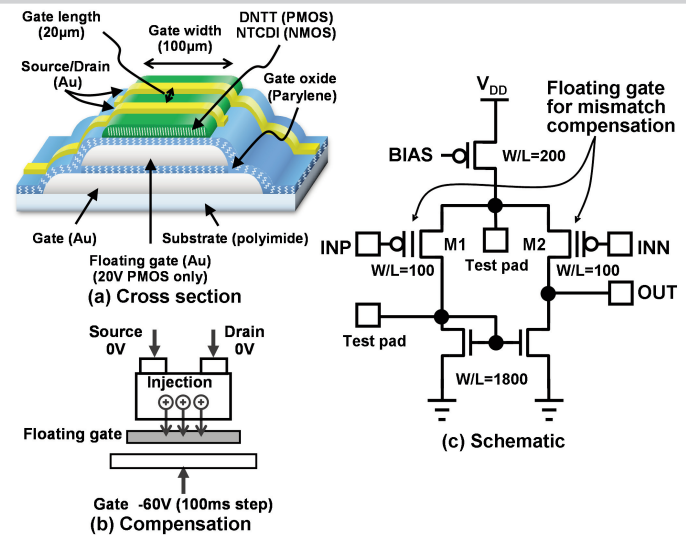


Figure 12.2.5: 20V organic CMOS opamp with floating gate for variation compensation.

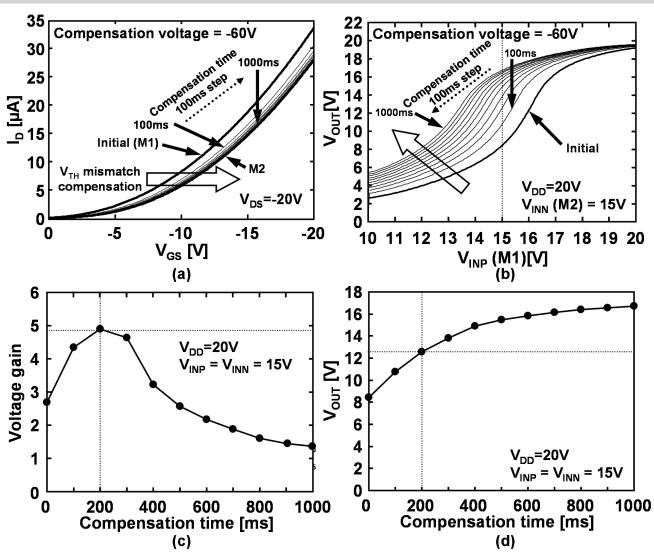
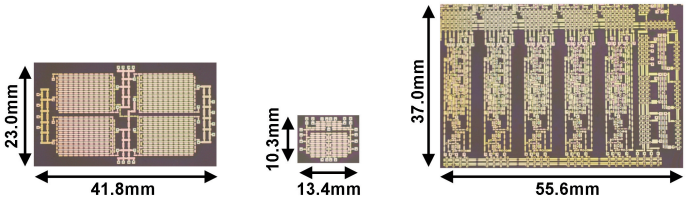


Figure 12.2.6: Measured mismatch compensation of opamp in Fig. 12.2.5.



(a) 100V PMOS rectifier (b) 20V opamp with FG (c) Pseudo-CMOS 5bit counter

Organic transistors	
100V PMOS	Pentacene(0.5 cm^2/Vs),
20V CMOS	PMOS:DNTT(0.7 cm^2/Vs), NMOS:NTCDI (0.09 cm^2/Vs)
Gate oxide material, thickness	Parelene, 560nm(100V), 360nm(20V), 240+240nm(20V+FG)
Compensation voltage	-60V(100ms step)
Organic LED	
Materials	TBADN, TCTA, TTPA
100V AC power monitor	
100V PMOS maximum power dissipation	2W (20mA@V_{GS}=-48V, V_{DS}=-100V)
Ring oscillator frequency of Pseudo-CMOS	156Hz@20V
Number of transistors	609Tr.
Total area excluding AC connector	200x200mm^2(unfolded), 70x70mm^2(folded)

Figure 12.2.7: Photographs and key features.

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