Device-Circuit Interactions in Extremely Low Voltage CMOS Designs (Invited)

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Abstract

In this paper, energy and minimum operating voltage (V_{DDmin}) are investigated for extremely-low-voltage CMOS logic designs. The dependences of energy and V_{DDmin} on device parameters, such as threshold voltage, subthreshold swing parameter, and DIBL coefficient, are examined based on simulations and measurements.

Introduction

Extremely-low-voltage operation in VLSI's is quite effective in reducing the power dissipation [1]. Fig. 1 shows simulated delay, power, and energy (power delay product) of a CMOS logic circuit. As the supply voltage (V_{DD}) is reduced, the delay increases, whereas the power dissipation dramatically decreases. Therefore, extremely-low-voltage operation has been considered to be suitable for low-power applications in which circuit speed is not a primary concern or can be compensated by parallelization. For such applications, an energy per instructions is a key metric. As shown in Fig. 1, the energy has its optimum value (E_{opt}), and V_{opt} is defined as V_{DD} at which the energy becomes optimum. Since the operation at V_{opt} can achieve the most energy-efficiency, V_{opt} is the target supply voltage for ultra-low-power applications.

V_{DD} reduction, however, could cause functional errors [2], which might make it impossible to operate at V_{opt}. Therefore, investigations on the minimum operating voltage (V_{DDmin}), which is the supply voltage where the first functional error occurs, are essential for extremely-low-voltage CMOS designs.

In this paper, what determines V_{DDmin} is explained first, and then the dependences of V_{DDmin} and energy on device parameters, such as threshold voltage, subthreshold swing parameter, and DIBL coefficient, are discussed.

Minimum Operating Voltage (V_{DDmin})

Fig. 2 shows a closed-form expression of V_{DDmin} of logic gates when the number of gates is relatively large [3]. V_{DDmin} can be expressed as a linear function of square-root of logarithm of the number of logic gates. This means that V_{DDmin} rises as the number of logic gates increases. The slope of the function is proportional to the standard deviation of the within-die variation in the threshold voltage (V_{TH}) difference between pMOS and nMOS transistors (σ_{pn}), and the intercept depends on the balance between intrinsic strengths of pMOS and nMOS transistors (β), device

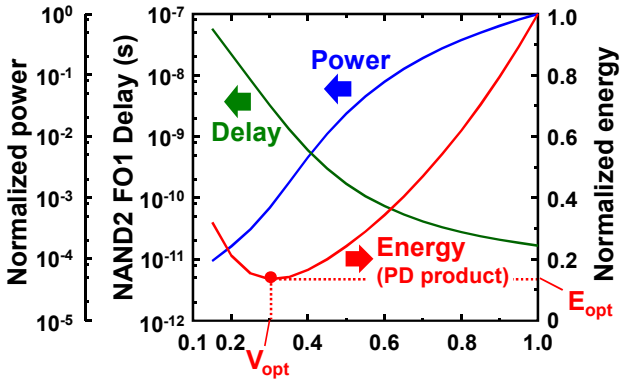

Fig. 1: Simulated dependence of power, delay, and energy of CMOS logic circuit on supply voltage in 65nm CMOS process. Energy has its optimum value (E_{opt}).

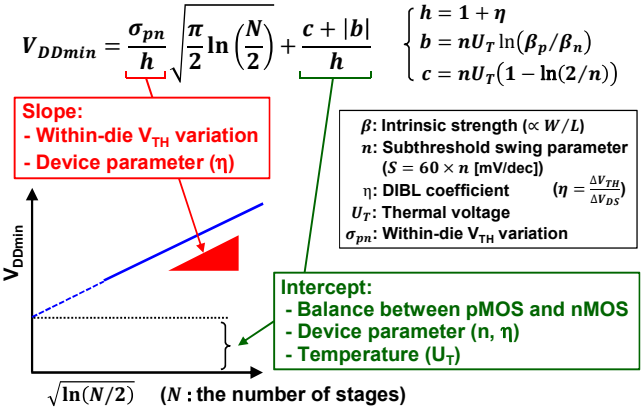

Fig. 2: Closed-form expression of median V_{DDmin} of logic gates where pMOS and nMOS are not perfectly balanced. N must be relatively large (more than 10-100). σ_{pn} represents standard deviation of within-die V_{TH} variation.

parameters, such as subthreshold swing parameter (n) and DIBL coefficient (η), and temperature (U_T).

Fig. 3 illustrates V_{DDmin}'s with various configurations of within-die V_{TH} variation obtained by Monte Carlo SPICE simulations and the closed-form expression (Fig. 2). Simulated results indicate V_{DDmin} is proportional to square-root of logarithm of the number of logic gates. Fig. 4 shows the dependence of V_{DDmin} of inverter chain on σ_{pn}. As the number of gates increases, the rise in V_{DDmin} due to within-die V_{TH} variation is enlarged. This means mitigating V_{TH} variation is effective in reducing V_{DDmin}, especially for large-

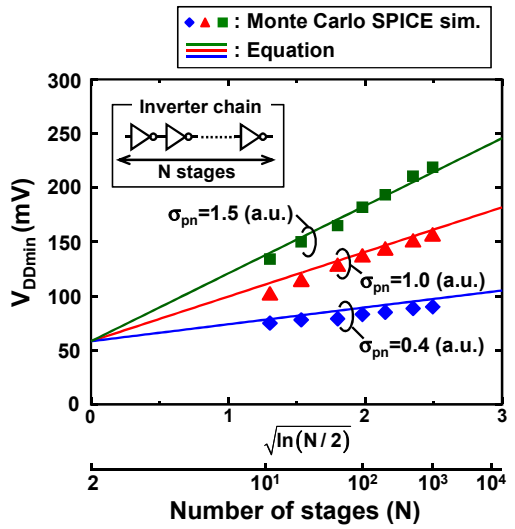

Fig. 3: V_{DDmin}'s of inverter chain obtained by Monte Carlo SPICE simulations and closed-form expression (Fig. 2) with various σ_{pn}'s in 65nm process. σ_{pn}'s are normalized by nominal value of this process.

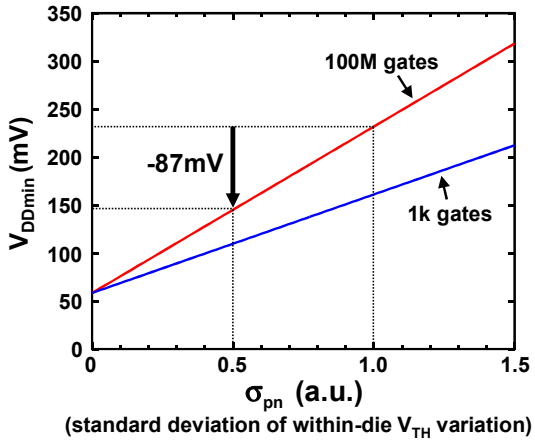

Fig. 4: Dependence of V_{DDmin}'s of inverter chain on σ_{pn}, which represents standard deviation of within-die V_{TH} variation in 65nm process. If σ_{pn} is reduced by 50%, V_{DDmin} of 100M inverters decreases by 87 mV.

scale circuits. For example, V_{DDmin} of 100M inverters decreases by 87 mV if σ_{pn} is reduced by 50%.

In addition, various gate chains were fabricated in a 65nm CMOS process, and V_{DDmin}'s of them were measured. The measurement results of the inverter and 2-input NAND chains are shown in Fig. 5. The closed-form expression (Fig. 2) also agrees with the measurement results.

Fig. 6 shows simulated V_{DDmin}'s of the inverter and NAND chains. V_{DDmin}'s of logic gates containing the larger number of stacked/paralleled transistors are much higher. This is because stacking and paralleling transistors contained in the NAND gate worsen the balance of the strength of pMOS and nMOS, which corresponds to the increase in parameter $|b|$ in the closed-form expression (Fig. 2). Although V_{DDmin} can be reduced by adjusting the balance

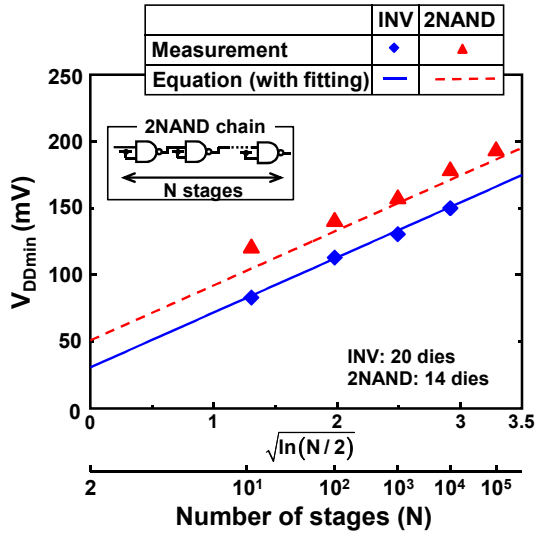

Fig. 5: Measured and calculated V_{DDmin}'s of inverter and 2-input NAND chains in 65nm process.

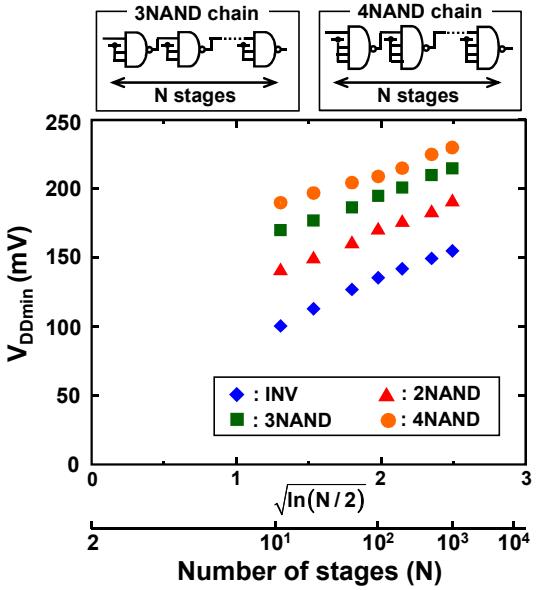

Fig. 6: Simulated V_{DDmin}'s of inverter and 2-, 3-, 4-input NAND chains. Slope is hardly affected by the number of transistor stacks.

between the strength of pMOS and nMOS, it is usually impractical, since the gate sizes of either pMOS or nMOS transistors must be significantly enlarged for the adjustment, and hence it is not acceptable due to the area constraint [4]. Therefore, the logic gates with a lot of inputs should not be used in the design of extremely-low-voltage CMOS logic circuits.

In Fig. 6, it should be noted that the increase in the number of transistor stacks does not affect the slope which is proportional to σ_{pn}. It is well known that σ_{pn} is proportional to $1/\sqrt{L \times W}$ [5]. For gate delays, transistor stack helps average gate delay variations induced by within-die V_{TH}

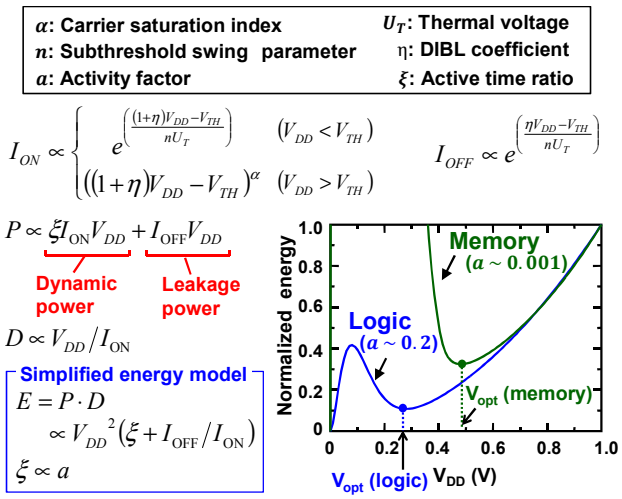

Fig. 7: Simplified energy model and dependence of energy on activity factor (a). Active time ratio ξ is introduced to express dynamic power, and is considered constant for simplicity.

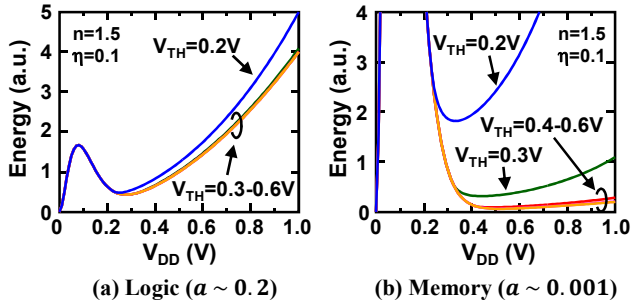

Fig. 8: Energy dependence on V_{TH}. V_{opt} and E_{opt} do not depend on V_{TH} as long as V_{opt} is less than V_{TH}.

variation, since the number of active transistors contributing the gate delay increases [6]. In contrast, no such averaging effect is observed for the dependence of V_{DDmin} on the number of transistor stacks as shown in Fig. 6.

Dependences of Energy and V_{DDmin} on Device Parameters

In order to comprehend the dependence of energy on V_{DD}, a simplified energy model shown in Fig. 7 is introduced. Figures regarding energy shown in this section are obtained by this energy model. Fig. 7 illustrates the normalized energies of a typical logic circuit and memory. V_{opt} depends on activity factor. V_{opt}'s of circuits with higher activity factors, such as logic circuits, are lower and may become less than 0.3V.

Fig. 8 shows the dependence of energy on V_{TH}. As long as V_{opt} is less than V_{TH}, V_{opt} and E_{opt} hardly depend on V_{TH} [7]. In this case, lower V_{TH} is preferable, since the decrease in V_{TH} can improve the circuit speed without any energy penalties.

On the other hand, V_{TH} itself does not determine V_{DDmin}. Fig. 9 illustrates the measured dependence of V_{DDmin} in

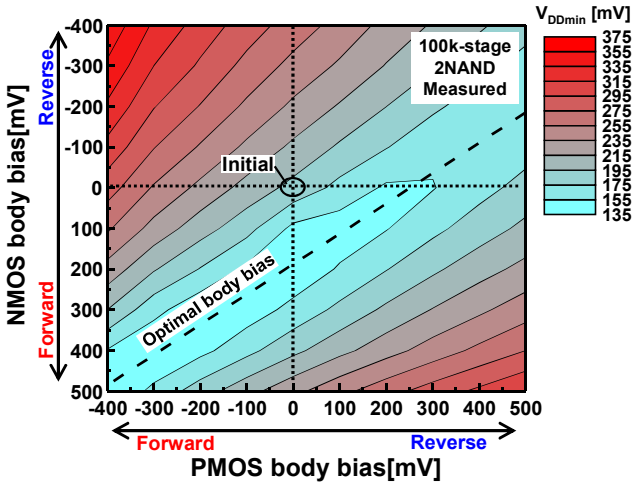

Fig. 9: Measured dependence of V_{DDmin} in 100k-stage 2NAND chain on body bias of pMOS and nMOS in 65nm process.

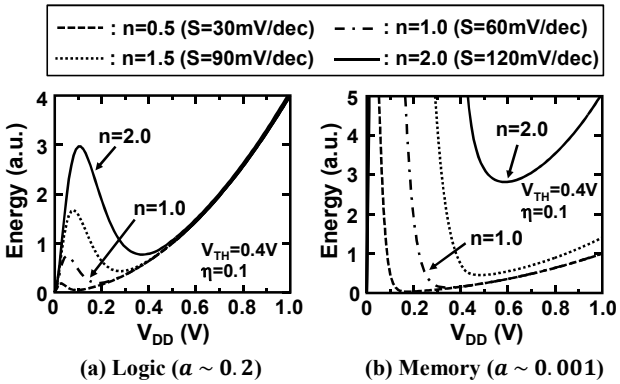

Fig. 10: Energy dependence on subthreshold swing parameter (n; $S = 60 \times n$ mV/dec). V_{opt} and E_{opt} strongly depend on n, and they are reduced as n decreases.

100k-stage NAND2 chain on body bias of pMOS and nMOS [4]. When pMOS and nMOS are well-balanced, V_{DDmin} is lowest as shown in the optimal body bias line. In contrast, when pMOS and nMOS are unbalanced, V_{DDmin} increases. This is because V_{DDmin} does not depend on the absolute value of V_{TH} but is determined by the relative relation between pMOS and nMOS, which is represented by parameter $|b|$ in the closed-form expression (Fig. 2).

Fig. 10 shows the dependence of the energy on subthreshold swing parameter (n). E_{opt} and V_{opt} are reduced as n decreases. Fig. 11 illustrates the dependence of V_{DDmin}'s of logic circuits on n obtained by the closed-form expression (Fig. 2). The decrease in n also reduces V_{DDmin}.

Fig. 12 depicts the dependence of the energy on DIBL coefficient (η). While the energy does not depend on η for logic circuit, E_{opt} is reduced as η decreases for memory, since the influence of leakage energy increases as the activity factor (a) is lowered.

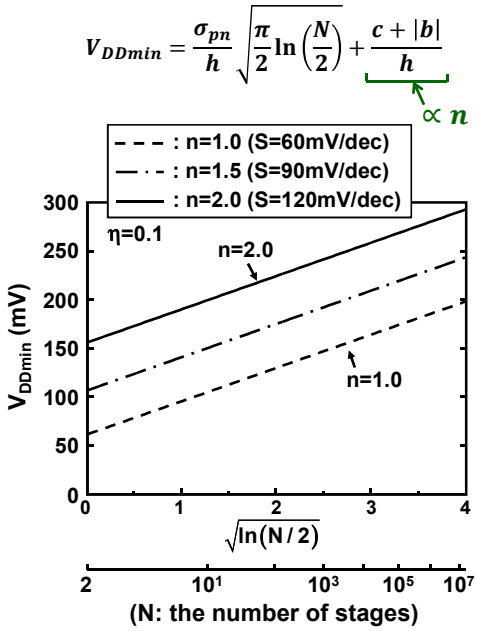

Fig. 11: V_{DDmin} dependence of logic gates on subthreshold swing parameter (n; $S = 60 \times n$ mV/dec) obtained by closed-form expression shown in Fig. 2. Decrease in n reduces V_{DDmin}, since intercept of V_{DDmin} expression is proportional to n.

Conclusion

In this paper, energy and V_{DDmin} in extremely-low-voltage circuits were discussed. Insights obtained from the discussions are; (1) V_{DDmin} is expressed as a function of the number of logic gates and its slope depends on within-die V_{TH} variation. Thus, a mitigation of within-die V_{TH} variation can significantly reduce V_{DDmin}. (2) The decrease in subthreshold swing parameter, that is, making the subthreshold slope steeper, is effective in reducing both the optimum energy (E_{opt}) and V_{DDmin}. (3) The decrease in DIBL coefficient (η), that is, mitigating the short-channel effect can reduce E_{opt} of circuits with lower activity factors, such as memory.

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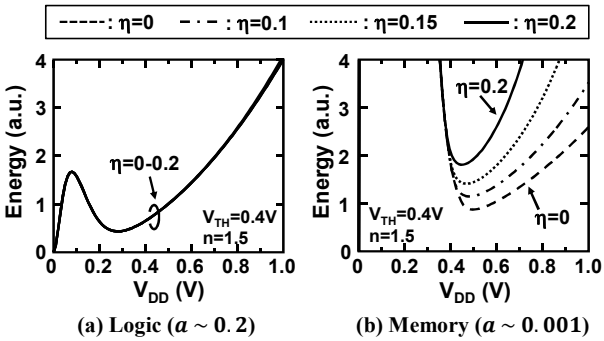

Fig. 12: Energy dependence on DIBL coefficient ($\eta = \Delta V_{TH} / \Delta V_{DS}$). Although energy does not depend on η for logic circuit, E_{opt} is reduced as η decreases for memory. This is because influence of leakage energy in memory is much larger than that in logic circuit.

References

[1] A.W. Wang, B. H. Calhoun, and A. P. Chandrakasan, Sub-threshold Design For Ultra Low-Power Systems, New York: Springer, 2006

[2] T. Niiyama, Z. Piao, K. Ishida, M. Murakata, M. Takamiya, and T. Sakurai, "Increasing Minimum Operating Voltage (V_{DDmin}) with Number of CMOS Logic Gates and Experimental Verification with up to 1Mega-stage Ring Oscillators," in *Proc. International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 117–122, 2008.

[3] H. Fuketa, S. Iida, T. Yasufuku, M. Takamiya, M. Nomura, H. Shinohara, and T. Sakurai, "A Closed-form Expression for Estimating Minimum Operating Voltage (V_{DDmin}) of CMOS Logic Gates," in *Proc. Design Automation Conference(DAC)*, pp. 984–989, 2011.

[4] T. Yasufuku, S. Iida, H. Fuketa, K. Hirairi, M. Nomura, M. Takamiya, and T. Sakurai, "Investigation of Determinant Factors of Minimum Operating Voltage of Logic Gates in 65-nm CMOS," in *Proc. International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 21-26, 2011.

[5] M. Pelgrom, A.C. J. Duinmaijer, and A.P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1439, May 1989.

[6] X.Zhang, K.Ishida, M.Takamiya, and T.Sakurai, "An On-Chip Characterizing System for Within-Die Delay Variation Measurement of Individual Standard Cells in 65-nm CMOS," in *Proc. Asia South Pasific Design Automation Conference (ASP-DAC)*, pp. 109-110, 2011.

[7] B. Zhai, R.G. Dreslinski, D. Blaauw, T. Mudge, and D. Sylvester, "Energy efficient near-threshold chip multi-processing," in *Proc. International Symposium on Low Power Electronics and Design (ISLPED)*, pp. 32–37, 2007.