

Transactions Briefs

On-Chip Measurement System for Within-Die Delay Variations of Individual Standard Cells in 65-nm CMOS

Xin Zhang, Koichi Ishida, Hiroshi Fuketa, Makoto Takamiya, and Takayasu Sakurai

Abstract—New measurement system for characterizing within-die delay variations of individual standard cells is presented. The proposed measurement system are able to characterize rising and falling delay variations separately by directly measuring the input and output waveforms of individual gate using an on-chip sampling oscilloscope in 65 nm 1.2V CMOS process. Seven types of standard cells are measured with 60 DUTs for each type. Good correlations of within-die delay distributions between measured and Monte Carlo simulated results are observed. The measured results of rising and falling delay are of great use to the modeling of standard cell library of deep-submicrometer process. By virtue of the proposed scheme, the relationship between the rising and falling delay variations and the active area of the standard cells is experimentally shown for the first time.

Index Terms—Active area, delay variation, on-chip oscilloscope, standard cell, within-die delay.

I. INTRODUCTION

With the advancement in deep submicrometer CMOS technology beyond 65 nm, accurate characterization and measurement of delay variation of standard cells is becoming essential for design for manufacture, process optimization, and yield enhancement [1]–[5]. Meanwhile, digital systems with increasing complexity and gigabytes per second data rate today are also demanding a more accurate timing analysis. Hence, there is a demand for a measurement technique which can perform delay characterization at individual gate level.

Measuring the waveform on the single gate level from the outside of the chip is almost impossible. Using external probes is an intrusive and complex way with limited accuracy, because large parasitic LC of probes may affect the measured waveform drastically. On the other hand, the transition time of on-chip signal reaches sub-10 ps order with the latest LSIs, whose bandwidth is too high for off-chip measurement. Thus, on-chip measurement techniques have been proposed by many researchers in order to measure the on-chip delays.

Conventionally, delay variation is measured with ring oscillator or gate-chain [6]–[10] because it's easily implemented on-chip and has a high sensitivity to process parameters. However, the period of ring oscillators and gate chain is determined by the sum of delays of all the stages, so measured σ of delay is averaged to σ/\sqrt{n} , where n is the number of total stages. Thus, it is impossible to measure single-gate contributions. Even though the authors in [11] proposed a modified

Manuscript received December 14, 2010; revised May 18, 2011; accepted July 04, 2011. Date of publication August 30, 2011; date of current version July 19, 2012. This work was supported in part by Semiconductor Technology Academic Research Center (STARC). The VLSI chips were fabricated through the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo, with the collaboration by STARC.

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Digital Object Identifier 10.1109/TVLSI.2011.2162257

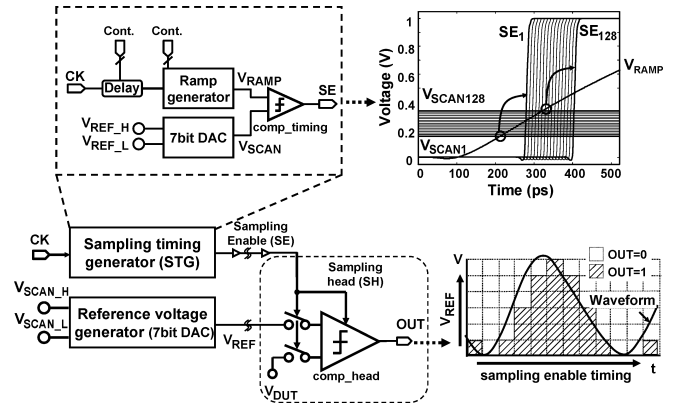


Fig. 1. Block diagram of on-chip sampling oscilloscope.

ring oscillator to characterize individual gate delay, they fail to separate the rising and falling delays, so the delay and variation with rising and falling transition are still averaged. Therefore, exploring an on-chip measurement system [12] to characterize the rising and falling delays separately is the focus of this paper. (In this paper, rising/falling delay is also referred as t_{pLH}/t_{pHL} , which means the propagation delay with a low-to-high /high-to-low transition in the output.)

Our proposed method for measuring the delay variation of standard cells utilizes the directly measured waveform of individual gate by using on-chip sampling oscilloscope [13], which is chosen because of its pico-second resolution and simple sampling head structure over prior art such as [14]. In this way, the input and output waveforms of an individual gate are captured separately, therefore enables the characterization of rising and falling delays separately. Seven types of standard cells: INV \times 1, INV \times 2, INV \times 4, NAND2, NOR2, NAND3, and NOR3 are measured with 60 DUTs for each type. Good correlations of within-die delay distributions between measured and Monte Carlo simulated results are observed. By virtue of proposed scheme, a relationship between the rising and falling delay variation and the active area is experimentally shown for the first time.

Experimental results of the test chip in 65-nm process successfully demonstrate the feasibility of measuring rising and falling delay variations of individual standard cells.

II. MEASURING WAVEFORM WITH ON-CHIP OSCILLOSCOPE

In order to measure the input and output waveform of individual standard cells directly, the on-chip sampling oscilloscope is implemented in 65 nm 1.2 V CMOS process. Fig. 1 shows the block diagram of the on-chip sampling oscilloscope, which consists of a sampling timing generator (STG), a reference voltage generator (a 7 bit DAC), and a sampling head (SH). V_{DUT} is connected to input or output of individual standard cell, and is repetitively sampled by the sampling head at sampling enable (SE) edge and compared with V_{REF} . By both scanning V_{REF} and the timing of SE, transient waveform of V_{DUT} can be converted to digital data by a voltage comparator (comp_head). Furthermore, in this operation, any random noise introduced by the on-chip sampling oscilloscope can be reduced by averaging hundreds of reconstructed waveforms.

The reference voltage generator is implemented by resistor ladder to generate 128 level of V_{REF} . V_{SCAN_L} and V_{SCAN_H} are connected to

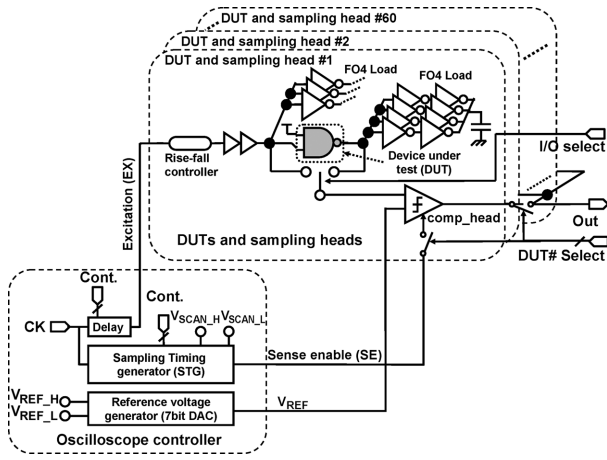


Fig. 2. Circuit schematic of within-die delay variation measurement using on-chip sampling oscilloscope.

−0.2 and 1.4 V, respectively, for a voltage range of −0.2 to 1.4 V with a 12.5-mV voltage resolution. The STG consists of a delay unit, a ramp generator, a 7 bit DAC and a voltage comparator (comp_timing). The delay unit in STG is employed to enable adjustable observing window for on-chip sampling oscilloscope. The 7 bit DAC is also implemented by resistor ladder and is used to generate 128 level of V_{SCAN} from $V_{REF_L} = 0.2$ V to $V_{REF_H} = 0.4$ V. The ramp generator produces a ramp waveform V_{RAMP} , which is then compared with 128 level of V_{SCAN} by comp_timing to provide 128 SE's with a pico-second step. Then SE is connected to SH as a scanning timing signal for a pico-second resolution of on-chip sampling oscilloscope.

III. IMPLEMENTATION OF DELAY VARIATION MEASUREMENT

Based on the above on-chip sampling oscilloscope, a scheme to measure the input and output waveform of individual standard cells is presented in Fig. 2. For one type of standard cell (shown as a NAND2 gate), 60 duplicates of DUTs and SHs are implemented to characterize within-die delay variation. The number of DUTs and SHs is chosen by a trade off of adequate number to show distribution, total available layout area, and types of standard cells to be measured.

Same comparator (comp_head) is used for measuring both input and output waveform, thus the offset of measured input and output signal brought by comparator can be cancelled out. Switch size of I/O select is carefully selected to minimize parasitic RC from DUT to comparator and the mismatch of the two channels. Inverters are employed as input and output load to DUT, as a normal situation of “fan-out 4” in a common digital system. A rise-fall controller is implemented to apply rising or falling edge of excitation (EX) signal to the DUT. Buffers from EX to DUT is sized bigger than normal, in order to introduce less variation on the buffer line, thus less disturbance on the variation of interest.

An oscilloscope controller is shared among all the 60 DUTs and SHs in order to minimize the variation introduced by the controlling circuit. The oscilloscope controller consists of a delay unit, a STG, and a reference voltage generator. The delay unit is controlled by a 6 bit digital signal to enable the tunability of timing control for EX.

Fig. 3 shows the top level block diagram of the fabricated within-die delay variation measurement circuit. Seven types of standard cells: INV×1, INV×2, INV×4 (named by increasing drivability), NAND2, NOR2, NAND3, and NOR3 are implemented with 60 DUTs for each in order to show the delay distributions. Great efforts have been made to reduce unwanted noise and variation introduced by the sampling oscilloscope control circuit, the power rail, and the signal buffers for DUTs.

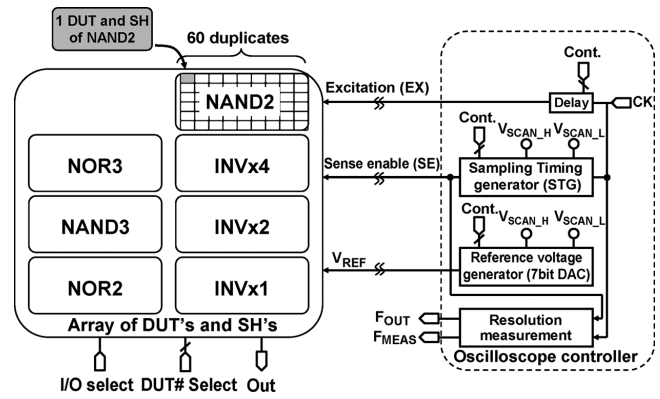


Fig. 3. Top level block diagram of within-die delay variation measurement using on-chip sampling oscilloscope.

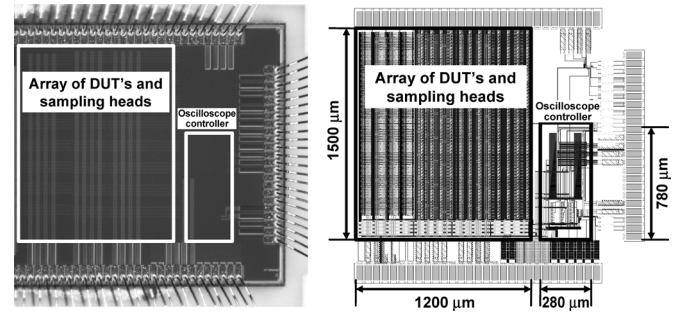


Fig. 4. Photo and layout of the test chip.

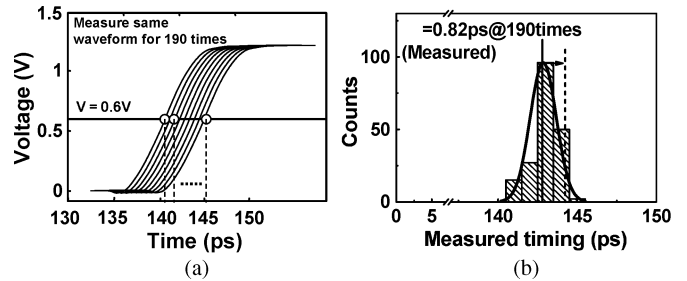


Fig. 5. (a) Measured DUT (INV×1) output waveform using the on-chip sampling oscilloscope. (b) Histogram of half V_{DD} timing of (a).

The oscilloscope controller is shared among all the 420 DUTs and SHs for the same reason mentioned above. “A resolution measurement block [13] shown in Fig. 3 is implemented to measure the timing resolution of the on-chip sampling oscilloscope. A reference ring oscillator is employed and its frequency can be measured by using frequency divider. The timing resolution (step of SE's) is measured by using calibration technique and measured result shows that the test chip achieves a minimum time resolution of 1 ps.”

The test chip is designed and fabricated in 65 nm bulk CMOS process. Fig. 4 shows the chip microphotograph and the layout. The total 420 DUT's and 420 sampling heads consumes an area of $1200 \mu\text{m} \times 1500 \mu\text{m}$, and the oscilloscope controller occupies $280 \mu\text{m} \times 780 \mu\text{m}$.

IV. MEASUREMENT RESULTS AND ANALYSIS

Rising and falling delays of 7 types, 420 DUTs are measured with 1.2 V V_{DD} . Measurement is at first carried out to evaluating the timing error introduced by the on-chip sampling oscilloscope. The noise due

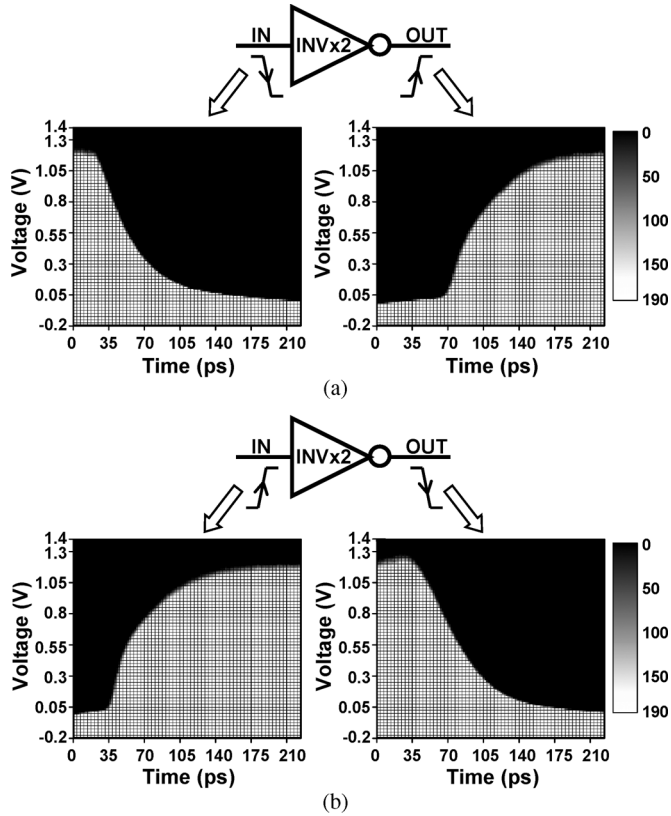


Fig. 6. Measured waveforms of an inverter with (a) rising output transition and (b) falling output transition.

to on-chip sampling oscilloscope can be reduced by averaging several reconstructed waveforms. In this study, each waveform is sampled 190 times and averaged to suppress random noise introduced by the sampling oscilloscope. Time interleave between each measurement is 500 ns. In order to evaluate the timing error, one DUT output (INV \times 1) is measured 190 times, and the time when the measured waveform crosses 0.6 V (half V_{DD}) is extracted in Fig. 5(a). Histogram of the measured half V_{DD} timing is shown in Fig. 5(b). It is observed that by measuring the same waveform for 190 times, the proposed scheme has a σ error of 0.82 ps, which is quite small compared with the delay of DUTs, thus ensure the measurement accuracy of on-chip transition signal. It is also smaller than the accuracy of 1 ps reported in [11], which is a ring oscillator-based design.

Fig. 6 shows the measured input and output waveforms of an INV \times 2 gate with rising output transition and falling output transition. 1.2 V V_{DD} is applied in the measurement. In this way, the rising and falling delays of each DUT are measured for the within-die delay variation. The histogram of within-die delay variations of 7 standard cells with rising output transition and falling output transition is shown in Fig. 7. The distribution is observed to be close to normal. The measured results are in accordance with well-known knowledge that the σt_{pd} from INV \times 1, INV \times 2 to INV \times 4 are decreasing because of the increasing gate area. Also, as expected, in the rising/falling transition, NOR3/NAND3 is observed to be the slowest, because there are three pMOSs/nMOSs in series from output to power/ground.

Fig. 8 shows the within-die delay distribution map with rising and falling output transition, respectively. The positions of totally 420 DUTs are corresponding to the actual test chip shown in Fig. 4. As shown in Fig. 8, the within-die delay variation is random and no systematic component due to IR-drop on power lines is observed, because ultra wide metals and multiple pads are used for power supply

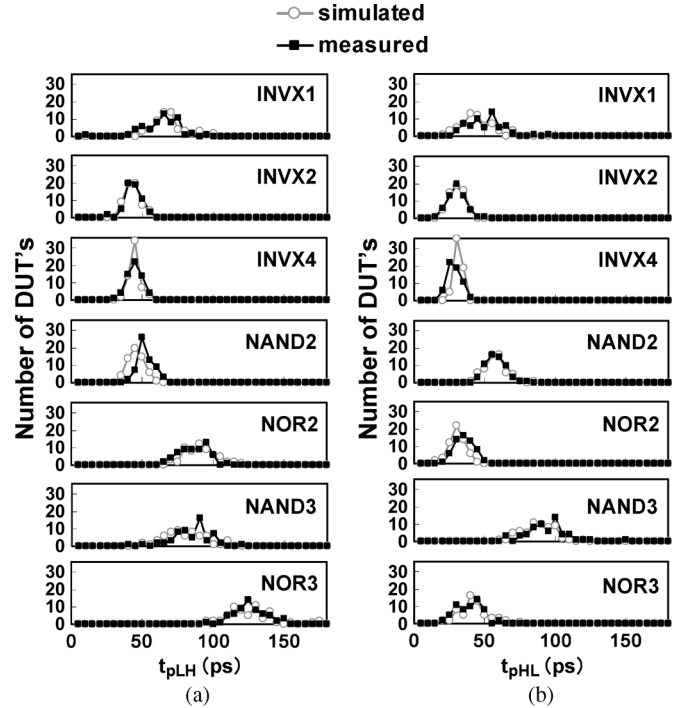


Fig. 7. Histogram of measured and simulated delay among 60 DUTs of 7 types of standard cells: (a) t_{pLH} and (b) t_{pHL} .

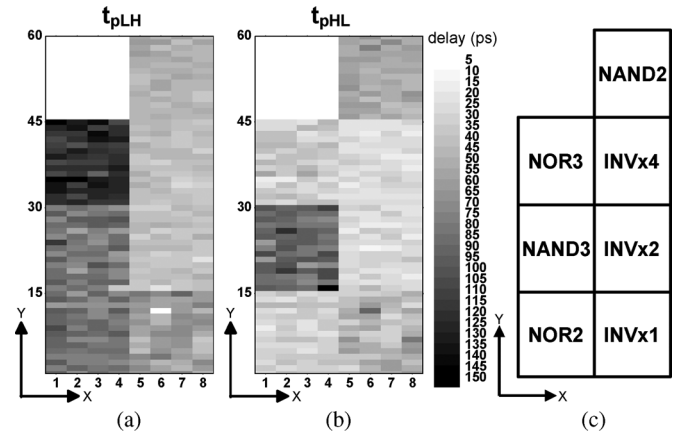


Fig. 8. Within-die delay distribution of (a) t_{pLH} , (b) t_{pHL} , and (c) actual layout of DUT's corresponding to (a) and (b).

and ground, moreover, power supply and ground are connected to each DUT through crossed metal layers.

Monte Carlo simulation has been carried out for the 7 types of standard cells with 60 samples each, with rising and falling output, respectively. Simulation is carried out by SPICE with after LPE netlist, and very close results are observed in Fig. 7 for simulated and measured result. Because the variations of gate length and oxide thickness and other effects that are not able to be included in the Monte Carlo simulation, parameters like A_{VT} , ΔV_T , and gamma are modified in the simulation. Fig. 9 shows the comparison of measured and simulated average delay with rising output transition and falling output transition. Great correlation for all types of standard cells can be observed.

As well acknowledged, for rising and falling output, the transition is a result of conduction through the devices in the path from output to the power or ground rail. Therefore, for a rising/falling output, the active transistors on the transition path will be the significant contributors to

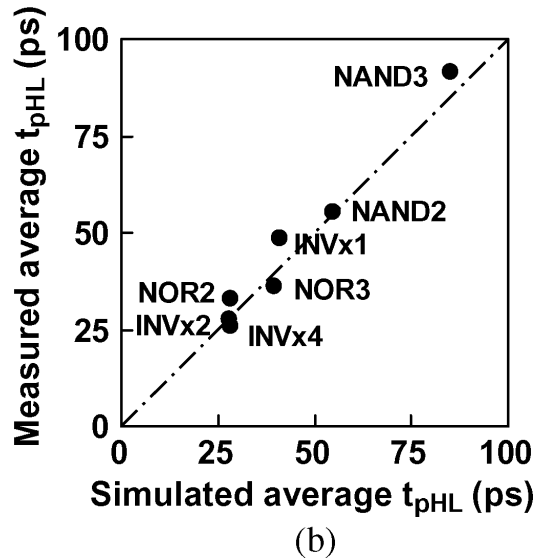
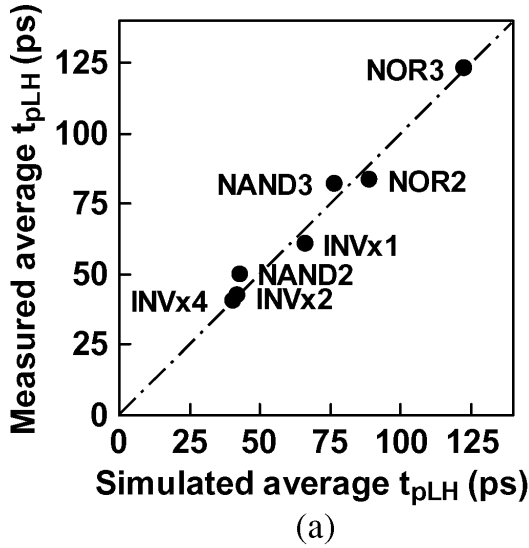


Fig. 9. Comparison of measured and simulated average delay. (a) t_{pLH} . (b) t_{pHL} .

the delay variation, as depicted in Fig. 10. In this way, we can calculate the active area of each type of DUT by summing the gate area of active transistors, with both rising output transition and falling output transition.

Fig. 11 shows the measured $\sigma t_p / \text{average } t_p$ ($\sigma t_p / \mu t_p$), the x-axis is chosen to be $1 / \sqrt{\text{Active area}(\mu\text{m}^2)}$, where active area is calculated by the total gate area of active transistors at rising and falling transition.

Variation of threshold voltage (σV_T) is known to be proportional to $1 / \sqrt{W \times L}$ [15]. As shown in Fig. 11, $\sigma t_p / \mu t_p$ has strong correlation with $1 / \sqrt{\text{Active area}(\mu\text{m}^2)}$, which is similar to the relationship between σV_T and $1 / \sqrt{W \times L}$. Moreover, the gradient of Fig. 11(b) is bigger than Fig. 11(a), which reveals a simple concept that nMOSs have bigger variation than pMOSs, because the gate area of nMOSs are smaller than that of pMOSs and A_{VT} of nMOSs is larger than that of pMOSs.

In the conventional methods, because t_{pLH} and t_{pHL} are mixed together, the dependency of $\sigma t_p / \mu t_p$ on active area shown in Fig. 11 is impossible to be measured. By measuring t_{pLH} and t_{pHL} separately, such dependency is shown for the first time.

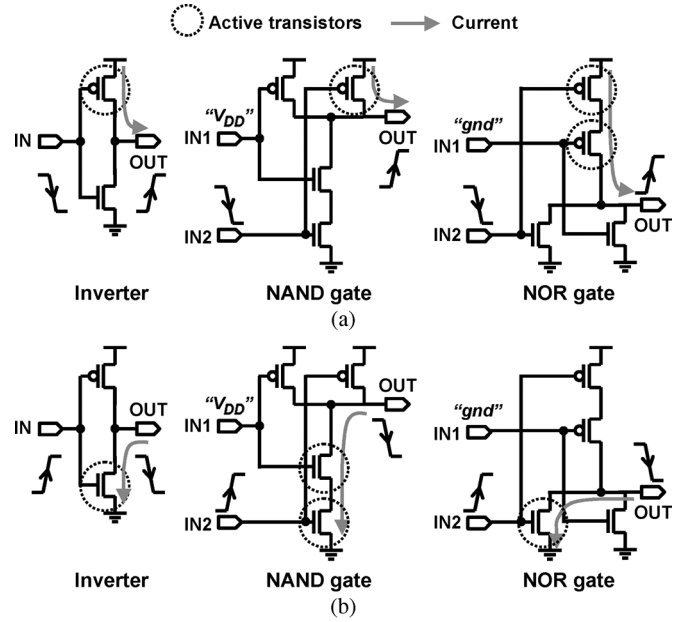


Fig. 10. Active transistors in DUTs with (a) rising output transition, and (b) falling output transition.

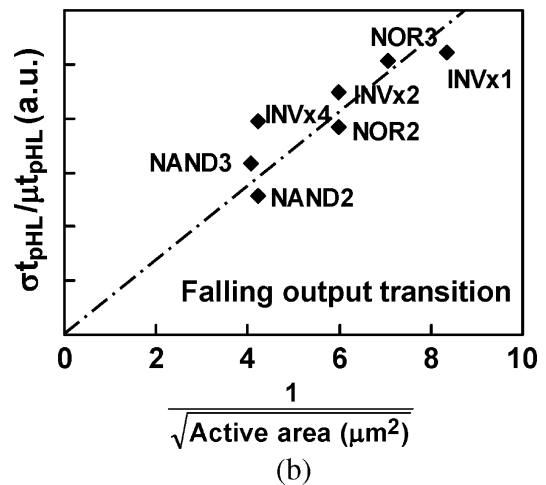
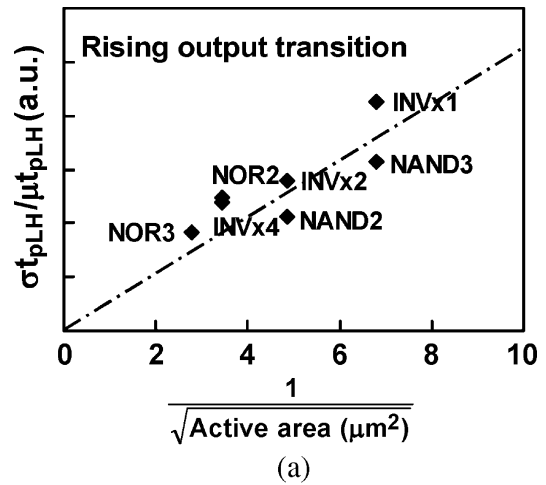


Fig. 11. Measured $\sigma t_p / \text{average } t_p$ ($\sigma t_p / \mu t_p$) with (a) rising output transition, and (b) falling output transition.

V. CONCLUSION

The proposed measurement system is able to characterize rising and falling delay variations separately by directly measuring the input and output waveforms of individual gate. 7 types of standard cells: $INV \times 1$, $INV \times 2$, $INV \times 4$, $NAND2$, $NOR2$, $NAND3$, and $NOR3$ in 65-nm process are measured with 60 DUT's for each type. Good correlations of within-die delay distributions between measured results and Monte Carlo simulated results are observed. The measured results of rising and falling delay are of great use to the modeling of standard cell library of deep-submicrometer process. By virtue of the proposed method, the relationship between the rising and falling delay variations and the active area is experimentally shown for the first time.

ACKNOWLEDGMENT

The authors would like to thank M. Murakata, K. Inagaki, and Y. Nakamura for the useful discussions.

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A High Performance Switched Capacitor-Based DC-DC Buck Converter Suitable for Embedded Power Management Applications

Biswajit Maity and Pradip Mandal

Abstract—Here, we propose high performance buck converter architecture suitable for embedded applications. The proposed converter has high power efficiency, high power density, good driving capability, low output ripple, and good line and load regulation. The step down converter is constructed using a simple building block called cross coupled converter. As this block use low swing internal signals to control half of its switches, the required switching loss decreases and these internal control signals enable us to use thin oxide transistor for making switch smaller and reducing power further. In addition, converter uses all the good features of non-overlapping rotational interleaving switching scheme. Switching frequency of the converter is dynamically adjusted based on load current to maintain high power efficiency. Good transient performance is achieved by using dynamic leaker circuit with a marginal increase of static current. The converter is designed in 0.18- μm CMOS process to get regulated 1.3–1.6 V output from 3.3 V input supply while output ripple is below 42 mV and provides 86% peak power. For 75% power efficiency, power density of the converter is 0.43 W/mm² using total 490 pF capacitor.

Index Terms—Controlled cross-coupled, frequency control (FC), non-overlapping rotational time interleaving (NRTI) switching scheme, shoot through (ST) current, switched-capacitor (SC).

I. INTRODUCTION

Since long back switched-capacitors (SCs) are used for DC-DC converters [1], [2]. But there is a recent trend to use these SC based DC-DC converter for embedded power management applications in order to achieve high power efficiency and power density. SC converter of [3] has high power efficiency but, it uses off-chip capacitor to keep output ripple at acceptable level. On the other hand, for high dropout applications, SC converter and linear regulator are combined to develop a hybrid converter [4]. Converter has 200 mV ripple with 200 pF load capacitor to get 1.05 regulated outputs. Such high ripple at the output is not suitable for embedded applications. In [5] the on-chip output capacitor is implemented but the power efficiency remains low and the output ripple is high due to unavailability of large flying capacitor and load capacitor for such embedded applications. The output ripple is reduced with less output capacitor in [6]–[8] by increasing effective switching frequency using interleaving switching schemes. Though shoot through (ST) current reduction technique is discussed in [7], but in [9] total ST current is eliminated by using non-overlapping rotational time interleaving (NRTI) switching scheme and power efficiency is improved. In addition, output ripple is also reduced in the converter. One drawback of NRTI, however, is power overhead due its control signal generation and control signal swing. In SC boost converter [10], [11], cross-coupled techniques are used to make use of internal node voltages as control signal. This helps to improve power efficiency by reducing dynamic

Manuscript received May 21, 2010; revised November 18, 2010, February 12, 2011, and May 14, 2011; accepted July 19, 2011. Date of publication August 22, 2011; date of current version July 19, 2012. This work was supported by the National Semiconductor Corporation.

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Digital Object Identifier 10.1109/TVLSI.2011.2163206