An 80 mV Startup Dual-Mode Boost Converter by Charge-Pumped Pulse Generator and Threshold Voltage Tuned Oscillator With Hot Carrier Injection

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***Abstract*—This paper presents an 80 mV startup-voltage dual-mode boost converter for energy harvesting applications. The charge-pumped pulse generator enables a startup operation of the boost converter from the input voltage of 80 mV. The threshold voltage tuned oscillator for the clock generator of the boost converter compensates for the die-to-die process variation by a hot carrier injection (HCI), thereby reducing the minimum operation voltage (V_{DDMIN}) of the clock generator by 45% with a trimming time of 10 minutes. The proposed step-up converter achieves the lowest startup voltage without using a mechanical switch or a large transformer.**

***Index Terms*—Charge-pumped pulse generator, dual-mode boost converter, energy harvesting, hot carrier injection, low voltage, startup, V_{TH}-tuned oscillator.**

I. Introduction

RECENTLY, wireless sensors are widely employed in various applications including environmental monitoring, energy consumption monitoring, and implantable medical sensors. There is a strong demand that those sensors could be self powered where direct power supply is inefficient and battery replacement is difficult. Various battery-free energy harvesters have been developed for such self powered applications [1]–[3]. One of the most critical problems of these energy harvesters is that the voltage provided by them is significantly less than the voltage required by most of the modern integrated circuits. Thus, it greatly limits the use of energy harvesters with integrated circuits like wireless sensors in a self powered system. For example, the thermoelectric generator can generate the output voltage that is proportional to the difference of the temperatures on both sides of it, in the range of 10 mV/K to 50 mV/K. For body-wearable applications, the output voltage is less than 100 mV for temperature difference of 2 K. The single-cell solar cell generates 500–600 mV in the outdoor and becomes as low as 100–200 mV in the dark office environment. With such low output voltages of the energy harvesters, the step-up DC-DC converter that can accommodate low input voltage and boost the harvested energy to usable output voltage is of great importance for a self powered system.

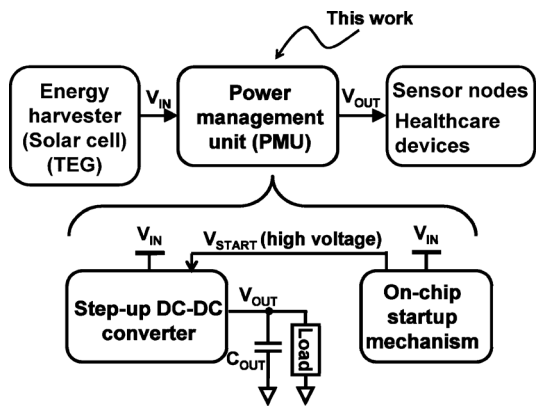

Fig. 1. Power management unit for energy harvesting applications.

Fig. 1 illustrates the power management unit for energy harvesting applications. It up-converts the harvested energy and provides a higher voltage to wireless sensors or healthcare devices. On-chip startup mechanism is applied for low-cost, compact applications because no additional off-chip devices are required. It provides high-voltage stimulus (V_{START}) to the step-up DC-DC converter and kick-start the system from extremely low input voltage (V_{IN}).

In this paper, an 80 mV startup-voltage dual-mode boost converter is proposed [4] for energy harvesting applications. Dual-mode operation means that the startup mode and the operation mode are both realized by an inductive step-up DC-DC converter. A charge-pumped pulse generator (CPPG) provides a large amplitude pulse signal to the power transistor and startup the system from 80 mV V_{IN} in 4.8 ms. It achieves the maximum conversion efficiency of 72% at 0.5 mA output current with 50 mV V_{IN}. A V_{TH}-tuned oscillator with HCI (DC-stress) compensates for the die-to-die process variation and the program time can be 20 times shorter than the conventional AC-stress [5], thereby reducing the test cost. The V_{DDMIN} of the oscillator is reduced from 128 mV to 80 mV in 3 minutes and can be

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as low as 70 mV after 10 minutes of programming. The proposed circuit demonstrates the feasibility of countermeasures for the process variation that limits the V_{DDMIN} of a CMOS ring oscillator.

This paper is organized as follows. Startup techniques in low input voltage DC-DC converters are introduced in Section II. Section III shows the system architecture of the proposed dual-mode boost converter. Section IV explains the V_{TH}-tuned oscillator with HCI. Section V describes the circuit implementation of the proposed charge-pumped pulse generator. The experimental results and comparison with the state-of-the-art are shown in Section VI. Finally, a conclusion is given in Section VII.

II. Startup Techniques in DC-DC Converters

The key challenge of the power management unit for energy harvesting applications is to develop a startup mechanism [6]. The startup mechanism is used to generate a high-voltage stimulus to kick start the step-up DC-DC converter (Fig. 1). Once the converter starts working, the control circuits in the converter can be powered by the output (V_{OUT}) and the converter functions even V_{IN} is lower than startup voltage.

Until now, several startup techniques were reported [7]–[11] for low voltage operation. A 650 mV external voltage and a 2 V battery are directly provided to the output of the power management unit in [7] and [8], respectively. For battery-free applications, however, no auxiliary voltage can be provided to the system. A battery-less 35 mV startup boost converter in [9] uses a vibration activated mechanical switch instead of the auxiliary voltage. The mechanical switch requires a non-standard process and the vibration requirement limits the applications. A completely electronic startup step-up converters using a transformer with a large turn ratio was presented in [10], [11]. The transformer is not well suitable for portable applications and it also causes larger conduction loss.

To alleviate these problems, the completely electronic, on-chip startup techniques without a mechanical switch or a transformer were presented in [12] and [5]. In [12], an on-chip charge pump (CP) was designed as a startup mechanism and provides a high voltage to the boost converter. The startup voltage of the DC-DC converter is limited to 180 mV because the load circuits of CP consume too much power. In [5], a 95-mV startup voltage step-up DC-DC converter was realized by the capacitor pass-on scheme with PMOS super cut-off technique. An on-chip CP charges the output capacitor (C_{OUT}) during startup and its load circuits are minimized to reduce the output current of the CP. The available output current of the CP depends on V_{IN} and the output voltage decreases as V_{IN} decreases. Even though it uses PMOS super cut-off technique to reduce the drain leakage of the power transistors, the startup voltage is still limited to 95 mV.

Fig. 2 shows the simulated leakage current of PMOS power transistor versus V_{START} under a temperature of 300 K for different configurations. The drain leakage is around 1 μA at 0.5 V V_{START} and becomes as low as 0.2 nA by applying PMOS super cut-off technique. The gate leakage current is approximately 10 times smaller than the drain leakage current with

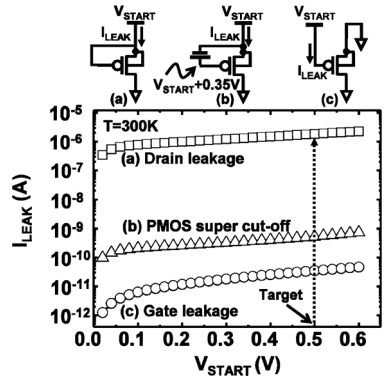

Fig. 2. Simulated leakage current of PMOS power transistor versus V_{START}. (a) Drain leakage. (b) Drain leakage current with PMOS super cut-off. (c) Gate leakage.

PMOS super cut-off. Therefore, charging the gate of power transistor during startup is a possible solution to reduce the output current of the on-chip charge pump, which limits the startup voltage of the boost converter.

In this paper, a dual-mode boost converter is proposed to further reduce the startup voltage. Fig. 3 shows the operation concept of the startup mechanism. M_N, M_P, L_1 and C_{OUT} built up the conventional boost converter while M_S is an additional power transistor for startup. The startup circuit charges and discharges the gate of power transistor M_S with high amplitude ($\sim$0.5 V). The energy is stored in L_1 in charging phase and transferred to C_{OUT} in discharging phase. Comparing with starting by the on-chip charge pump [5], the proposed inductive startup mechanism provides larger current to C_{OUT} during startup because M_S turns on well. Therefore, the startup time can be significantly reduced. The proposed scheme eliminates the drain current problem in [5] and the startup voltage can be reduced to 80 mV.

III. System Architecture

The detailed block diagram of the proposed dual-mode boost converter is shown in Fig. 4. The switch status in this figure represents the initial state. O_1 and O_2 are the control signals for the switches. The proposed dual-mode boost converter consists of the conventional boost converter, a V_{TH}-tuned oscillator with HCI, a charge-pumped pulse generator (CPPG), two voltage detectors (VD_1, VD_2) [5], and a pulse generator for operation. An additional power transistor M_S is designed for startup. The V_{TH}-tuned oscillator with HCI generates the clock signals (CK_{CP}) for CPPG under 80 mV V_{IN}. CPPG provides a high-amplitude high-duty clock signal to M_S and kicks start the boost converter. The pulse generator for operation is used to provide a pulse signal with fixed duty cycle to the power transistors M_N and M_P during operation. In our design, the target is to verify the on-chip startup mechanism in DC-DC converter. The pulse-width modulation circuit is not included in this scheme and the output voltage is not regulated.

The size of the external components (L_1, C_{OUT}) is determined by the design specification. The target V_{IN}, V_{OUT}, I_{OUT}, the output ripple $(\triangle V_{OUT})$, and the switching frequency (f_S) are 80 mV, 1.3 V, 1 mA, 0.1 V, and

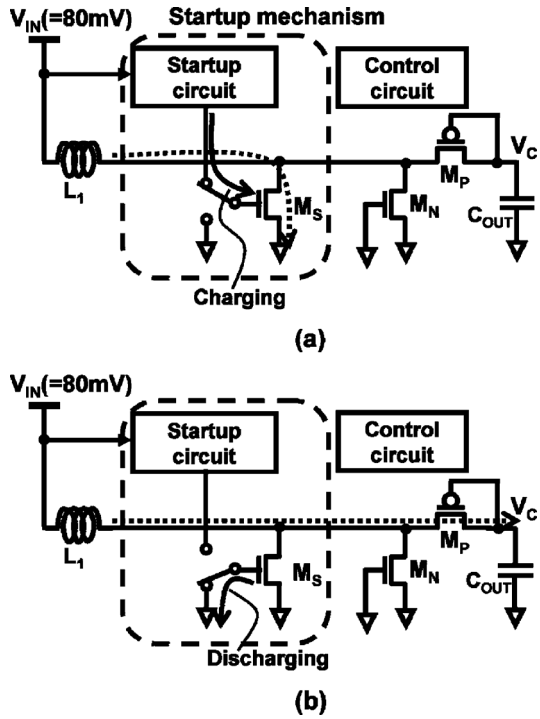

Fig. 3. Operation concept of proposed startup mechanism. (a) Charging of the gate of $\mathrm{M_S}$. (b) Discharging of the gate of $\mathrm{M_S}$.

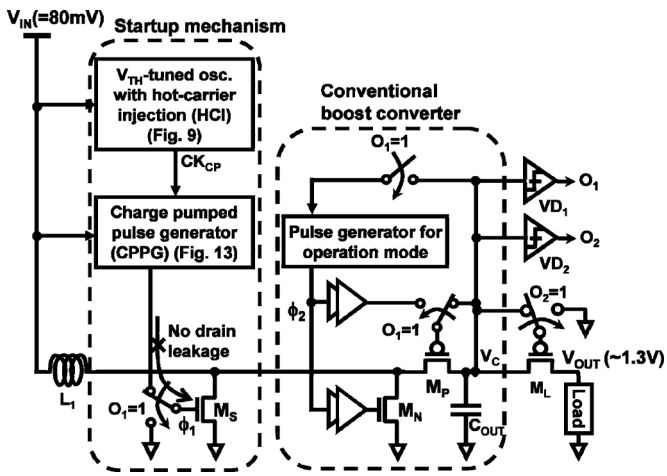

Fig. 4. Proposed dual-mode boost converter. Startup is achieved by charging $\mathrm{C_{OUT}}$ by driving power transistor $\mathrm{M_S}$ with CPPG.

2 MHz, respectively. The estimated conversion efficiency (η) at $\mathrm{V_{IN}} = 80$ mV is 60%. Therefore, $\mathrm{C_{OUT}}$ is approximately derived from the following equation:

$$\mathrm{C_{OUT(min)}} = \frac{\mathrm{I_{OUT}} \times \mathrm{D}}{\eta \times \mathrm{f_S} \times \Delta \mathrm{V_{OUT}}} \approx 8\ \mathrm{nF} \tag{1}$$

where the duty cycle (D) can be calculated from

$$\mathrm{D} = 1 - \frac{\mathrm{V_{IN}} \times \eta}{\mathrm{V_{OUT}}} \approx 0.96. \tag{2}$$

The inductance of $\mathrm{L_1}$ depends on the inductor ripple $(\triangle \mathrm{I_L})$. Generally, the inductor ripple range is 20% to 40% of the maximum input current and we use 30% for calculation. The inductor ripple and inductance of $\mathrm{L_1}$ can be calculated from the following equation:

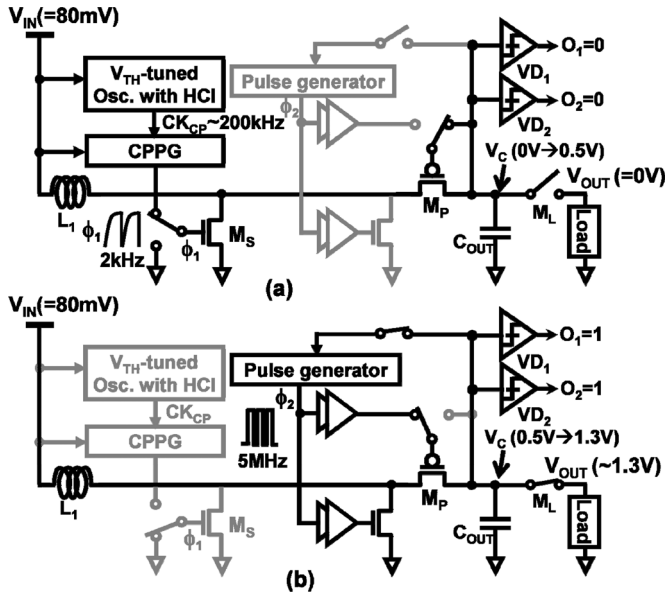

Fig. 5. Dual mode in the proposed boost converter (a) Startup mode ($\mathrm{V_C} \leq 0.5$ V) with low input voltage. (b) Operation mode ($\mathrm{V_C} \geq 0.5$ V) with high efficiency.

$$\Delta \mathrm{I_L} = 0.3 \times \mathrm{I_{OUT}} \times \frac{\mathrm{V_{OUT}}}{\mathrm{V_{IN}}} \approx 5\ \mathrm{mA} \tag{3}$$

$$\mathrm{L_1} = \frac{\mathrm{V_{IN}} \times (\mathrm{V_{OUT}} - \mathrm{V_{IN}})}{\Delta \mathrm{I_L} \times \mathrm{f_S} \times \mathrm{V_{OUT}}} \approx 7.5\ \mu\mathrm{H}. \tag{4}$$

Therefore, an off-chip inductor of 6.8 μH and an off-chip capacitor of 10 nF are applied in this design.

The dual mode operation of the proposed boost converter is illustrated in Fig. 5. Fig. 5(a) shows the startup mode with low startup voltage and Fig. 5(b) shows the operation mode with high conversion efficiency. These modes can be automatically changed by detecting the capacitor voltage $(\mathrm{V_C})$ by $\mathrm{VD_1}$. When $\mathrm{V_C} < 0.5$ V, $\mathrm{VD_1}$ provides "low" signal and the converter is operating under startup mode. Otherwise, $\mathrm{VD_1}$ provides "high" and the converter is in operation mode. $\mathrm{VD_2}$ turns on the switch $\mathrm{M_L}$ when $\mathrm{V_C}$ is higher than 0.6 V. The trigger voltage of $\mathrm{VD_2}$ is slightly higher than that of $\mathrm{VD_1}$ to make sure the load is connected to $\mathrm{V_C}$ after the boost converter starts working and the output can be boosted smoothly. An additional switch $\mathrm{M_L}$, however, reduces the conversion efficiency of the boost converter. To reduce the conduction loss caused by $\mathrm{M_L}$, the transistor size of $\mathrm{M_L}$ is designed to be twice of $\mathrm{M_P}$. If the load current increases and $\mathrm{V_{OUT}}$ is smaller than 0.6 V, $\mathrm{M_L}$ will turn on and off repeatedly.

The waveforms illustrating the circuit operation sequences are illustrated in Fig. 6. During startup, the $\mathrm{V_{TH}}$-tuned oscillator with HCI provides the clock signal $(\mathrm{CK_{CP}})$ to CPPG at 80 mV $\mathrm{V_{IN}}$. CPPG is designed to convert an 80 mV input to a high-amplitude high-duty clock signal to drive the power transistor $\mathrm{M_S}$. The amplitude of $\mathrm{CK_{CP}}$ is designed to be 0.5 V, which is higher than the threshold voltage $(\mathrm{V_{TH}})$ of the power transistors. High duty-cycle is required to store the enough energy in the inductor

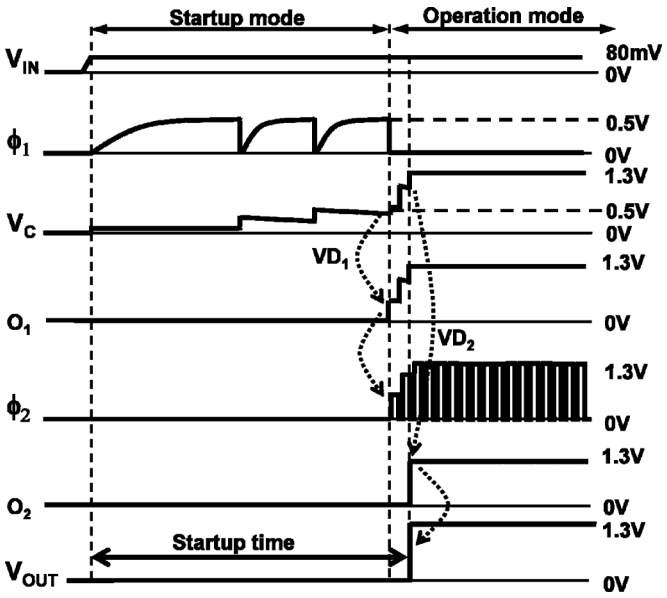

Fig. 6. Waveforms illustrating the circuit operation sequences.

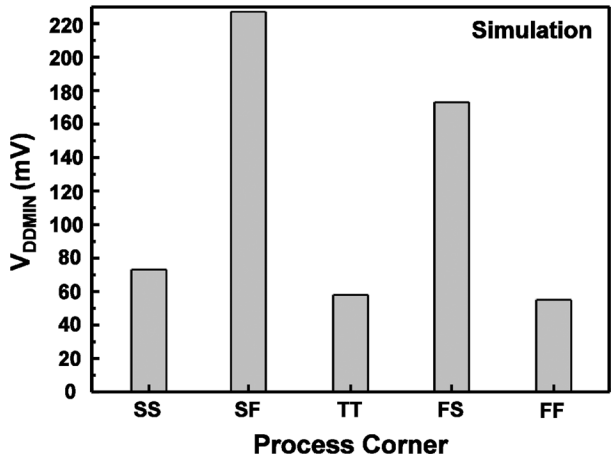

Fig. 7. Simulation results of $\mathrm{V_{DDMIN}}$ of CMOS ring oscillator under different process corners. SS means slow NMOS and slow PMOS, SF means slow NMOS and fast PMOS, and so on.

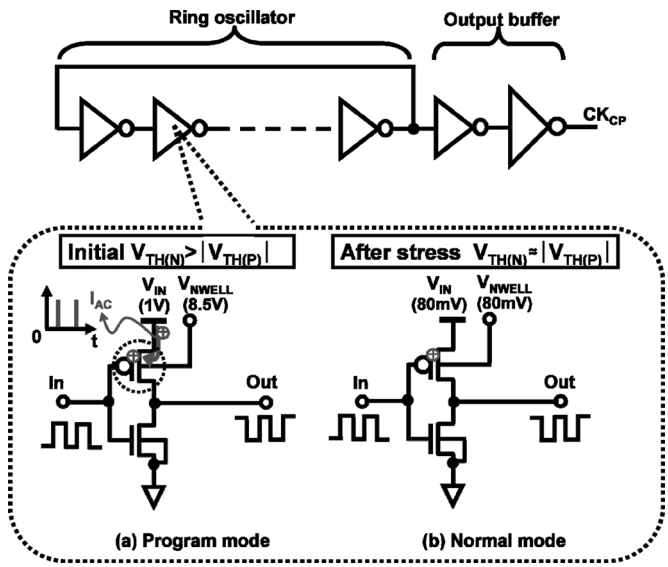

Fig. 8. Circuit schematic of conventional $\mathrm{V_{TH}}$-tuned oscillator with AC stress in [5]. (a) Program mode. (b) Normal mode.

during startup. When ϕ_1 is high, $\mathrm{M_S}$ turns on and the inductor current increases. If ϕ_1 changes from high to low, $\mathrm{M_S}$ turns off and the current stored in the inductor $\mathrm{L_1}$ flows through the diode connected PMOS transistor $\mathrm{M_P}$. Therefore, $\mathrm{C_{OUT}}$ is charged by the inductor current and $\mathrm{V_C}$ increases.

When $\mathrm{V_C}$ is charged to the preset trigger voltage of $\mathrm{VD_1}$, the state changes and the boost converter is operating under operation mode. During operation mode, the charge stored in $\mathrm{C_{OUT}}$ activates the pulse generator and the pulse generator drives the power transistors $\mathrm{M_N}$ and $\mathrm{M_P}$ with high amplitude $(\mathrm{V_C})$ to achieve high conversion efficiency. When $\mathrm{V_C}$ is higher than the preset trigger voltage of $\mathrm{VD_2}$, the switch $\mathrm{M_L}$ turns on to power the load circuits.

IV. $\mathrm{V_{TH}}$-Tuned Oscillator With Hot Carrie r Injection

The $\mathrm{V_{TH}}$-tuned oscillator with HCI is used to generate the clock signals for CPPG. The startup mechanism fails if the oscillator does not function. Therefore, the minimum operation voltage $(\mathrm{V_{DDMIN}})$ of the oscillator also limits the startup voltage of the boost converter in standard CMOS process.

The $\mathrm{V_{DDMIN}}$ of an oscillator is usually limited by $\mathrm{V_{TH}}$ unbalance between NMOS and PMOS transistors. Fig. 7 shows the simulation results of $\mathrm{V_{DDMIN}}$ of CMOS ring oscillator under different process corners. SS means slow NMOS and slow PMOS. SF means slow NMOS and fast PMOS, and so on. The simulation results show that $\mathrm{V_{DDMIN}}$ of lower than 80 mV can be achieved if the $\mathrm{V_{TH}}$ of NMOS and PMOS transistors are well balanced. If we can adjust the $\mathrm{V_{TH}}$ of transistors, for example, by adjusting fast NMOS slow PMOS to slow NMOS slow PMOS; $\mathrm{V_{DDMIN}}$ can be reduced from 173 mV to 73 mV.

$\mathrm{V_{TH}}$ unbalance in CMOS technology is usually caused by within-die and die-to-die process variations. The within-die process variation issue can be easily solved by increasing the transistor width in this design. The die-to-die process variation is usually adjusted by controlling the body bias of the transistors. In the startup circuit, however, the body-biasing circuit would not function before the system startup because only the input voltage exists in the system. Therefore, the die-to-die process variation limits the $\mathrm{V_{DDMIN}}$ in our applications. One possible way to compensate for the die-to-die process variation is trimming the transistors in post-fabrication process. In this process, the ideal power supply is available to program the transistors. A $\mathrm{V_{TH}}$-tuned oscillator trimmed by AC stress is firstly reported in [5], as shown in Fig. 8. In program mode, the oscillator functions under 1 V input voltage and AC current $(\mathrm{I_{AC}})$ draws through the transistor. PMOS transistor is trimmed by applying high reverse body bias ($\mathrm{V_{NWELL}} = 8.5$ V) and $\mathrm{V_{TP}}$ increases. It requires 60 minutes for programming because only AC current draws in program mode.

To reduce the program time, we proposed a $\mathrm{V_{TH}}$-tuned oscillator with HCI (DC-stress), as shown in Fig. 9. The circuit consists from an 11-stage inverter-based ring oscillator and inverter-based output buffers. The transistors $\mathrm{M_{NP}}$ and $\mathrm{M_{PP}}$ are added to provide DC current path for programming. To avoid

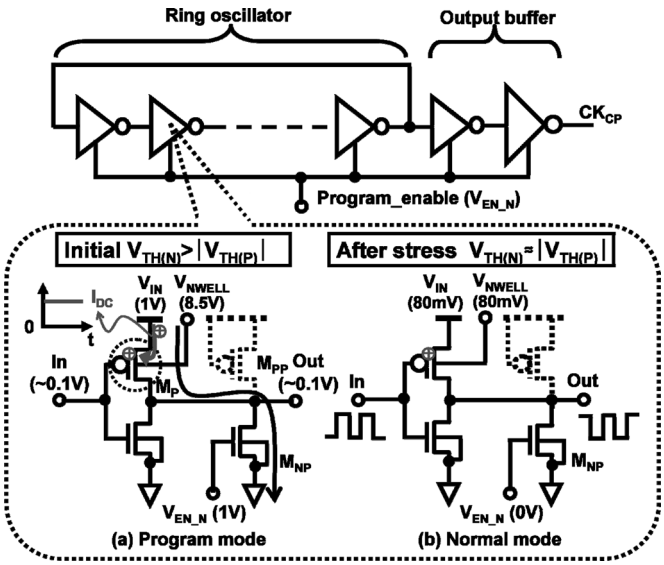

Fig. 9. Circuit schematic of proposed V_{TH}-tuned oscillator with HCI (DC stress). (a) Program mode. (b) Normal mode.

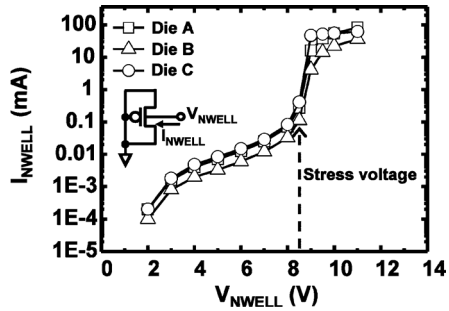

Fig. 10. Measured dependences of body current (I_{NWELL}) on the well voltage (V_{NWELL}).

the within-die process variation, the transistor width of the inverter is designed to be 64 times larger than standard cell. In the following, only the PMOS programming will be introduced for easier understanding.

In program mode, a high reverse body bias is applied to PMOS transistors ($V_{NWELL} = 8.5$ V) while the body of NMOS transistors are connected to its source. The enable signal (V_{EN_N}) of 1 V is applied to M_{NP} and the output voltage (Out) is pulled-down to low ($\sim$0.1 V). In this scheme, the input (In) is the output of the previous stage and the input voltage is also low ($\sim$0.1 V). Therefore, M_P is turned on and a large DC current flows through M_P. During program mode, $|V_{TP}|$ is much higher than V_{TN} because the high reverse body bias is applied to PMOS transistors and the input/output voltages remain low even both M_P and M_{NP} turn on. A high reverse body bias of M_P enables the positive charges injected into the gate dielectrics of transistors. The injected charges are fixed in the dielectrics and increases V_{TP} even the high reverse body bias is removed. Note that V_{TP} shift shows nonvolatile characteristics and does not require any additional process steps. Since the body of NMOS transistors are connected to its source, V_{TN} is not programmed. Comparing with AC stress, DC stress increases the current flowing through M_P and reduces the program time significantly.

When $|V_{TP}|$ is balanced with V_{TN}, the post-fabrication programming is stopped. The circuit is then operating under normal mode and only an 80 mV input is provided without any reverse body bias. The injected positive charges are still fixed in PMOS transistors even the high reverse body bias is removed. Therefore, $|V_{TP}|$ is still balanced with V_{TN} and V_{DDMIN} of the oscillator is reduced. In our design, the V_{TH}-tuned oscillator needs to operate under 80-mV V_{IN} and provide clock signals to CPPG.

Fig. 10 shows the measured dependences of body current (I_{NWELL}) on the well voltage (V_{NWELL}). From the measurement, the breakdown voltage of p-n junction is between 8.5 V to 9 V. The program time is related to the bias condition of the PMOS transistor and a higher reverse body bias reduces the program time. To reduce the program time, we manually increase V_{NWELL} until I_{NWELL} reaches 1 mA. Therefore, an 8.5-V V_{NWELL} is applied for this programming. The reverse body bias is limited by the p-n junction breakdown voltage and the supply voltage is limited by the gate breakdown voltage because of reliability consideration. In both AC and DC stress, V_{gs} and V_{gd} of the transistors are lower than the gate breakdown voltage and V_{WELL} is 8.5 V.

The program time also depends on V_{IN}. A higher V_{IN} increases the DC current and reduces the program time. V_{IN} is limited by gate breakdown voltage and available DC current. A large DC current occurs during programming because the transistor width of the output buffer is large. Therefore, V_{IN} is selected to 1 V in our design. This bias condition is the same as AC stress and is easier to compare the program time between these two methods.

In this session, we focus on PMOS programming to compensate for the die-to-die process variation. If V_{TP} is higher than V_{TN} in fabricated chips, NMOS programming is also available. M_{PP} needs to turn on to provide a DC path and a high reverse body bias can be provided to M_N to increase V_{TN}.

V. Charge-Pumped Pulse Generator

The CPPG is the key building block in the proposed dual-mode boost converter. It converts a low V_{IN} to a high-amplitude high-duty pulse signal (ϕ_1) to activate the power transistor M_S. The conventional approach uses a Dickson charge pump [13], a ring oscillator, and a duty cycle generator, as shown in Fig. 11. The Dickson charge pump converts V_{IN} to a higher level (>0.5 V). Fig. 12 shows the simulated output voltages of the 30-stage Dickson charge pump under different output currents and input voltages. The capacitance of each flying capacitor in the charge pump is 1 pF. CK_{CP} is provided from an on-chip 11-stage CMOS oscillator and the clock frequency depends on V_{IN}. The duty cycle of the clock signal is 50% and the clock frequency is 200 kHz when $V_{IN} = 80$ mV. Even though the clock amplitude provided to the circuit is much smaller than V_{TH}, there still exists the current difference between I_{ON} and I_{OFF}. Therefore, the charge pump can still build up the high output voltage from V_{IN} if the output current is small enough. From the simulation, the output current of the charge pump is limited to 4 nA. To generate a high-amplitude pulse signal with

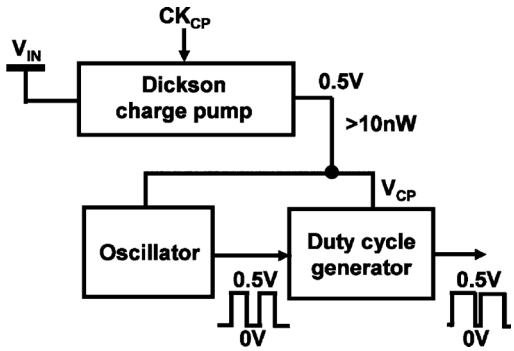

Fig. 11. Block diagram of conventional approach to generate a high-amplitude high-duty clock signal for boost converter.

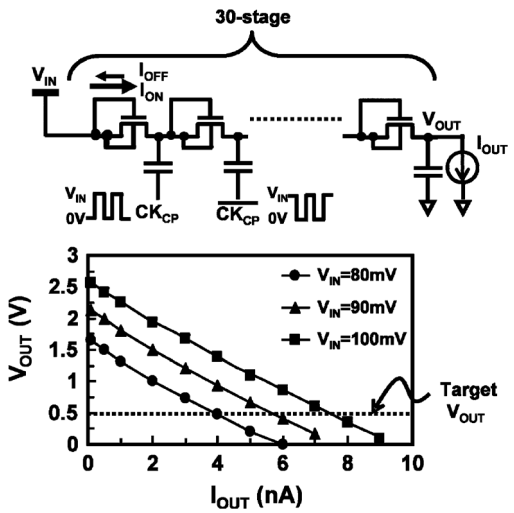

Fig. 12. 30-stage Dickson charge pump. (a) Circuit schematic. (b) Simulated dependence of output voltage on output current under different input voltage.

such a low output current, we proposed a charge-pumped pulse generator (CPPG). Fig. 13 shows the block diagram of the proposed circuit. It consists from a Dickson charge pump, a 0.5-V voltage detector (VD_3) [5], and some switches. The concept of this scheme is to charge the node ϕ_1 without dynamic current and automatically pull ϕ_1 to 0 V by detecting $\mathrm{V_{CP}}$. The trigger voltage of VD_3 is designed to be 0.5 V to limit the pulse amplitude.

Fig. 14 shows the simulated waveforms of the proposed CPPG. Initially, $\mathrm{V_{CP}}$ is smaller than the trigger voltage of VD_3 and $\mathrm{V_G}$ $(\mathrm{V_D})$ is low. The charge pump charges the node $\mathrm{V_{CP}}$ and ϕ_1. During the charging cycle, the load current of the charge pump is limited and $\mathrm{V_{CP}}$ pumps up. When $\mathrm{V_{CP}}$ reaches the preset trigger voltage of VD_3 (0.5 V), $\mathrm{V_G}$ provides a pulse signal and pulls the node ϕ_1 to low. The delay cell is added to guarantee that the ϕ_1 is discharged to low while $\mathrm{V_{CP}}$ still remains high and the charging time of ϕ_1 is reduced. Comparing with the conventional approach, the proposed charge pumped pulse generator generates the pulse signal only when the output voltage of the charge pump achieves 0.5 V. Therefore, the power consumption can be reduced. The proposed CPPG provides a solution for generating a 0.5-V pulse signal with sub-1-nW power consumption in CMOS process.

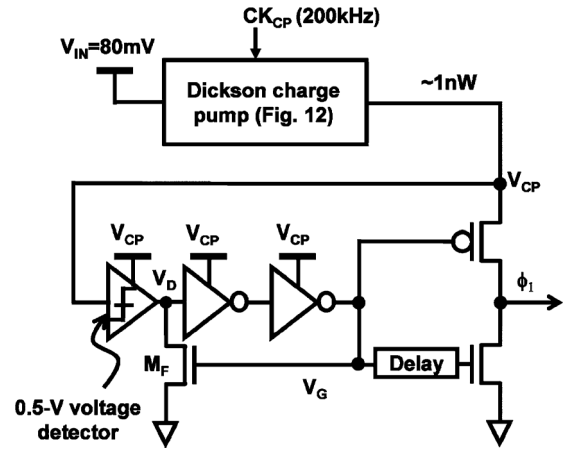

Fig. 13. Block diagram of the proposed sub-1 nW charge-pumped pulse generator (CPPG).

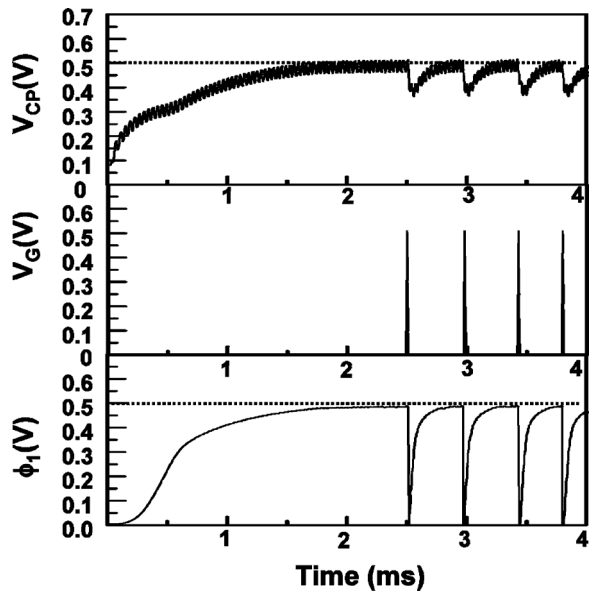

Fig. 14. Simulated waveform of the proposed charge-pumped pulse generator.

VI. Experimental Results

The test chip was fabricated using 65-nm standard CMOS technology. The microphotograph of the proposed dual-mode boost converter is shown in Fig. 15. The active area including the $\mathrm{V_{TH}}$-tuned oscillator with HCI, CPPG, the pulse generator and the boost converter is 0.25 mm^2. The circuit is measured with an off-chip inductor of 6.8 μH and an off-chip capacitor of 10 nF. The number of the off-chip components is same as the typical boost converter without startup mechanism and no additional off-chip devices are required.

Fig. 16 shows the measured dependence of $\mathrm{V_{DDMIN}}$ of the $\mathrm{V_{TH}}$-tuned oscillator with HCI on program time. To verify $\mathrm{V_{DDMIN}}$ improvement, three test dies were measured. As can be seen, $\mathrm{V_{DDMIN}}$ of the oscillator is reduced to 80 mV in 3 minutes and becomes as low as 70 mV in 10 minutes. The maximum $\mathrm{V_{DDMIN}}$ improvement is 45% in our measured chips. Comparing with AC stress in [5], the test time can be

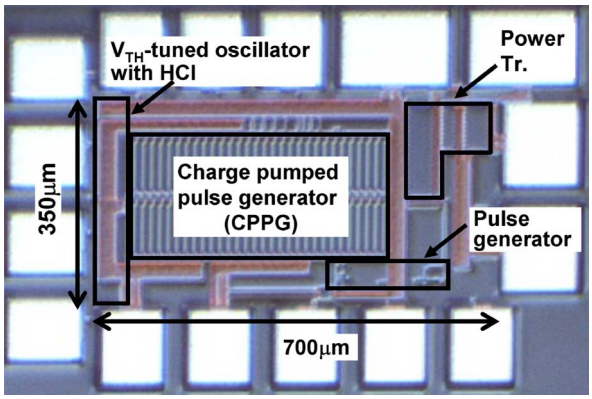

Fig. 15. Chip micrograph of dual-mode boost converter in 65-nm CMOS.

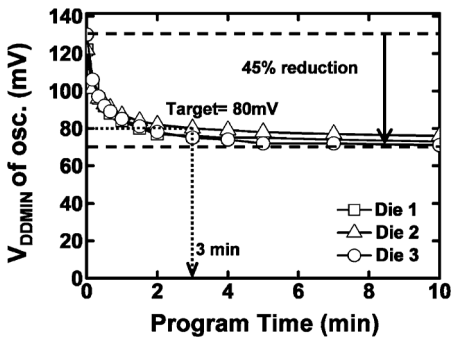

Fig. 16. Measured dependence of V_{DDMIN} of V_{TH}-tuned oscillator with HCI in Fig. 10 on program time for 3 dies.

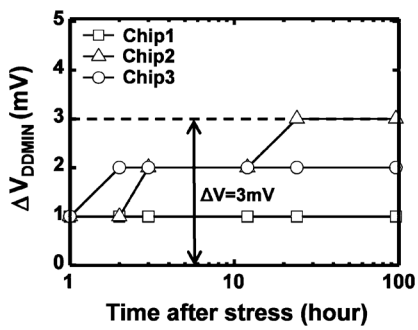

Fig. 17. Measured dependence of V_{DDMIN} change on time after program is finished.

reduced by 1/20. Therefore, the test cost can be significantly reduced.

Fig. 17 shows the measured dependences of V_{DDMIN} variation over the time after the program is finished. The circuit is operating under normal mode and the high reverse body bias is removed. V_{DDMIN} change is less than 3 mV after 100 hours of operating and gets stable.

Fig. 18 shows measured startup waveforms of the proposed dual-mode boost converter with CPPG under 80 mV V_{IN}. By applying dual-mode scheme with CPPG, V_C rises dramatically and reduces the startup time to 4.8 ms. The output voltage V_{OUT} is obtained after the boost converter is in operation mode. Fig. 19 shows the measured dependence of conversion efficiency on different load current. The proposed circuit achieves the maximum efficiency of 72% and 60% at 50 mV

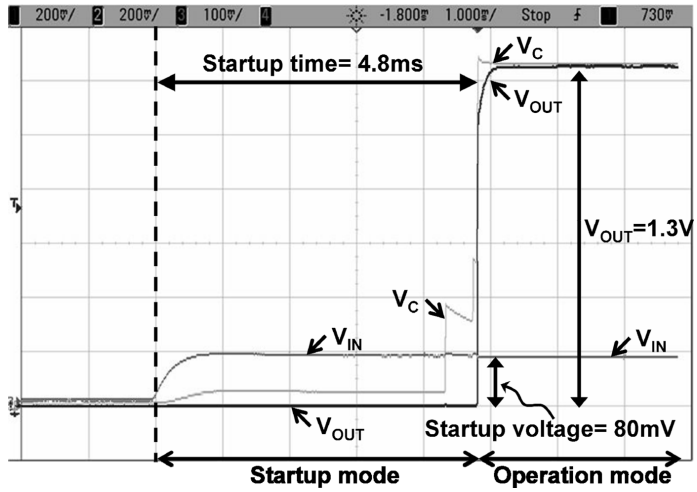

Fig. 18. Measured startup waveforms of proposed dual-mode boost converter.

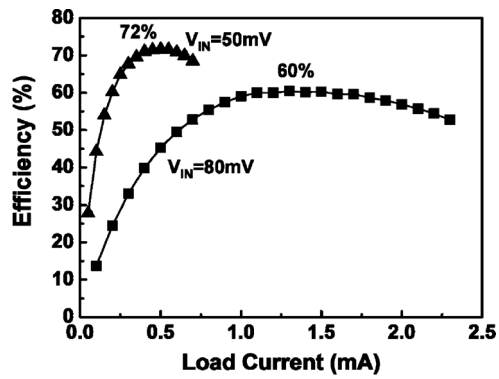

Fig. 19. Measured dependence of conversion efficiency on load current.

TABLE I
COMPARISON WITH PUBLISHED LOW-STARTUP VOLTAGE STEP-UP DC-DC CONVERTERS

Ref	Startup			Peak Efficiency	Program time for Osc.	CMOS process
	Mechanism	*Min. Voltage*	*Startup time*			
[9]	Boost converter with mechanical switch	35mV	18ms	58%@ V_{IN}=50mV	–	350nm
[5]	Charge pump	95mV	262ms	*72%@ V_{IN}=100mV	60min	65nm
[12]	Charge pump	180mV	N/A	N/A	–	65nm
[7]	External Voltage	650mV	N/A	75%@ V_{IN}=100mV	–	130nm
This work	Boost converter with CPPG	80mV	4.8ms	*72%@ V_{IN}=50mV	3min	65nm

* The output voltage is not regulated

and 80 mV V_{IN}, respectively. The conversion efficiency at 50 mV V_{IN} is higher because the power consumed by the driver circuits is smaller than that of 80 mV V_{IN}.

The performance comparison with the state-of-the-art step-up DC-DC converter with startup mechanism is shown in Table I. The proposed startup mechanism achieves 4.8 ms startup time and is shortest to date. Among the on-chip startup mechanisms, the lowest startup voltage of 80 mV is achieved. Although the

startup voltage of 35 mV is already implemented in [9], it requires a mechanical switch activated by vibration and is not an on-chip startup mechanism. The proposed V_{TH}-tuned oscillator by HCI (DC-stress) compensates for the die-to-die process variation reduces the program time to 3 minutes, which is 1/20 of the conventional AC-stress.

VII. Conclusion

A dual-mode boost converter with CPPG is developed in 65-nm CMOS for energy harvesting applications. CPPG generates a high-amplitude (0.5 V) high-duty clock signal with low power consumption (1 nW) to kick start the system. Therefore, an 80 mV startup voltage is achieved and is the lowest in on-chip startup mechanisms. A startup by the boost converter instead of a charge pump reduces the startup-time to 4.8 ms and is the shortest to date. We also proposed a V_{TH}-tuned oscillator with HCI to compensate for the die-to-die process variation. It achieves 45% of V_{DDMIN} reduction in the program time of 10 minutes. In addition, the program time can be 20 times shorter than the conventional AC stress, thereby reducing the test cost.

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