Large Within-Die Gate Delay Variations in Sub-Threshold Logic Circuits at Low Temperature

Ryo Takahashi, *Student Member, IEEE*, Hidehiro Takata, Tadashi Yasufuku, *Member, IEEE*, Hiroshi Fuketa, *Member, IEEE*, Makoto Takamiya, *Member, IEEE*, Masahiro Nomura, *Member, IEEE*, Hirofumi Shinohara, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—Temperature dependence of 256 within-die random gate delay variations in sub-threshold logic circuits is measured in 40-nm CMOS test chips. When the temperature is reduced from 25°C to −40°C, the sigma/average (σ/μ) of the gate delay at 0.3 V increases by 1.4 times. A newly developed model shows that σ/μ of the gate delay is proportional to $1/T$ for the first time, where T is the absolute temperature.**

***Index Terms*—Delay variations, device matrix array (DMA), sub-threshold, temperature.**

I. Introduction

SUB-THRESHOLD circuits, which operate at a lower supply voltage (V_{DD}) than threshold voltage (V_{TH}), are one of promising solutions to achieve ultra-low power operation [1]. When V_{DD} is reduced from the above-threshold region to the sub-threshold region, the gate delay variations (= sigma/average(= σ/μ)) due to the within-die random V_{TH} variation sharply increase [2], because the sub-threshold current has an exponential dependence on V_{TH}. In the sub-threshold logic circuits, the average (μ) and the variation (σ/μ) of the gate delay increase with decreasing temperature [3]. Therefore, the worst-case μ as well as the largest σ/μ is observed at low temperatures (e.g., −40 °C), a variability analysis at the worst-case temperature is required. Therefore, in this paper, the temperature dependence of 256 within-die random gate delay variations (σ/μ) in sub-threshold logic circuits is measured in 40-nm CMOS test chips and is explained with a newly developed model. It is found that σ/μ in sub-threshold logic circuits is proportional to $1/T$ for the first time, where T is the absolute temperature.

This paper is organized as follows. Section II describes silicon measurements of the within-die distribution of the oscillation periods of ring oscillators (ROs) and the calculation of random component of the gate delay variations. In order to investigate the dependence of the gate delay variation on temperature at low V_{DD}, a new model of the temperature dependence of the gate delay variations is proposed in Section III. Finally, Section IV concludes this paper.

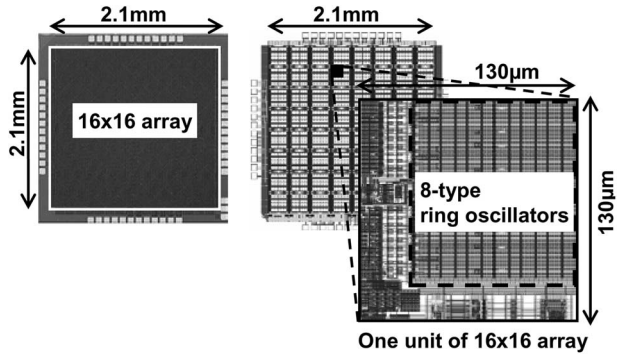

Fig. 1. Chip micrograph and layout of the device matrix array (DMA) test chip in 40-nm CMOS.

II. Measurement of Within-Die Random Gate Delay Variations

A. Test Chip Design

In order to measure the within-die random variation of the gate delay dependence on the supply voltage and the temperature efficiently, a device matrix array (DMA) test chip is designed and fabricated in 40-nm low-Vth (LVT) CMOS technology.

Fig. 1 shows the chip micrograph and layout. The device under testing is a 16 × 16 array with a 2.1-mm square. Each unit with a 130-μm square includes eight-type ROs.

Fig. 2 shows a schematic of the DMA. The oscillation periods of ROs are measured and the variability among 256 ROs is analyzed. The ROs are in the variable supply voltage region and the output of ROs are level-shifted to the nominal voltage (= 1.1 V). The measured eight-type ROs and measurement conditions are shown in Table I and Table II. The 11-stage ROs at 0.7 V and 1.1 V, and 31-stage ROs at 1.1 V, are not measured, since the oscillation frequencies are too fast to be measured in our measurement setup. Two-input NAND gate with ×2 drivability and two-input NOR gate with ×2 drivability are used. These ROs are designed so that the every gate has the same fan-out.

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R. Takahashi, T. Yasufuku, H. Fuketa, and T. Sakurai are with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan (e-mail: ryo-taka@iis.u-tokyo.ac.jp).

H. Takata, M. Nomura, and H. Shinohara are with Semiconductor Technology Academic Research Center (STARC), Yokohama 222-0033, Japan.

M. Takamiya is with the VLSI Design and Education Center (VDEC), University of Tokyo, Tokyo 153-8505, Japan.

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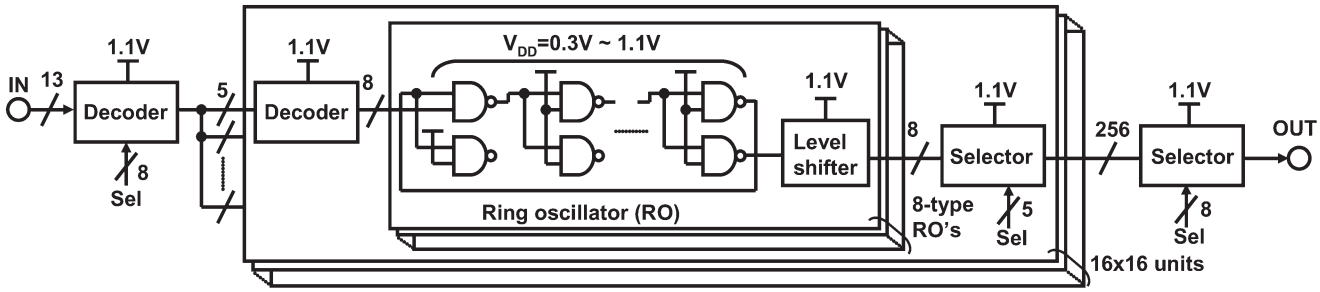

Fig. 2. Schematic of the DMA. The measurement circuit consists of $16 \times 16 \times 8 (= 2048)$ ROs.

TABLE I
TYPES OF RING OSCILLATORS UNDER TEST

NAND	11-stage	NOR	11-stage
	31-stage		31-stage
	85-stage		85-stage
	241-stage		241-stage

TABLE II
MEASUREMENT CONDITIONS

Supply voltage [V]	0.3 / 0.5 / 0.7 / 1.1
Temperature [ºC]	-40 / -20 / 0 / 25 / 50 / 85

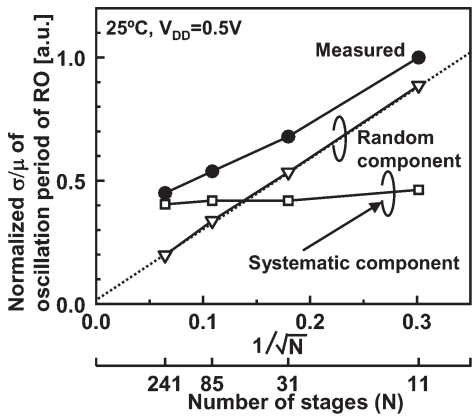

Fig. 3. Measured dependence of the normalized σ/μ of oscillation period on number of stages (N) of RO at $V_{DD} = 0.5$ V and 25 °C. Random component of variation of NAND RO cycle time is inversely proportional to the square of number of stages.

B. Measurement Results

Fig. 3 shows the measured dependence of the normalized σ/μ of the oscillation period on the number of stages (N) at $V_{DD} = 0.5$ V and 25 °C. σ/μ is normalized to the 11-stage RO. In order to separate the random variability component and the systematic variability component from the measured raw data, the fourth-order polynominal fitting proposed in [4] is used in this paper. The extracted random component is inversely proportional to the square root of N, which confirms the validity of the separation.

Figs. 4 and 5 show the measured temperature dependence of normalized mean (μ) and variation (σ/μ) of NAND and NOR gate delay with different V_{DD}, respectively. In Figs. 4 and 5, μ and σ/μ are normalized to the NAND gate at 1.1 V and 25 °C. In Fig. 4, the worst-case $(=$ largest$)$ μ is observed at 0.3 V and -40 °C, where the normalized μ is more than 10^4. In Fig. 5, the worst-case $(=$ largest$)$ σ/μ is also observed at

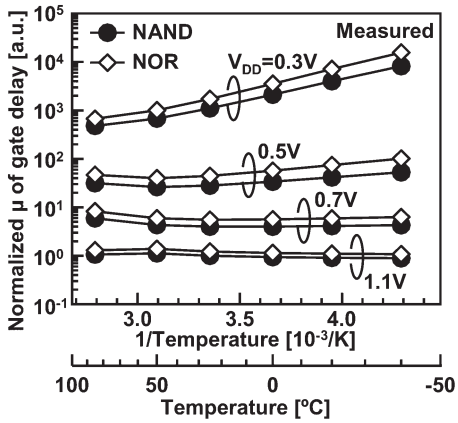

Fig. 4. Measured temperature dependence of normalized mean (μ) of NAND and NOR gate delay in 85-stage ROs with different V_{DD}.

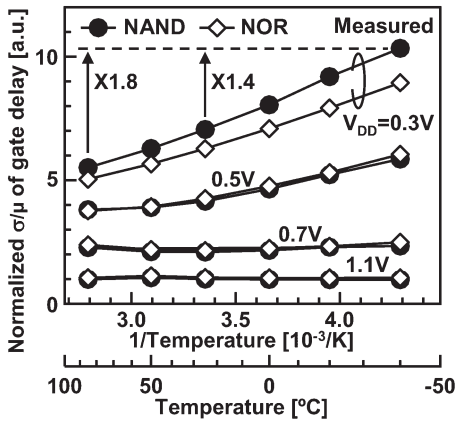

Fig. 5. Measured temperature dependence of normalized variation (σ/μ) of NAND and NOR gate delay in 85-stage ROs with different V_{DD}.

0.3 V and -40 °C, where the normalized σ/μ is more than 10. In the NAND gate at 0.3 V, σ/μ at -40 °C is 1.4 times of that at 25 °C, and 1.8 times of that at 85 °C. The temperature dependence of σ/μ in the sub-threshold logic circuits is not negligible. Therefore, the temperature dependence of σ/μ is modeled in the next section.

III. MODELING OF TEMPERATURE DEPENDENCE OF GATE DELAY VARIATIONS

A. Temperature Dependence of Gate Delay Variations in the Above-Threshold Region

In this section, σ/μ of the gate delay in the above-threshold region is modeled. In the above-threshold region, on current

(I_{ON}) is modeled by the alpha-power law MOSFET model [5] as

$$I_{ON} = I_O(V_{DD} - V_{TH})^{\alpha} \tag{1}$$

where α is the velocity saturation index and I_O is a technology-dependent parameter. Let t_{pd} be a gate delay and it is given by

$$t_{pd} = b\frac{CV_{DD}}{I_{ON}} = \frac{bCV_{DD}}{I_O(V_{DD} - V_{TH})^{\alpha}} \tag{2}$$

where b is a proportional constant and C is the load capacitance. The gate delay variation (Δt_{pd}) induced by the V_{TH} variation (ΔV_{TH}) can be expressed by the first-order approximation as

$$\begin{aligned}\Delta t_{pd} &= \frac{dt_{pd}}{dV_{TH}}\Delta V_{TH} = \frac{b\alpha CV_{DD}}{I_O(V_{DD} - V_{TH})^{\alpha+1}}\Delta V_{TH} \\ &= t_{pd}\frac{\alpha}{V_{DD} - V_{TH}}\Delta V_{TH}.\end{aligned} \tag{3}$$

When ΔV_{TH} is σ_{VTH}, which is defined as the standard deviation of the within-die V_{TH} variation, Δt_{pd} corresponds to the standard deviation of the gate delay variation (σ). Therefore, σ/μ of the gate delay due to the within-die random V_{TH} variation is derived from (3) as

$$\frac{\sigma}{\mu} = \frac{\Delta t_{pd}}{t_{pd}} = \frac{\alpha}{V_{DD} - V_{TH}}\Delta V_{TH} = \frac{\alpha}{V_{DD} - V_{TH}}\sigma_{VTH}. \tag{4}$$

In this paper, we assume that α and σ_{VTH} do not depend on temperature for simplicity, since the dependence of σ_{VTH} on temperature is small, as reported in [6]. The dependence of σ/μ of the gate delay on temperature is derived as

$$\frac{d\left(\frac{\sigma}{\mu}\right)}{dT} = \frac{\alpha\kappa\sigma_{VTH}}{(V_{DD} - V_{TH})^2} \tag{5}$$

where κ is the temperature coefficient for V_{TH} and given by

$$V_{TH}(T) = V_{TH}(T_0) - \kappa(T - T_0) \tag{6}$$

where $V_{TH}(T)$ is V_{TH} at the temperature of T and T_0 is the nominal temperature. At the nominal supply voltage of 1.1 V, $(V_{DD} - V_{TH})^2$ is much larger than $\alpha\kappa\sigma_{VTH}$ and, hence, the dependence of σ/μ of the gate delay on temperature is significantly small, as shown in Fig. 5.

B. Temperature Dependence of Gate Delay Variations in the Sub-Threshold Region

In this section, σ/μ of the gate delay in the sub-threshold region is modeled. In the sub-threshold region, I_{ON} is expressed as

$$I_{\mathrm{ON}} = I_O \exp\left(\frac{q}{nkT}(V_{DD} - V_{TH})\right)\cdot\left(1 - \exp\left(-\frac{qV_{DD}}{kT}\right)\right) \tag{7}$$

where n is the sub-threshold swing parameter, k is the Boltzmann constant, q is the elementary charge, T is the absolute temperature, and I_0 is a technology-dependent parameter [7]. When V_{DD} is more than 0.1 V, I_{ON} is approximated to

$$I_{ON} \cong I_O \exp\left(\frac{q}{nkT}(V_{DD} - V_{TH})\right). \tag{8}$$

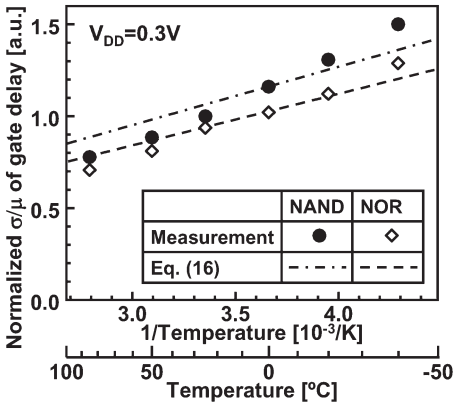

Fig. 6. Measured and calculated temperature dependence of normalized variation (σ/μ) of NAND and NOR gate delay in 85-stage ROs at 0.3 V.

Here, X_{VTH} is introduced to express the within-die random V_{TH} variation as

$$V_{TH} = V_{TH0} + X_{VTH}, \tag{9}$$

$$X_{VTH} \sim N\left(0, \sigma_{VTH}^2\right) \tag{10}$$

where σ_{VTH} is the standard deviation of the within-die random V_{TH} variation and V_{TH0} is the mean of the V_{TH} variation.

A gate delay (t_{pd}) in the sub-threshold region is derived as

$$t_{pd} = d\frac{CV_{DD}}{I_{ON}} = A\exp\left(\frac{q}{nkT}X_{VTH}\right) \tag{11}$$

where d is a proportional constant and

$$A = \frac{dCV_{DD}}{I_O\exp\left(\frac{q}{nkT}(V_{DD} - V_{TH0})\right)}. \tag{12}$$

Equation (11) indicates that the variation of the gate delay in the sub-threshold region follows log-normal distribution. Therefore, the mean and the variance of the gate delay variation are given by

$$\mu = A\exp\left(\frac{\left(\frac{q\sigma_{VTH}}{nkT}\right)^2}{2}\right), \tag{13}$$

$$\sigma^2 = A^2\exp\left(\left(\frac{q\sigma_{VTH}}{nkT}\right)^2\right)\left\{\exp\left(\left(\frac{q\sigma_{VTH}}{nkT}\right)^2\right) - 1\right\}. \tag{14}$$

Consequently, σ/μ of the gate delay is derived as

$$\frac{\sigma}{\mu} = \sqrt{\exp\left(\left(\frac{q\sigma_{VTH}}{nkT}\right)^2\right) - 1}. \tag{15}$$

When $(q\sigma_{VTH}/nkT)^2 \ll 1$, (15) can be approximated to

$$\frac{\sigma}{\mu} \cong \sqrt{\left\{1 + \left(\frac{q\sigma_{VTH}}{nkT}\right)^2\right\} - 1} = \frac{q\sigma_{VTH}}{nkT}. \tag{16}$$

Since the dependence of σ_{VTH} on temperature is small [6], (16) shows that σ/μ in the sub-threshold region is proportional to $1/T$, which is clarified for the first time. Equation (16) is compared with the measured results in Fig. 6. It should be noted that σ_{VTH} in (16) is estimated by the least squares method. Fig. 6 shows the measured and calculated temperature

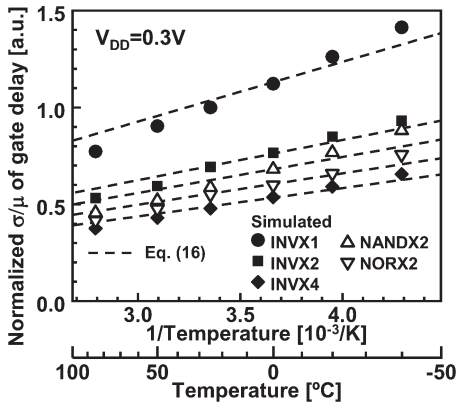

Fig. 7. SPICE simulated and calculated temperature dependence of normalized variation (σ/μ) of five-type gate delay in 11-stage ROs with different V_{DD}.

dependence of normalized σ/μ of NAND and NOR gate delay at 0.3 V. σ/μ is normalized to the NAND gate at 25 °C. Equation (16) is a good approximation to the measured temperature dependence of the gate delay variations, since the relative errors between the measured and calculated results are less than 11%.

In Fig. 6, only NAND and NOR gates are shown. In order to investigate the temperature dependence in various gates, five-type gates are simulated with SPICE and compared with the calculated results by (16). Fig. 7 shows the SPICE simulated and calculated temperature dependence of normalized σ/μ of the five-type gates at 0.3 V. Three-type inverters with $\times 1$ drivability, $\times 2$ drivability, and $\times 4$ drivability are added. σ/μ is normalized to the inverter with $\times 1$ drivability at 25 °C. The simulated results are obtained by 3000 times Monte-Carlo SPICE. Fig. 7 indicates that (16) is a good approximation to the simulated temperature dependence of the gate delay variations, since the relative errors between the simulated and calculated results are less than 12%. As the inverter drivability is reduced, σ/μ increases, because the random V_{TH} variations increase with reducing transistor size.

IV. Conclusion

In this paper, the temperature dependence of the within-die random gate delay variations in sub-threshold logic circuits is measured in 40-nm CMOS test chips. When the temperature is reduced from 25 °C to −40 °C, the sigma/average (σ/μ) of the gate delay at 0.3 V increases by 1.4 times. A newly developed model shows that variation (σ/μ) of the gate delay is proportional to $1/T$ for the first time, where T is the absolute temperature. Therefore, the large delay variations at low temperatures should be considered in the worst-case design of the sub-threshold logic circuits.

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