A 100-V AC Energy Meter Integrating 20-V Organic CMOS Digital and Analog Circuits With a Floating Gate for Process Variation Compensation and a 100-V Organic pMOS Rectifier

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***Abstract*—A 100-V ac energy meter based on the system-on-a-film (SoF) concept, in which various devices are integrated on a flexible film, is presented. The system consists of 20-V organic CMOS digital and analog circuits with a floating gate (FG) for process variation compensation, 100-V organic pMOS rectifiers for generating a 50-Hz clock and 20-V dc power, and an organic LED (OLED) bar indicator. The energy meter based on the SoF is flexible and therefore can be installed to monitor each ac outlet simultaneously. The organic devices are printable, and it is expected that they can be formed using a low-cost printing process in the future. The energy meter can measure the accumulated energy of a 100-V_{rms} ac lineup to a full-scale value of 360 Wh when a 500-W target load is monitored. The flexible film is foldable and its total area excluding the ac connector is 200 × 200 mm^2 in the unfolded form or 70 × 70 mm^2 when folded.**

***Index Terms*—Floating gate (FG), large-area electronics, mismatch compensation, operational amplifier, organic CMOS, organic LED, pseudo-CMOS, system-on-a-film (SoF).**

I. Introduction

A SMART meter is essential for realizing a smart grid. To further reduce the energy loss in the power grid, instead of simply replacing conventional energy meters with smart meters, an extremely fine-grain power-monitoring system (e.g., power monitoring of every electric outlet or battery) is desirable [1]. This will require an enormous number of low-cost energy meters. Existing energy meters, however, do not meet the requirements for this application in terms of their cost and form factor.

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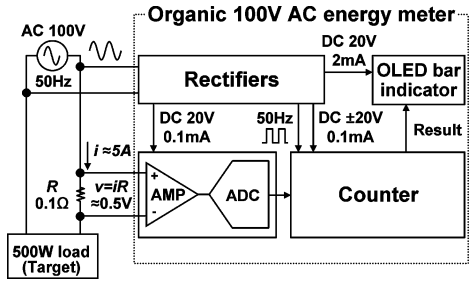


Fig. 1. Overview of the organic 100-V ac energy meter.

On the other hand, printable organic devices on flexible films have great potential to realize low-cost energy meters and a flexible energy meter can be installed to monitor each ac outlet simultaneously. In this context, a 100-V ac energy meter based on the system-on-a-film (SoF) concept was proposed, and its feasibility was demonstrated [2].

In this paper, we describe the 100-V ac energy meter in detail and provide detailed measurement results and some discussion. In Section II, we give an overview of the proposed energy meter and the SoF concept. In Section III, we describe the circuit design in detail. In Section IV, we present and discuss the experimental results. Finally, conclusions are given in Section V.

II. Overview of 100-V AC Energy Meter

Fig. 1 shows an overview of the 100-V ac energy meter, which consists of four circuit blocks. For instance, a 3-W, 0.1-Ω resistor that can handle a current of up to 5.48 A_{rms} is used as a current-sensing resistor (R). This component is suitable for the measurement of the 100-V_{rms}, 500-W target load. An ac current (i) of about 5 A_{rms} flows into the ac power line circuit loop. The voltage (v) across the sensing resistor is amplified and the power level is converted into a number of digital pulses per unit of time. The counter accumulates the digital pulses and the resulting measured energy is displayed by an organic LED (OLED) bar indicator. We use the OLED indicator since this energy meter is designed for domestic uses. When the energy meter is used for large buildings, offices, and industry, either a wired or wireless communication circuitry should be added to monitor the measured data in real time. The organic rectifiers supply both dc power with a maximum current of more than

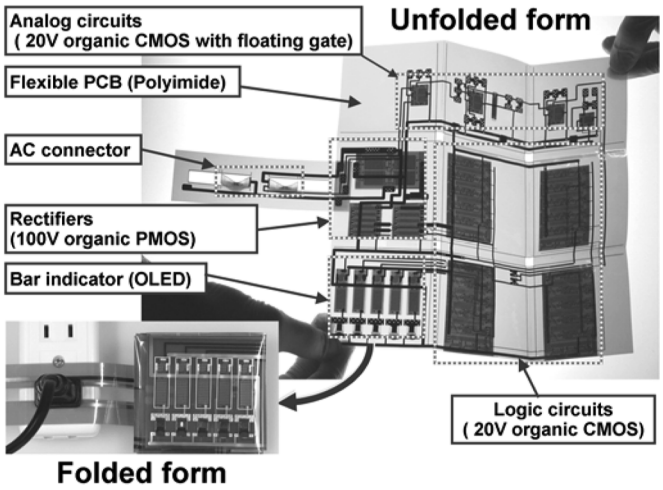


Fig. 2. Prototype of the organic 100-V ac energy meter on a flexible film.

2 mA and 50-Hz clock pulses to the circuit blocks in the energy meter.

To handle both a small signal of approximately 0.5 V and a high voltage of 100 V_{rms} ac at the same time, various organic devices have been used to meet diverse design requirements. Fig. 2 shows a photograph of the proposed organic 100-V ac energy meter on a flexible film. The key components of the energy meter include: 1) a rectifier composed of a 100-V organic pMOS for generating the 20 V DC power and clock pulses for the energy meter; 2) analog circuits composed of 20-V organic CMOS transistors with a floating gate (FG) like the operational amplifier for sensing the ac current; 3) logic circuits composed of 20-V organic CMOS transistors for the frequency divider and the counter accumulating the measured power; 4) an OLED [3] bar indicator for displaying the measured energy; and 5) an ac connector inserted between the power plug and the ac outlet and discrete passive components (capacitors and resistors for circuit tuning) which are fully integrated on a 200×200 mm^2 flexible film. We name this type of system implementation an SoF. The energy meter based on the SoF is flexible and therefore can be installed to monitor each ac outlet simultaneously. The organic devices are printable and will be manufactured using low-cost printing process in the future. The entire sheet of the film can be folded and the total size of the proposed 100-V ac energy meter can be reduced to 70×70 mm^2. In this work, the system dimensions are mainly determined by the manufacturable sizes of the printable organic transistors. The system dimensions can be further reduced by design-rule scaling of the printable organic transistors.

III. Circuit Design

A. System Block Diagram and Target Specifications

Fig. 3(a) shows a block diagram of the 100-V ac energy meter, which consists of four blocks. Rectifiers implemented with 100-V organic pMOS transistors include a full-wave rectifier for the dc power supplies and a half-wave rectifier for clock generation. The required dc supplies for the energy meter ($V_{DD} = 20$ V, GND $= 0$ V, $V_{SS} = -20$ V) are provided by

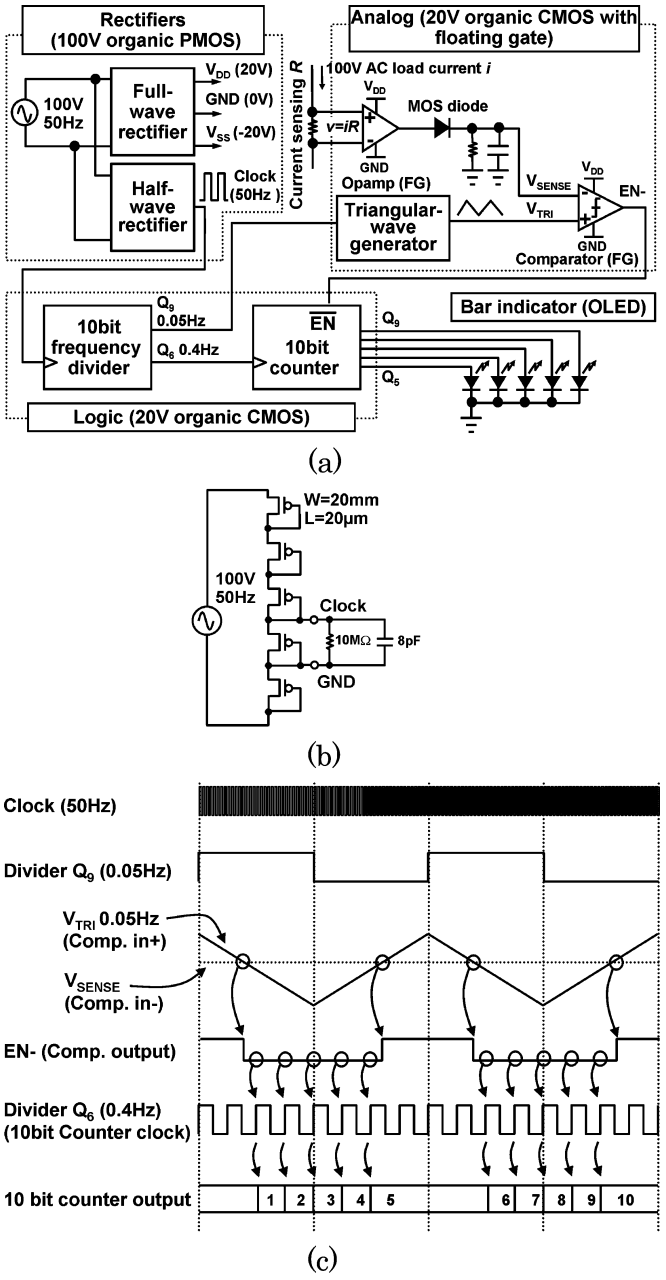


Fig. 3. Overview of the organic 100-V ac energy meter. (a) Block diagram of the ac energy meter. (b) Schematic of the half-wave rectifier used for clock generation. (c) Timing chart.

converting the 100-V_{rms} 50-Hz ac power to 20-V dc power using the full-wave rectifier. The 50-Hz clock pulses used for the input of the 10 bit frequency divider are directly generated from the 100-V_{rms} 50-Hz ac signal by a half-wave rectifier, which consists of five diode-connected pMOS transistors as shown in Fig. 3(b).

In this implementation, we do not use dc-to-dc converters or voltage regulators, which require a voltage reference, to simplify the circuitry. V_{SS} is generated by a voltage divider, which consists of diode-connected pMOS transistors. Therefore, both V_{DD} and V_{SS} are determined by the load current. To improve the regulation of the output voltage, voltage regulators for the power supplies should be added in a practical design.

Analog circuits implemented with a 20-V organic CMOS with an FG include an operational amplifier, a MOS diode, a voltage comparator, and a triangular-wave generator. The ac load current i is converted to a voltage of up to ac 0.5 $\mathrm{V_{rms}}$ by the sensing resistor R. To amplify the 0.5-$\mathrm{V_{rms}}$ input voltage, the input mismatch of the amplifier should be suppressed to well below 0.5 V. The operational amplifier employs a mismatch compensation scheme that exploits the transistor FG [4]. This scheme requires three times higher V_{DD} voltage than the normal supply voltage to inject charges into the FG. If we used an FG for 100-V devices, 300 V or more would be required for FG operation, which is too high to be handled safely. Therefore, we use a 20 V CMOS process for the analog circuits. This 20-V CMOS operational amplifier is used in linear gain region without feedback loop because of its small open-loop gain. The MOS diode converts the ac voltage at the output of the operational amplifier into the dc voltage V_{SENSE} as shown in Fig. 3(a). Then, V_{SENSE} is compared with a 0.05-Hz triangular-wave V_{TRI} by a comparator. The operational amplifier with the FG as shown in Fig. 3(c) is used for this comparator and its output is amplified by a pseudo-CMOS inverter [9]. The triangular-wave generator is driven by Q_9 of the frequency divider. The output of the comparator is connected to the enable pin of the 10-b counter operating at 0.4 Hz (Q_6 of the frequency divider), which is eight times higher than the frequency of the triangular-wave. The output of the comparator, which depends on the input signal polarity, enables or disables the 10 bit counter. Since the triangular-wave is symmetric, the dc voltage is evaluated with four $(= 8/2)$ voltage steps (equivalent to 2-b resolution).

The logic circuits implemented with a 20-V organic CMOS consist of a 10-b frequency divider and a 10-b counter. The 0.05-Hz clock for the input of the triangular-waveform generator and the 0.4-Hz clock for the 10-b counter are both generated by the 10-b frequency divider. To measure the accumulated energy instead of obtaining instantaneous readings, the maximum integration time of the energy meter is designed to be 43 min $(= 2^{10}/0.4\ \mathrm{Hz}/60\ \mathrm{s})$, which is equivalent to 360 Wh with a 500-W load.

The five most significant bits in the 10-b counter are connected to the 5-b OLED bar indicator used for displaying the measured results. By observing the OLED bar indicator, the user can visualize the amount of electric power that he/she is using. The minimum energy indicated by the OLED bar indicator is 11 Wh $(= 360\ \mathrm{Wh}/2^{\circ}5\ \mathrm{bit})$.

In this implementation, the OLED indicator displays raw binary data to simplify the circuitry, that is, the OLED indicator will be reset if the counter reaches 360 Wh. To avoid this inconvenience, the number of counter bits should be increased and the maximum value should be stored in a practical design.

B. All-PMOS Full-Wave Rectifier

To supply dc power to the energy meter from a 100-$\mathrm{V_{rms}}$ ac power source, we implemented a full-wave rectifier using a 100-V organic pMOS based on the semiconductor pentacene. Since in our technology the driving capability of an organic nMOS is weaker than that of a pMOS by approximately an order of magnitude, it is not practical to use an nMOS in the rectifier. The total current consumption of our logic circuit is tens of ìA, while our OLED-based bar indicator requires a total current of 2 mA for all five OLED modules; thus, we use an all-PMOS full-wave rectifier. For a typical rectifier using pMOS diode-connected transistors as shown in Fig. 4(a), the power efficiency is poor since each pMOS transistor operates at the pinch-off region. To increase the output current of the rectifier, two pMOS diodes are replaced with a pair of cross-coupled pMOS transistors operating in the linear region as shown in Fig. 4(b). V_{GS} for the cross-coupled pMOS transistors is equal to V_{DD} (up to 100 V). These cross-coupled transistors are strongly on, and V_{DS} for the diode-connected transistors in the proposed rectifier is higher than that in the conventional solution as shown in Fig. 4(c). Therefore, the output current can be larger than that of conventional pMOS diode-connected transistors. Both the conventional and proposed rectifiers have been implemented using pMOS transistors with a gate length and width of 20 μm and 100 mm, respectively and the measurements results will be shown in Section IV. These transistors can supply up to 2-W dc power as shown in Fig. 5, which is the highest power level ever reported.

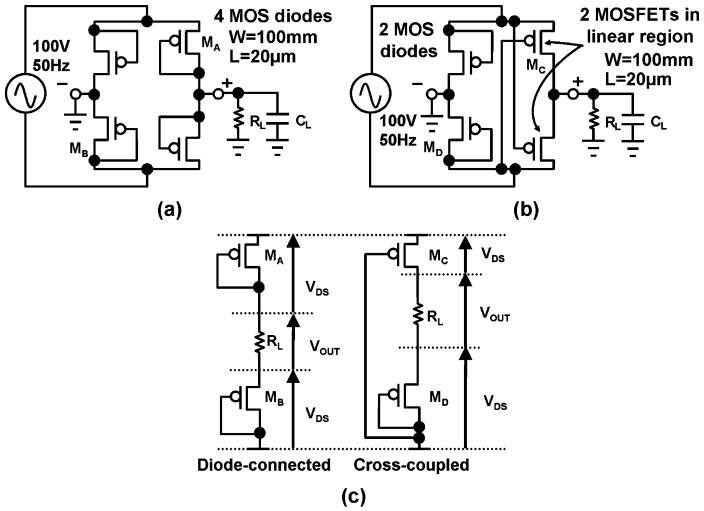


Fig. 4. The 100-V organic all-PMOS rectifier. (a) Conventional pMOS diode rectifier. (b) Proposed cross-coupled pMOS rectifier. (c) Comparison of the operation.

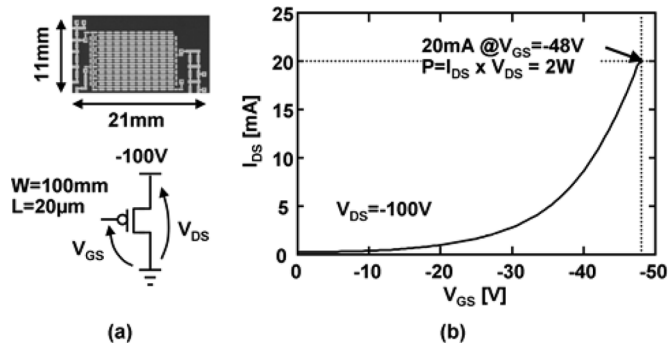


Fig. 5. The 100-V organic pMOS transistor. (a) Photograph. (b) Measured I_{DS}–V_{GS} characteristic.

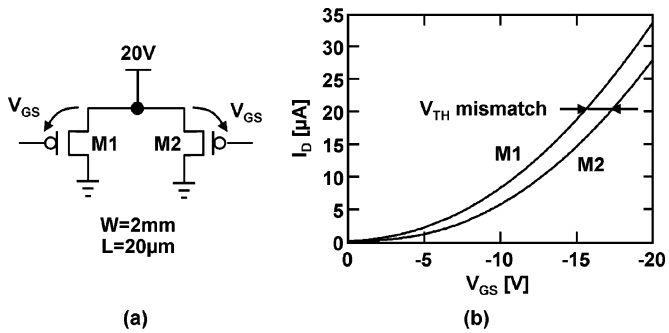


Fig. 6. Measured $V_{\rm TH}$ mismatch for a differential pair in 20-V CMOS process. (a) Schematic. (b) Measured I_D–$V_{\rm GS}$ characteristics.

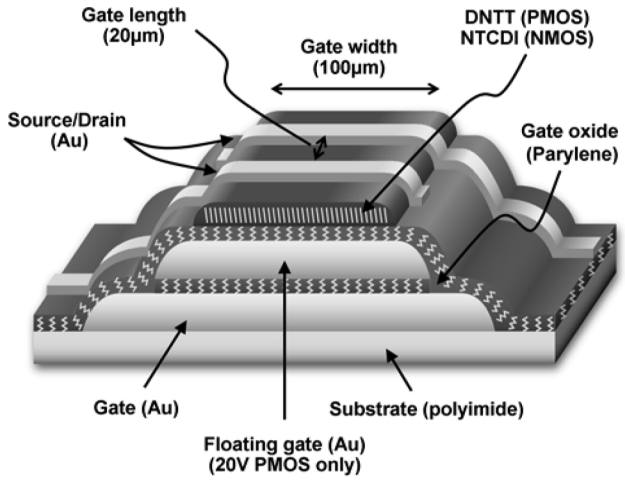


Fig. 7. Device structure of 20-V organic CMOS transistor.

C. 20-V CMOS Organic Operational Amplifier With an FG for Compensation

A major challenge in organic circuit design is to compensate for the large process variations of organic devices. The offset voltage in the differential pair of the operational amplifier due to the device mismatch of organic devices can be much larger than the sensing voltage generated by the sensing resistor R in Fig. 3. As discussed above, the maximum voltage expected on the sensing resistor is 0.5 V. On the other hand, the measured standard deviation of $V_{\rm TH}$ is 1.78 V at an I_D of 1 $\times 10^{-7}$ A in our 20-V organic CMOS process. Fig. 6 shows the worst-case scenario of the $V_{\rm TH}$ mismatch for a differential pair in this work.

Various techniques for compensating for variation such as back gate biasing [5], [6] have been reported. However, the back gate voltage of each organic device needs to be continuously supplied throughout the operation time. To tackle this design challenge, we employ FG pMOS technology [4] for the input stage of the operational amplifier to compensate for process variations.

The device structure of the 20-V organic CMOS transistor with an FG is shown in Fig. 7. Polyimide is used for the substrate. Gold is used for both the gate and the FG, and is deposited on the substrate. The gate oxide material is parylene and the total gate oxide thickness is 480 nm (= 240 nm + 240 nm). The organic semiconductor materials used for the pMOS and nMOS are DNTT [7] and NTCDI [8], respectively.

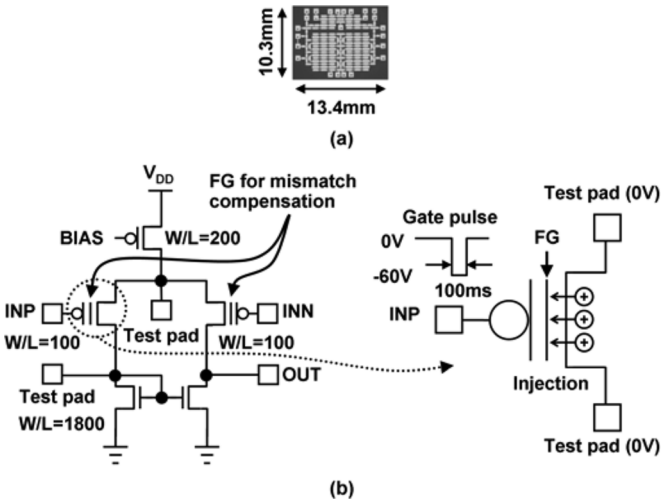


Fig. 8. The 20-V organic CMOS operational amplifier with FG for variation compensation. (a) Photograph. (b) Schematics.

Fig. 8(a) shows a photograph of the 20-V organic CMOS operational amplifier with an FG to compensate for variation. Fig. 8(b) shows schematics of the operational amplifier and the corresponding compensation scheme. The input differential pair of the operational amplifier is composed of two pMOS transistors (M1, M2) with an FG and five IO pads are added to compensate the mismatch.

Both the source and drain are fixed to 0 V during compensation. By applying −60-V, 100-ms-wide pulses to the gate terminal as shown in Fig. 8(b), positive charges are injected into the FG, which increases the absolute value of $V_{\rm TH}$ of the pMOS with an FG to compensate for variation. The key advantages, compared with supplying back-gate voltages, include: 1) the variation can be compensated for using a single high-voltage source with a fixed voltage (e.g., −60 V in our case); 2) controllability can be achieved by varying the voltage pulsewidth (e.g., 100 ms) and the number of pulses; and 3) once the variation has been compensated for, no external dc voltage sources are required throughout the operation time.

D. 20-V Pseudo-CMOS-Based 10-b Frequency Divider

A major design challenge in large-scale organic logic circuits is to ensure a satisfactory noise margin. In our 20-V CMOS technology, a DNTT-based pMOS has eight times higher carrier mobility (= 0.7 $\rm cm^2/Vs$) than an NTCDI-based nMOS (= 0.09 $\rm cm^2/Vs$) [7], [8]. As a result, the measured CMOS inverter gain was only 3.2 at 20 V, as shown in Fig. 9(a). The low gain may lead to retention errors in the latches used in large-scale organic logic circuits.

To solve this problem, we designed a frequency divider based on high-gain pseudo-CMOS inverters [9] instead of CMOS inverters, as shown in Fig. 10. In the divider, nMOS transistors are only used in CMOS transmission gates, where no gain is required. The pseudo-CMOS inverter uses only pMOS devices as shown in Fig. 9(b). A very high measured inverter gain of 148 and a static noise margin of 6.7 V, as well as a 156-Hz oscillation frequency for a three-stage ring oscillator, can be achieved simultaneously at a 20-V supply voltage, as shown in Fig. 11.

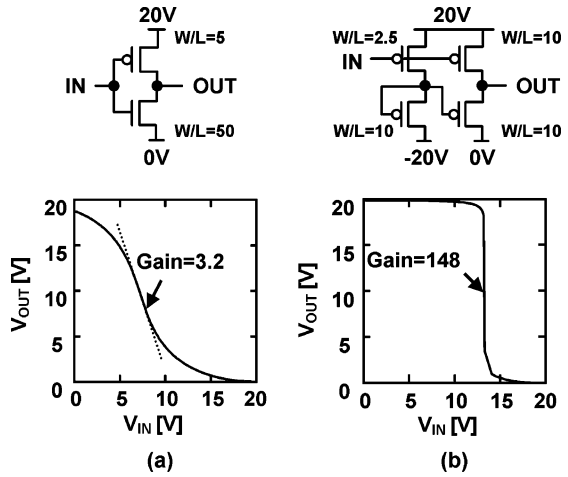


Fig. 9. Comparison of schematics and measured inverter gains. (a) CMOS inverter. (b) Pseudo-CMOS inverter.

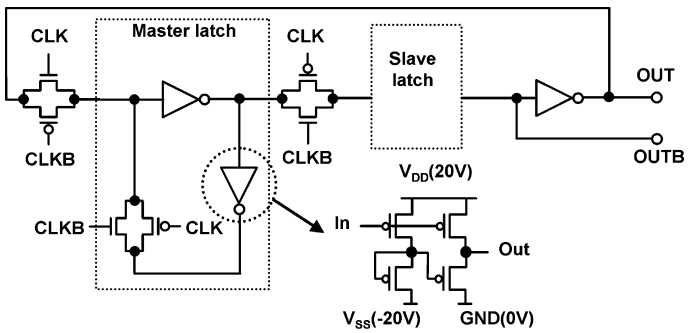


Fig. 10. Schematic of the proposed pseudo-CMOS-based frequency divider.

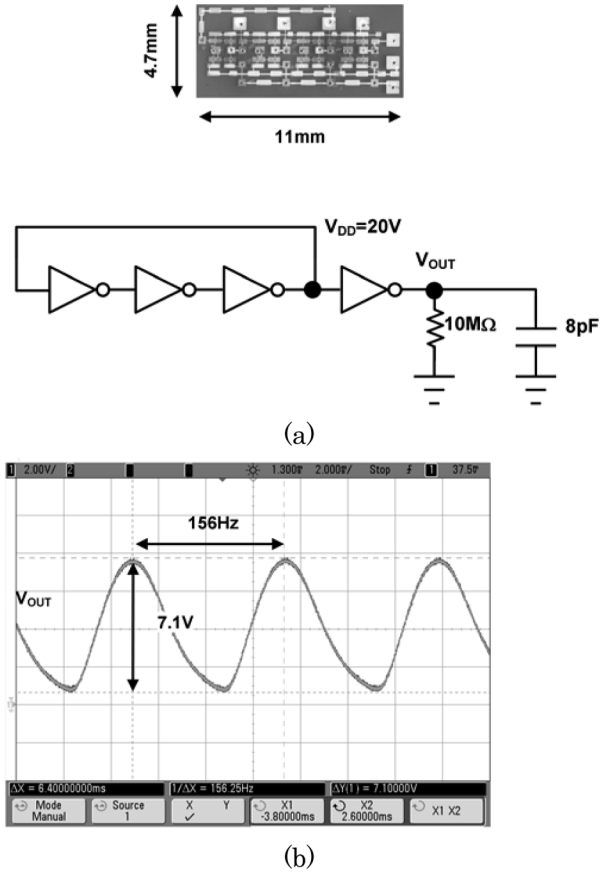


Fig. 11. Three-stage ring oscillator with pseudo-CMOS inverter. (a) Photograph and schematic. (b) Measured waveform.

IV. Measurement Results and Discussion

A. All-PMOS Full-Wave Rectifier

Both the conventional pMOS diode-connected rectifier and the rectifier using a cross-coupled pMOS were measured. The measured circuits are shown in Fig. 4. A comparison of the measurement results for these two rectifiers is shown in Fig. 12. The pMOS diode rectifier supplies a 2.1-mA output current at 20 V, which is not sufficient for the target specification indicated in Fig. 12. On the other hand, the cross-coupled pMOS rectifier increases the output current by 24% to provide an output current of 2.7 mA at an output voltage of 21.9 V, which is sufficient for our system.

Fig. 13(a) shows the measured waveform of the output voltage of 21.9 V obtained using the cross-coupled pMOS rectifier with an output-smoothing capacitance of 100 μF. The output ripple is less than 0.16 V (0.73% of the output voltage) at the target load current of 2.7 mA. Fig. 13(b) shows the measured waveform of the rectifier without the output-smoothing capacitance. Although amplitude fluctuations due to device variations are observed, the waveform demonstrates full-wave rectification of the 100-$V_{\rm rms}$ 50-Hz ac power supply.

B. 20-V CMOS Organic Operational Amplifier With an FG for Compensation

Fig. 14 shows the effect of the compensation of mismatch by charge injection to the FG on the measured $I_D - V_{\rm GS}$ characteristics of M1 and M2. The measurement and the compensation of M1 are performed 10 times. The initial $V_{\rm TH}$ mismatch was 1.5 to 2.0 V, which is unacceptable for amplifying a sensing voltage of below 0.5 V. Therefore, some kind of compensation of variation is required. $V_{\rm TH}$ for M1 can be monotonically moved towards that for M2 by increasing the number of gate pulses as shown in Fig. 14(b). As a result, the $V_{\rm OUT} - V_{\rm IN}$ characteristics of the operational amplifier can be modified as shown in Fig. 15. By

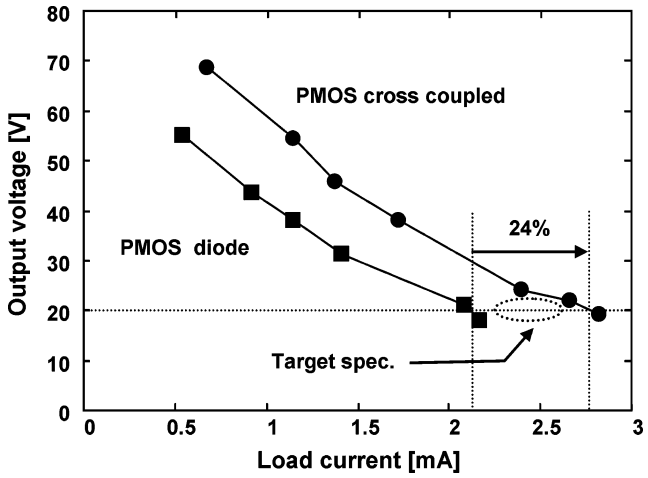


Fig. 12. Measured output voltage versus load current of conventional pMOS diode rectifier and proposed cross-coupled pMOS rectifier in Fig. 4.

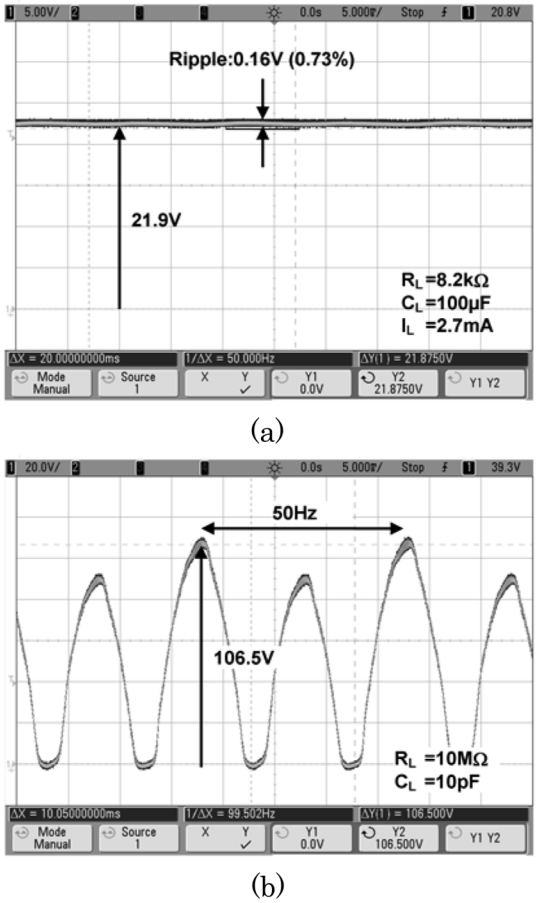


Fig. 13. Measured waveform of the cross coupled pMOS full-wave rectifier. (a) With output-smoothing capacitance of 100 μF. (b) Without output-smoothing capacitance.

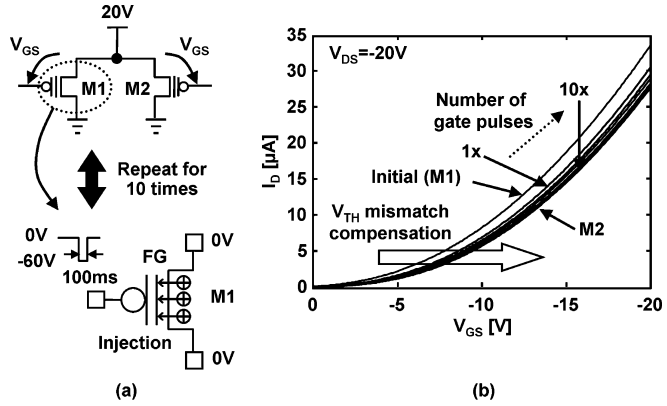


Fig. 14. Measured mismatch compensation of a pair of transistors. (a) Schematic. (b) Measured result.

increasing the number of gate pulses, the characteristic monotonically shifts to the left until the offset is sufficiently small.

Fig. 16 shows the dependence of the differential voltage gain at $V_{\rm INP} = V_{\rm INN} = 15$ V on the number of pluses derived from Fig. 15(b). The initial gain of 2.7 (8.6 dB) can be increased to 4.9 (13.8 dB) by applying two pulses ($= 200$ ms). Fig. 17 shows the dependence of $V_{\rm OUT}$ at $V_{\rm INP} = V_{\rm INN} = 15$ V on the number of pulses. $V_{\rm OUT}$ is also shifted from 8.4 to 12.5 V by applying two pulses. In this way, the gain of the operational amplifier can be

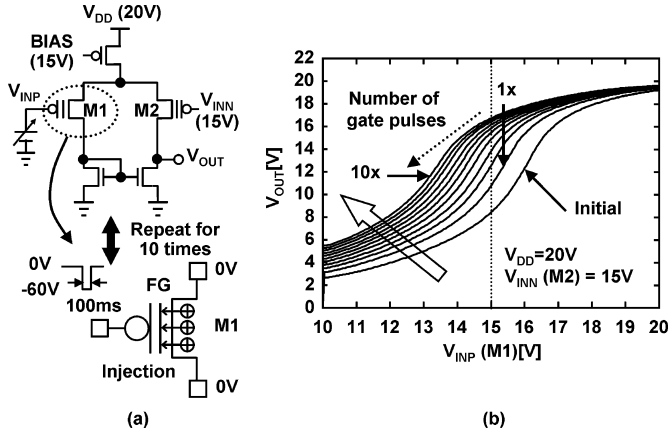


Fig. 15. Measured $V_{\rm OUT} - V_{\rm IN}$ characteristics of operational amplifier. (a) Schematic. (b) Measured result.

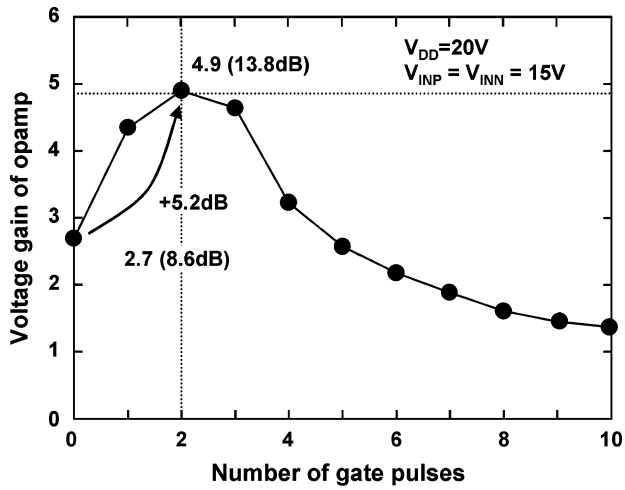


Fig. 16. Measured dependence of operational amplifier gain on the number of pulses.

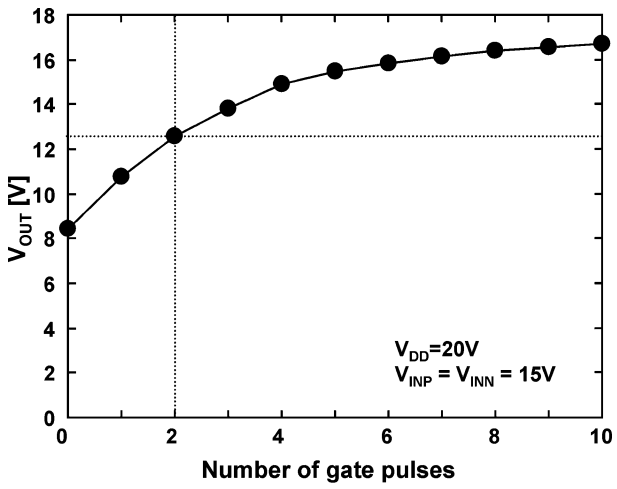


Fig. 17. Measured dependence of output voltage of operational amplifier on the number of pulses.

increased by 5.2 dB using the proposed FG programming, while the offset is suitably reduced. To increase the differential voltage gain, the differential transistors must be biased correctly. The compensation of mismatch is also important for increasing the

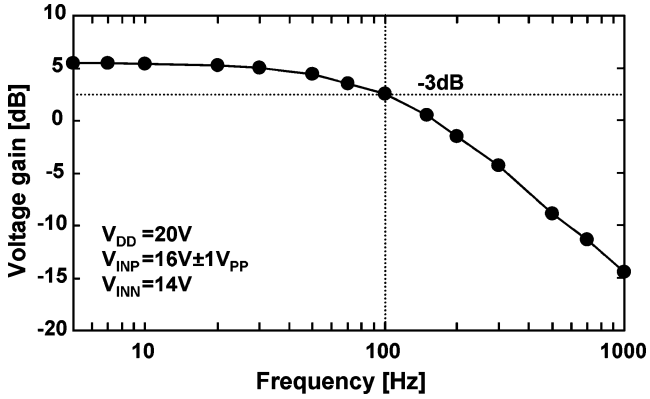


Fig. 18. Measured frequency response of operational amplifier.

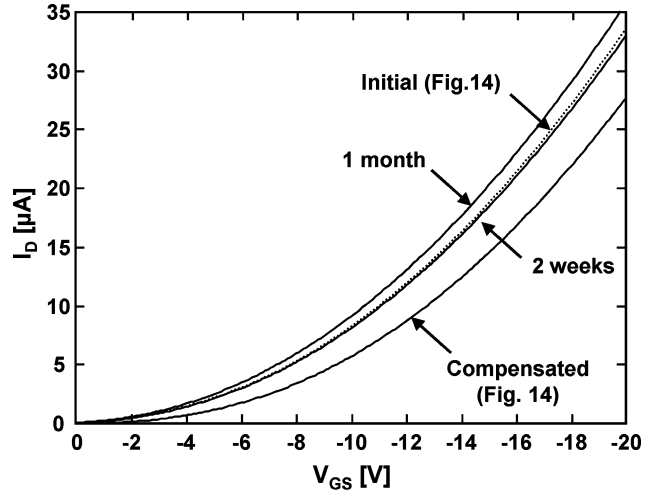


Fig. 19. Measured retention of the compensation by the FG (I_D–$V_{\rm GS}$ for M1 in Fig. 14).

amplifier gain. The proposed compensation scheme of injecting carriers into the FG compensates the device mismatch and improves the gain of the CMOS operational amplifier.

The frequency response of the operational amplifier without compensation was also measured. A 1-V peak-to-peak, 16-V dc offset sinusoidal wave and a 14.1-V dc signal were used for $V_{\rm INP}$ and $V_{\rm INN}$, respectively. The measured open-loop gain is 5.5 dB, the bandwidth is 100 Hz, and GBW is approximately 150 Hz as shown in Fig. 18. Although the uncompensated bandwidth is higher than 50 Hz, the open-loop gain after the proposed compensation is still small. If the performance of the organic nMOS transistors such as the driving capability and the drain current saturation characteristic can be improved, then the performance of the CMOS operational amplifier will be further improved.

The retention of the proposed compensation scheme was also measured. Fig. 19 shows the measured time shift of the $I_{\rm D} - V_{\rm GS}$ characteristics of M1. $V_{\rm TH}$ for M1 shifted by -2 V in two weeks. $V_{\rm TH}$ after a month was lower than its initial value. This means that the effectiveness of the compensation is reduced by the time-dependent degradation of $V_{\rm TH}$. On the other hand, the measured gain still exhibits good retention after a month as shown in Fig. 20. Once M1 is compensated and balanced with M2, both M1 and M2 will track together in the same environment. Therefore, the proposed compensation scheme is still effective for increasing the amplifier gain.

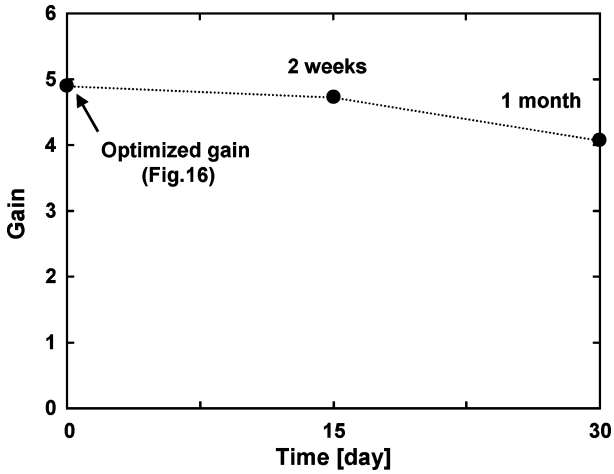
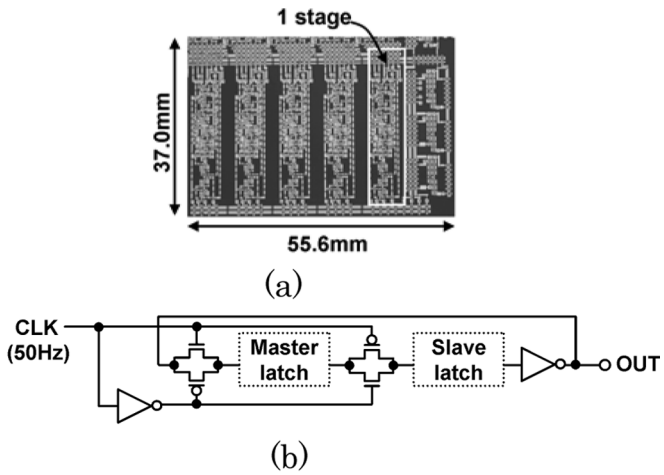


Fig. 20. Measured retention of the compensation by the FG (operational amplifier gain).



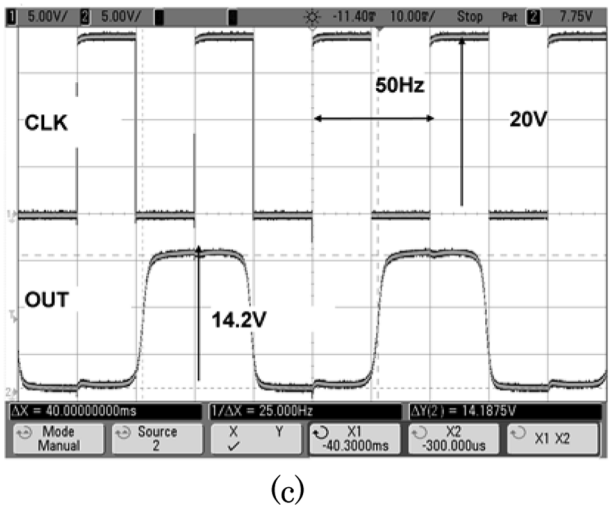


Fig. 21. Pseudo-CMOS-based frequency divider. (a) Photograph. (b) Schematic. (c) Measured waveform.

C. 20-V Pseudo-CMOS-Based 10-b Frequency Divider

Fig. 21(a) shows a photograph of a 5-b pseudo-CMOS frequency divider. Fig. 21(b) shows a schematic of the pseudo-

TABLE I
KEY FEATURES AND SUMMARY OF PERFORMANCE

Organic transistors	
100V PMOS	Pentacene(0.5 cm^2/Vs),
20V CMOS	PMOS:DNTT(0.7 cm^2/Vs), NMOS:NTCDI (0.09 cm^2/Vs)
Gate oxide material, thickness	Parelene, 560nm(100V), 360nm(20V), 240+240nm(20V+FG)
Compensation voltage	-60V(100ms step)
Organic LED	
Forward current	0.3mA@7V
100V AC energy meter	
Target energy and load	360Wh with 500W load
100V PMOS maximum power dissipation	2W (20mA@V_{GS}=-48V, V_{DS}=-100V)
Ring oscillator frequency of Pseudo-CMOS	156Hz@20V
Number of transistors	609Tr.
Total area excluding AC connector	200x200mm^2(unfolded), 70x70mm^2(folded)

CMOS frequency divider used to divide the frequency by two. Owing to the high gain of the pseudo-CMOS inverter, the divider successfully operates at 50 Hz and 20 V as shown in Fig. 21(c).

Table I provides the key features and a summary of the performance of the proposed 100-V ac energy meter. The energy meter consists of 609 transistors and its total area excluding the ac connector is 200×200 mm^2 (unfolded) or 70×70 mm^2 (folded).

V. CONCLUSION

A 100-V ac energy meter based on the SoF concept, which integrates various devices on a flexible film, was presented. The system includes key technologies such as a 100-V pMOS cross-coupled full-wave rectifier to improve the output current by 24%, a 20-V operational amplifier that compensates the mismatch of V_{TH} by charge injection into the FG, thus improving the gain by 5.2 dB, and a 20-V pseudo-CMOS-based frequency divider. The energy meter based on the SoF is flexible and therefore can be installed to monitor each ac outlet simultaneously. The energy meter is expected to be formed using a low-cost printing process in the future. Organic SoF integration is expected to pave the way for future low-cost and flexible electronics.

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