Startup Techniques for 95 mV Step-Up Converter by Capacitor Pass-On Scheme and V_{TH}-Tuned Oscillator With Fixed Charge Programming

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***Abstract*—This paper presents a 95 mV startup-voltage step-up DC-DC converter for energy harvesting applications. The capacitor pass-on scheme enables operation of the system from an input voltage of 95 mV without using additional off-chip components. To compensate for the die-to-die process variation, post-fabrication threshold voltage (V_{TH}) trimming is applied to reduce the minimum operating voltage (V_{DDMIN}) of the oscillator. Experimental results demonstrate the 34% V_{DDMIN} reduction of the oscillator by post-fabrication V_{TH} trimming. The proposed step-up converter achieves the lowest startup voltage in standard CMOS without using a mechanical switch or large transformer.**

***Index Terms*—Boost converter, capacitor pass-on, DC-DC converter, energy harvesting, fixed-charge programming, low voltage, startup, V_{TH}-tuned oscillator.**

I. Introduction

HARVESTING energy from the environment by using thermoelectric generators (TEG) or the photovoltaic cells provides solutions for battery-free sensor networks or electronic healthcare systems [1]–[3]. One of the main challenges is the extremely low output voltage that the energy harvesters can provide. The TEG generates output voltages in the range of 10 mV/K to 50 mV/K, depending on its process and size. For body-wearable applications, the output voltage is less than 100 mV for a temperature difference of 2K. The output voltage of a single solar cell is 500 to 600 mV outdoors but becomes as low as 100 to 200 mV in dark office environments. These voltages are lower than the threshold voltages (V_{TH}) of most standard CMOS technologies. Even in advanced CMOS technologies, the V_{TH} is still around 400 mV and is difficult to operate under subthreshold region. Therefore, a low-startup voltage step-up DC-DC converter is required to kick-start the system. It also needs to convert the harvested energy to usable output voltages because the harvested voltages are too low for electronic devices.

In this paper, a 95 mV startup voltage step-up converter without mechanical stimuli is proposed to extend the applicability of energy harvesting [4]. The proposed circuit converts the 100 mV input to 0.9 V output at 0.9 mA load current. We also propose a V_{TH}-tuned oscillator trimmed by fixed charge programming to compensate for the die-to-die process variation. The minimum operating voltage (V_{DDMIN}) of the oscillator can be reduced by 34%. The circuit demonstrates the feasibility of countermeasures for the process variation that limits the V_{DDMIN} of an on-chip ring oscillator.

This paper is organized as follows. Startup techniques for low input voltage DC-DC converters are introduced in Section II. Section III describes the proposed system architecture. Section IV explains the circuit implementation of the proposed voltage detector. Section V shows the circuit implementation of the V_{TH}-tuned oscillator with fixed charge programming. The experimental results and comparison with the state-of-the-art are shown in Section VI. Finally, a conclusion will be drawn in Section VII.

II. Startup Techniques in DC-DC Converters

Developing a startup mechanism is one of the most critical issues for low input voltage DC-DC converters [5]. The concept of the conventional step-up converter startup mechanism is illustrated in Fig. 1 [6]. The startup mechanism is used to generate a higher auxiliary voltage ($> V_{TH}$) and charges C_{OUT}. It can be an external voltage or another power management circuit. Once the C_{OUT} is charged to a high voltage, the control circuit can be powered by V_{OUT}. The control circuit then drives the power devices in the DC-DC converter with sufficient amplitude ($> V_{TH}$) for the DC-DC converter to function. The V_{OUT} is now charged by the main DC-DC converter and supplies the control circuit. The key technique in the scheme is to generate an auxiliary voltage higher than V_{TH} to C_{OUT}.

Until now, several startup techniques were reported [6]–[11] for low voltage operation. [6], [7] kick start the system by applying the auxiliary voltage directly to the output. The 650 mV external voltage and 2 V battery are required in [6] and [7], respectively. A battery-less 35 mV startup boost converter was implemented by using a mechanically assisted step-up process

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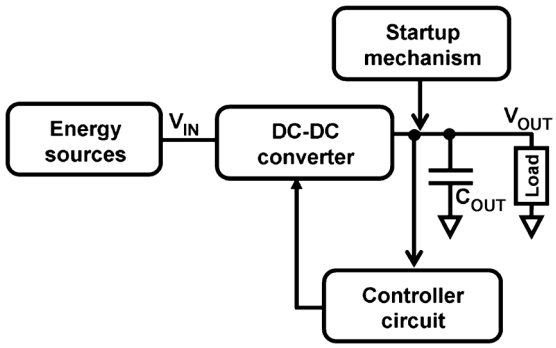

Fig. 1. Concept of the conventional step-up converter with a startup mechanism [6].

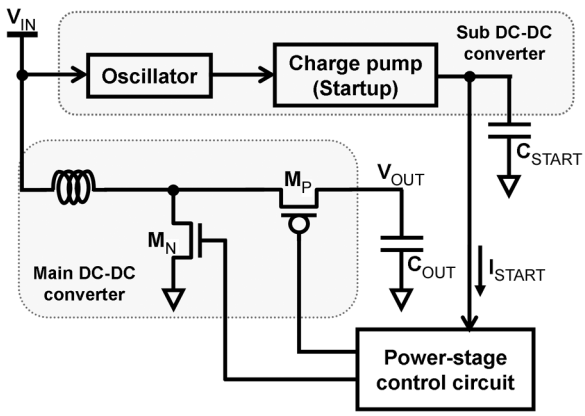

Fig. 2. Conventional startup mechanism in [12].

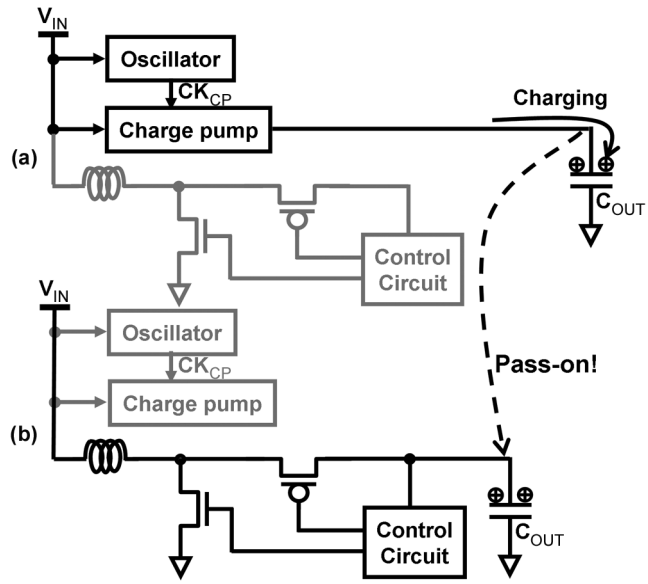

Fig. 3. Proposed capacitor pass-on scheme to kick-start the system. (a) Startup mode. (b) Operation mode.

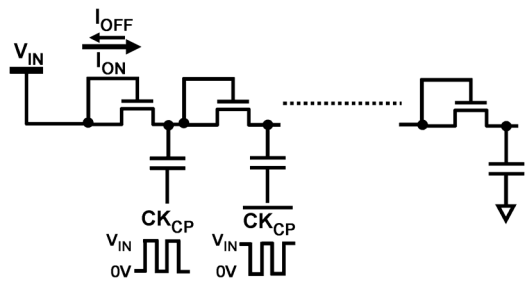

Fig. 4. The circuit schematic of the 20-stage dickson charge pump.

[8]. It uses a mechanical switch to eliminate the clock requirement at startup but vibration is required to activate the mechanical switch. This limits the application and increases the cost. A completely electronic startup step-up converter without using an external voltage was presented in [9]–[11]. Refs. [9] and [10] use a transformer with a large turn ratio and are not well suited for portable applications. In [11], it eliminates a transformer but the startup voltage is limited to 330 mV. Therefore, our main target in this work is to design a CMOS on-chip startup mechanism with minimal off-chip components.

Fig. 2 shows a previous CMOS on-chip startup technique reported in [12]. It applies a charge pump (CP) to generate high voltage for the control circuit and kick-start the system from 180 mV. In this approach, two off-chip capacitors are required. One (C_{START}) is for the CP and the other (C_{OUT}) is for the boost converter. When operating under low input voltage (V_{IN}), the CP is so weak that it cannot build up the higher voltage when even a small amount of leakage exists. Therefore, the startup voltage is limited by the power consumption of the control circuit (I_{START}). This startup voltage is higher than our target (100 mV) and further improvement is required.

To reduce the startup voltage, we propose the capacitor pass-on scheme for the startup mechanism. The operation concept of the capacitor pass-on scheme is shown in Fig. 3. C_{START} in Fig. 2 can be eliminated by using the output capacitor of the boost converter, C_{OUT}, as the charge buffer of the CP. During startup, C_{OUT} is charged by the on-chip 20-stage Dickson-type CP [13], as shown in Fig. 4. The pumping capacitor in each stage is 3 pF. The CP is driven by an on-chip CMOS oscillator, which generates a 330 kHz clock signal when provided supply voltage as low as 95 mV. In conventional approach, Dickson charge pump is diode connected and has the diode voltage drop between stages. In our application, however, the output current is limited during startup and the output capacitor is available to be charged to a high voltage. Even though the clock amplitude is smaller than V_{TH}, there still exists the current difference between I_{ON} and I_{OFF}, as shown in Fig. 4. This current difference charges the pumping capacitor and pumps up the output voltage. Since the amplitude of the clock provided to CP (CK_{CP}) is small, the available output current of the CP is limited. Therefore, we cut off the current path of the control circuit to minimize the output current in startup mode.

When C_{OUT} is charged to the preset voltage, C_{OUT} is "passed on" with its charge inside to be the boost converter and supplies the control circuit. To turn on the power transistors M_N and M_P by using the control circuit, C_{OUT} should be charged to higher than V_{TH}. In our design, the V_{TH} of the power transistors is about 400 mV. Therefore, the preset voltage is designed to 460 mV to make sure the clock amplitude is enough to turn-on the power transistors. By using the proposed scheme, the startup voltage can be reduced to 95 mV and the large external capacitor C_{START} in Fig. 2 can be eliminated.

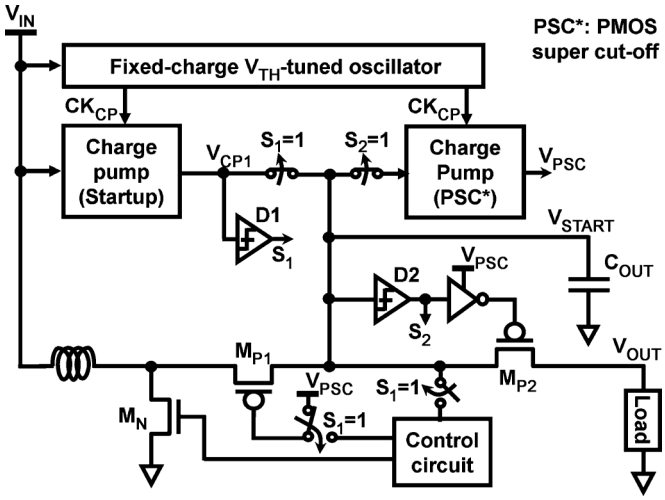

Fig. 5. Block diagram of proposed step-up converter with capacitor pass-on scheme. The switch status in the figure represents the initial state. S_1 and S_2 are control signals.

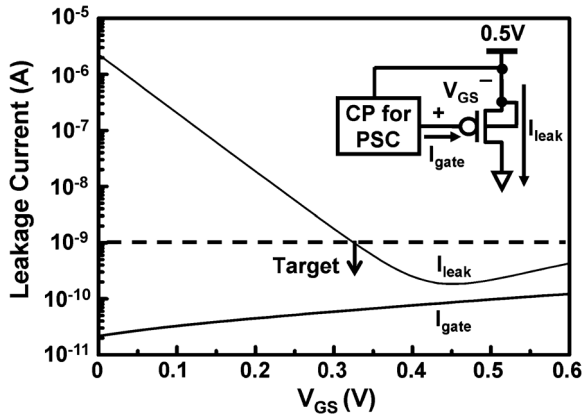

Fig. 6. Simulated dependence of leakage current on gate over-drive voltage.

III. System Architecture

The detailed block diagram of the proposed step-up DC-DC converter with the capacitor pass-on scheme is shown in Fig. 5. It consists of power transistors M_N, M_{P1}, M_{P2}, a fixed-charge V_{TH}-tuned oscillator, the CP for startup, CP for pMOS super cut-off (PSC), the control circuit, and two voltage detectors D1 and D2. The switch status in this figure represents the initial state. S_1 and S_2 are the control signals for the switches. In our design, the target is to verify the on-chip startup mechanism in the DC-DC converter. The control circuit generates the pulse signal with fixed duty cycle for the power transistors but does not include the pulse-width modulation control.

The fixed-charge V_{TH}-tuned oscillator is used to generate the clock signals for the CP during startup. In our application, the oscillator needs to function under sub-100 mV supply voltage. The CP for startup is designed to charge the output capacitor (C_{OUT}) at the startup. Although the control circuit is not connected to C_{OUT}, the leakage current of the power transistors M_{P1} and M_{P2} still limit the startup voltage. To reduce the leakage current, we applied the CP for PSC to provide the overdrive voltage to the gate of pMOS transistors (M_{P1} and M_{P2}). The simulated dependence of leakage current on gate overdrive voltage is shown in Fig. 6. As can be seen, before providing the gate overdrive voltage, the leakage current is 1 μA, which is too large for the low-voltage CP. Our target leakage current of each power transistor is below 1 nA. Therefore, we applied 0.35 V of gate overdrive voltage to reduce the leakage current.

Fig. 7 illustrates the operation sequences of the proposed step-up DC-DC converter. There are three modes, the startup mode, the warm-up mode and the operation mode. These modes are selected by using two voltage detectors D1 and D2 with different trigger voltages. During the startup mode, the C_{OUT} is charged by CP and V_{START} rises. When V_{CP1} $(= V_{START}$ @Startup) is pumped to the preset trigger voltage of D1, the node S_1 changes from low to high to pass the C_{OUT} on to the boost converter.

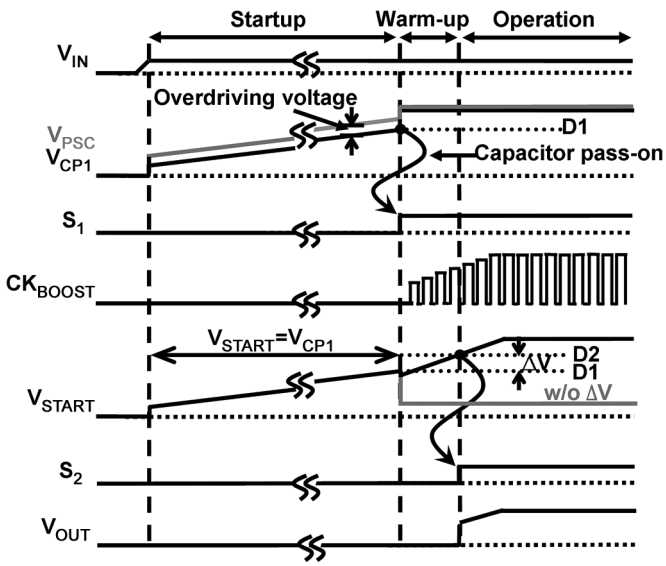

Fig. 7. Waveforms illustrating the operation sequences of the proposed step-up converter.

The warm-up mode is used to ensure the output switch M_{P2} turns on after the boost converter starts working and the output can be boosted smoothly. During this mode, C_{OUT} becomes a kind of power supply. The charge stored in C_{OUT} activates the control circuit and starts driving the boost converter. The control circuit must provide enough voltage amplitude $(> V_{TH})$ to drive the power transistors M_N and M_{P1}. The power transistor M_{P2} does not turn-on immediately when the capacitor is passed-on. If the load is connected at the same time when the capacitor is passed-on (w/o warm-up mode), the charge stored in C_{OUT} drains out and the boost converter fails to startup. To overcome this problem, a voltage detector D2 with 60 mV higher trigger voltage compared to D1 is added to delay the load connection timing a bit. When V_{START} is boosted to the preset trigger voltage of D2, the node S_2 changes from low to high and V_{OUT} is almost equal to V_{START}. During the operation mode, the C_{OUT} becomes an output capacitor of the boost converter to smooth the output voltage.

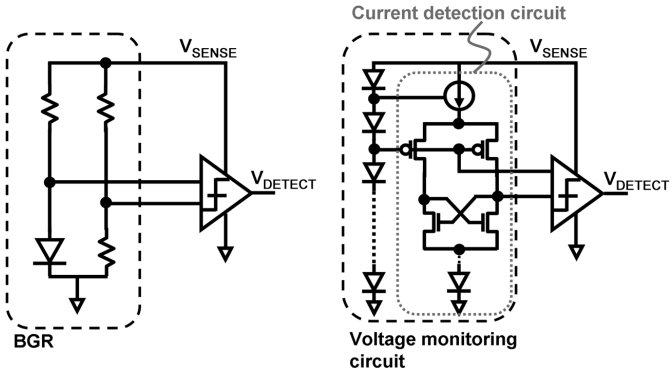

Fig. 8. Conventional voltage detector using (a) BGR and (b) voltage monitoring circuit in [14].

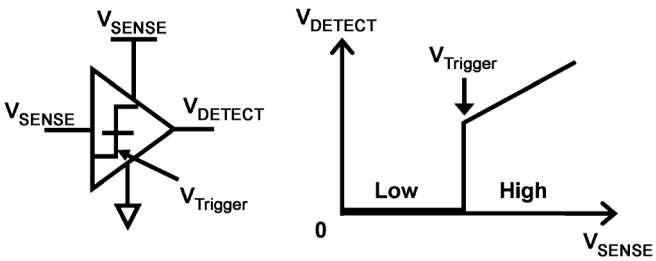

Fig. 9. Waveform illustrating the proposed voltage detector.

IV. Voltage Detector

The modes of the proposed step-up converter can be automatically changed by detecting the capacitor voltage ($\mathrm{V_{START}}$). The key building blocks in this scheme are the voltage detectors D1 and D2. Since the detector D1 and D2 are directly connected to $\mathrm{C_{OUT}}$ at startup, they act as the load of the CP. Again, since the CP is weak during startup, the operating current of the detectors may spoil the normal startup. Thus, the power consumption of the detectors should be minimized.

Conventionally, the voltage is detected by using the bandgap reference (BGR) and a comparator, as shown in Fig. 8(a). The BGR consumes several microwatts since it uses DC-biased resistors. Another approach uses a voltage monitoring circuit instead of BGP to reduce the power consumption [14], as shown in Fig. 8(b). The voltage monitoring circuit, however, needs a high supply voltage to realize the current detection circuit. In our startup mechanism, both low-voltage and low-power detector circuit is required to switch the operation modes. To meet this requirement, we propose a reference-less CMOS voltage detector with 1.6-nW power consumption, as shown in Fig. 9. To further decrease the power consumption, the proposed scheme eliminates the comparator and only one input signal is applied ($\mathrm{V_{SENSE}}$). It can detect the voltage level of the $\mathrm{V_{SENSE}}$ and provide the trigger signal to the switches. In the following, the circuit design of the proposed voltage detector will be described in detail.

Fig. 10 shows the circuit schematic of the detector core. The detector core consists of two cascode transistors: $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$. Both transistors were chosen to be pMOS transistors because all pMOS configuration has less process variation than NMOS-

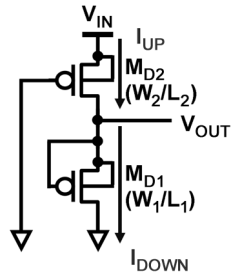

Fig. 10. Circuit schematic of the proposed voltage detector core.

PMOS configuration. The trigger voltage in this scheme is determined by comparing the currents $\mathrm{I_{UP}}$ and $\mathrm{I_{DOWN}}$. The circuit is operating under subthreshold region, thus the current draw through the transistor $\mathrm{M_{D2}}$ can be given as [15]

$$I_{UP} = I_0 e^{q\frac{V_{GS}-V_{th}}{mkT}}\left(1 - e^{q\frac{-V_{DS}}{kT}}\right) \tag{1}$$

$$I_0 = \mu C_{OX}\frac{W_2}{L_2}\left(\frac{kT}{q}\right)^2 = K\frac{W_2}{L_2} \tag{2}$$

where k is the Boltzman constant, μ is the hole mobility, $\mathrm{C_{OX}}$ is the gate oxide capacitance per area and m is the subthreshold swing coefficient ($\mathrm{m} > 1$). kT/q is the thermal voltage and is approximately 26 mV at room temperature ($T = 300$ K). If $\mathrm{V_{DS}}$ is large enough ($\mathrm{V_{DS}} > 100$ mV), $\mathrm{I_{UP}}$ can be simplified as

$$I_{UP} = K\frac{W_2}{L_2}e^{q\frac{V_{IN}-V_{th}}{mkT}}. \tag{3}$$

Therefore, $\mathrm{I_{UP}}$ increases exponentially as $\mathrm{V_{IN}}$ increases. Similarly, the transistor $\mathrm{M_{D1}}$ is also operating in the subthreshold region ($\mathrm{V_{GS}} = 0$) and assuming $\mathrm{V_{DS}}$ is large enough ($\mathrm{V_{DS}} > 100$ mV). To reduce the power consumption, the gate of $\mathrm{M_{D1}}$ is connected to its source and only off-current ($\mathrm{I_{DOWN}}$) flows. The current $\mathrm{I_{DOWN}}$ can be given as

$$I_{DOWN} = K\frac{W_1}{L_1}e^{q\frac{-V_{th}}{mkT}}. \tag{4}$$

As can be seen, $\mathrm{I_{DOWN}}$ is constant and only depends on the transistor ratio. The trigger voltage ($\mathrm{V_{Trigger}}$) is defined as $\mathrm{V_{IN}}$ when $\mathrm{V_{OUT}}$ changes from low to high. Therefore, $\mathrm{V_{Trigger}}$ is the input voltage when $\mathrm{I_{UP}} = \mathrm{I_{DOWN}}$, which can be written as

$$V_{IN} = V_{Trigger} = \frac{mkT}{q}\mathrm{In}\left(\frac{W_1}{W_2}\times\frac{L_2}{L_1}\right). \tag{5}$$

This equation shows that $\mathrm{V_{Trigger}}$ can be tuned easily by designing the transistor size of $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$. Although $\mathrm{V_{Trigger}}$ is proportional to the temperature, this is not a critical problem in our application. This is because the circuit is targeted for body-wearable applications or indoor solar cells. Therefore, the temperature variation is limited.

In our application, $\mathrm{V_{Trigger}}$ is designed to be larger than $\mathrm{V_{TH}}$ of the transistors. Assuming $\mathrm{V_{Trigger}}$ is 460 mV at room temperature and $\mathrm{m} \approx 1.1$, the transistor ratio of $\mathrm{M_{D2}}$ and $\mathrm{M_{D3}}$ can be calculated as

$$\left(\frac{W_1}{L_1}\right)\Big/\left(\frac{W_2}{L_2}\right) = e^{q\frac{V_{Trigger}}{mkT}} \approx 9700000. \tag{6}$$

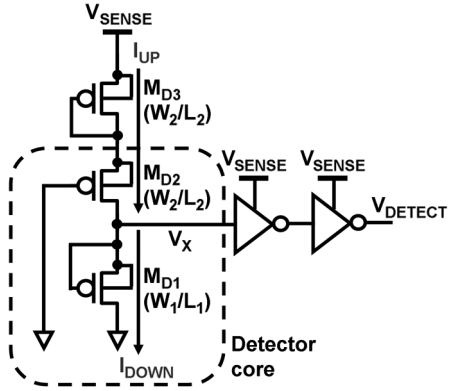

Fig. 11. Circuit schematic of the proposed voltage detector with a diode connected transistor to adjust the trigger voltage.

This ratio is too large and is not practical for implementation. To solve this problem, we added a diode-connected pMOS transistor $\mathrm{M_{D3}}$ with transistor size of $\mathrm{W_2/L_2}$ to almost double the trigger voltage, as shown in Fig. 11. Since the transistor size of $\mathrm{M_{D2}}$ and $\mathrm{M_{D3}}$ are the same. From (1), $\mathrm{V_{GS}}$ of $\mathrm{M_{D2}}$ and $\mathrm{M_{D3}}$ are the same. The transistor ratio of $\mathrm{M_{D1}}$ and $\mathrm{M_{D2}}$ can be modified as

$$\left(\frac{W_1}{L_1}\right) \Big/ \left(\frac{W_2}{L_2}\right) = e^{q\frac{V_{Trigger}}{2mkT}} \approx 3100 \qquad (7)$$

which is possible to implement in practice. Adding a transistor $\mathrm{M_{D1}}$, however, reduces the voltage amplitude of node $\mathrm{V_X}$ to 0.5 $\mathrm{V_{SENSE}}$. Therefore, we designed two-stage inverters to amplify the voltage swing.

The simulation results of the proposed voltage detector are shown in Fig. 12. In our design, the channel width and channel length are designed as follows: $\mathrm{W_2} = 0.2\ \mu$m, $\mathrm{L_1} = 0.13\ \mu$m, and $\mathrm{L_2} = 2\ \mu$m. The $\mathrm{W_1}$ of voltage detectors D1 and D2 are 63 μm and 144 μm, respectively. As can be seen, the trigger voltage difference (ΔV in Fig. 7) between D1 and D2 can be designed by changing the channel width $\mathrm{W_2}$. The voltage $\mathrm{V_X}$ rises when the $\mathrm{V_{SENSE}}$ is close to $\mathrm{V_{Trigger}}$ and amplified by the inverter buffer. Therefore, the output voltage ($\mathrm{V_{DETECT}}$) changes from low to high sharply at $\mathrm{V_{Trigger}}$. Fig. 13 shows the simulated dependence of power dissipation on $\mathrm{V_{SENSE}}$. The spikes in current are due to the buffer inverter shoot-through in trigger voltage. This current can be mitigated by adjusting the transistor size of the buffer. Reducing the W/L ratio of the transistors can minimize this current. The power consumption of the startup mode is most critical because it is charged by the low-voltage CP. From the simulation, we can obtain that the proposed voltage detector consumes less than 1.6 nW when $\mathrm{V_{SENSE}} < \mathrm{V_{Trigger}}$ (Startup mode). The proposed voltage detector achieves both low voltage and low power operation to detect the desired voltage.

V. Fixed-Charge $\mathrm{V_{TH}}$-Tuned Oscillator

The fixed-charge $\mathrm{V_{TH}}$-tuned oscillator is used to generate the clock signal for the charge pump. The minimum operation voltage ($\mathrm{V_{DDMIN}}$) of the oscillator limits the startup voltage of the step-up DC-DC converter in standard CMOS technology.

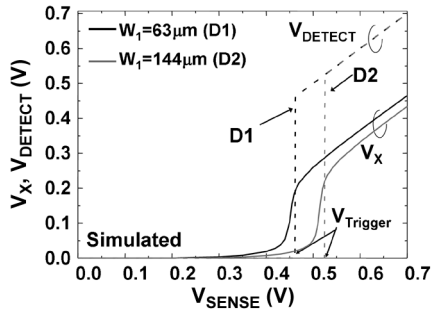

Fig. 12. Simulation results of the proposed voltage detector depicting the dependence of $\mathrm{V_X}$ and $\mathrm{V_{DETECT}}$ on $\mathrm{V_{SENSE}}$.

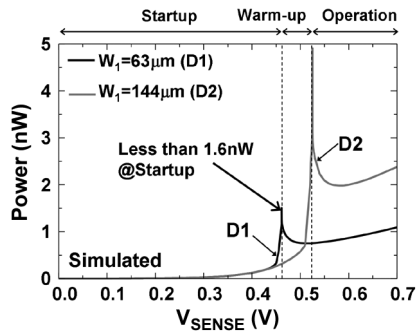

Fig. 13. Simulated dependence of power consumption on $\mathrm{V_{SENSE}}$.

This is because the clock signal is required for a charge pump when starting up the system.

Practically, the $\mathrm{V_{DDMIN}}$ of an oscillator is usually limited by PMOS-NMOS $\mathrm{V_{TH}}$ imbalance caused by within-die and die-to-die $\mathrm{V_{TH}}$ variations. The within-die $\mathrm{V_{TH}}$ variation issue can be solved by increasing the channel width and thus it can be easily solved in this application. The problem is the die-to-die variation which is usually adjusted by controlling the body bias of the MOSFETs. In the startup circuit, however, a body-biasing circuit would not function before the system startup because only the input voltage exists in the system. Therefore, a new technique is required to compensate for the die-to-die process variation without using body biasing.

Fig. 14 shows the simulation results of a $\mathrm{V_{DDMIN}}$ of 15-stage inverter-based ring oscillator under different process corners. SS means slow nMOS and slow pMOS. ST means slow nMOS and typical pMOS, and so on. The simulation results show that $\mathrm{V_{DDMIN}}$ of lower than 100 mV can be achieved if the $\mathrm{V_{TH}}$ of nMOS and pMOS are well balanced. Therefore, if we can adjust the threshold voltage of transistors, for example, adjust fast nMOS slow pMOS to slow nMOS slow PMOS, $\mathrm{V_{DDMIN}}$ can be reduced from 173 mV to 73 mV, which is as low as the target operation voltage.

To make sure the circuit functions even under the die-to-die process variation, we proposed a new fixed-charge $\mathrm{V_{TH}}$-tuned oscillator. The $\mathrm{V_{TH}}$ of the transistors in the ring oscillator and the buffer are trimmed by fixed-charge programming to make sure the circuit functions even under die-to-die process variation. The detailed circuit schematic is shown in Fig. 15. The circuit consists of a 15-stage inverter-based ring oscillator and inverter-based output buffer. We added two pads for the substrate

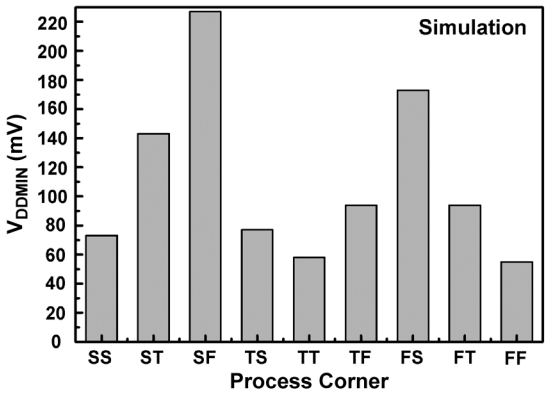

Fig. 14. Simulation results of V_{DDMIN} of oscillator under different process corners. SS means slow nMOS and slow pMOS, TF means typical nMOS and fast pMOS, and so on.

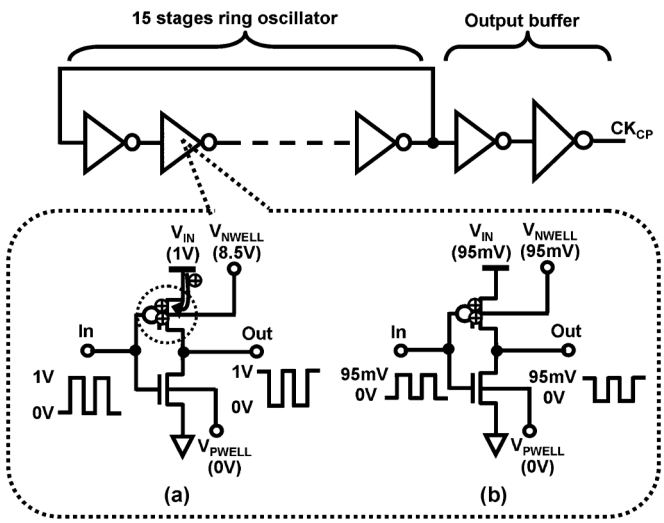

Fig. 15. Circuit schematic of the proposed fixed-charge V_{TH}-tuned oscillator. (a) Program mode. (b) Normal mode.

of the pMOS (V_{NWELL}) and nMOS (V_{PWELL}) transistors to provide the body bias.

To reduce within-die process variation, the transistor width of the inverter in the oscillator is designed at least 16 times larger than the standard cell. In the measured chips, since the V_{TH} of an nMOS (V_{TN}) was higher than that of a pMOS (V_{TP}), V_{TP} is adjusted (increased) to reduce the V_{DDMIN} of the oscillator here. This is because the fixed-charge programming is much easier to increase the V_{TH} than to reduce the V_{TH}.

In program mode, the power supply is set to 1 V and the ring oscillator oscillates. In pMOS programming, the V_{TP} is programmed by applying high reverse body bias to all pMOS transistors ($V_{NWELL} = 8.5$ V) while the body of nMOS transistors are connected to the source ($V_{PWELL} = 0$). Because the high reverse body bias is provided, positive charges are injected into the gate dielectrics when AC current flows. This AC current is caused by the flow-through current when the clock signal changes its state. The injected charge is fixed in the dielectrics and increases the V_{TP} even after the high reverse body bias is removed. Note that the V_{TP} shift shows nonvolatile characteristics and does not require any additional process steps. Since

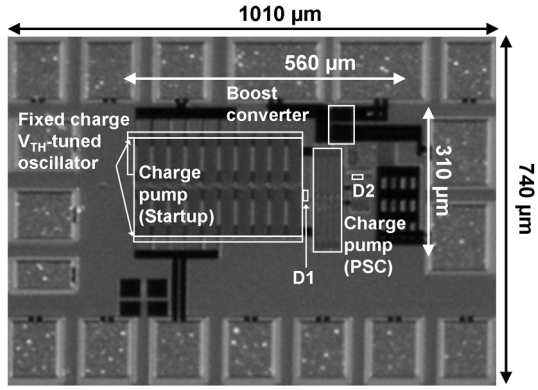

Fig. 16. Chip micrograph of dual-mode boost converter in 65-nm CMOS.

no body bias is applied to the nMOS transistors, the V_{TN} is not programmed and remain the same voltage.

When V_{DDMIN} of the ring oscillator is decreased to lower than our target voltage, the post-fabrication programming can be stopped. The circuit is then operating under normal mode and only a 95 mV supply is provided. The V_{NWELL} in normal mode is provided to V_{IN} to avoid the body effect. The injected charge is still fixed in the pMOS transistor and the $|V_{TP}|$ remains higher than the initial value. $|V_{TP}|$ is now balanced with V_{TN} and V_{DDMIN} of the oscillator can be reduced. Now, the circuit can be operating under 95 mV and drives the CP at such a low voltage.

We introduced the pMOS programming in this paper. Similarly, if V_{TP} is higher than V_{TN} and nMOS programming is required, the high reverse voltage to V_{PWELL} and 1 V supply to V_{NWELL} can be applied to increase V_{TN}.

VI. Experimental Results

The test chip is fabricated using 65-nm standard CMOS technology. Fig. 16 shows the chip micrograph of the proposed step-up DC-DC converter. The active area including the fixed-charge V_{TH}-tuned oscillator, the CP for startup, the CP for PSC and the boost converter is 0.17 mm^2. The circuit is measured with an off-chip inductor of 6.8 μH and an off-chip capacitor of 10 nF. The startup circuit is all implemented on-chip and there are no additional devices for the startup mechanism.

Fig. 17 shows the measured dependences of V_{DDMIN} of the fixed-charge V_{TH}-tuned oscillator on trimming time. Three test chips are measured to verify V_{DDMIN} improvement. The V_{TH} of the pMOS transistors are increased as trimming time increases and 34% of V_{DDMIN} reduction is achieved in 60 minutes. In this prototype design, we manually tested the chip and obtain the V_{DDMIN}. The trimming time depends on the bias condition of the circuit. The trimming time will be reduced by applying higher reverse body bias and higher supply voltage. The reverse body bias is limited by the p-n junction breakdown voltage and the supply voltage is limited by the gate breakdown voltage. By applying the fixed-charge programming, the V_{DDMIN} of the oscillator can be reduced from 125 mV to 82 mV, which achieves our design target. Fig. 18 shows the measured dependences of V_{DDMIN} variation over the time after programming is finished. In this test, the circuit is operating under the operation mode and 95 mV supply

TABLE I
COMPARISON WITH PUBLISHED LOW-STARTUP VOLTAGE STEP-UP DC-DC CONVERTER

	[6]	[16]	[12]	[8]	This work
Startup mechanism	External voltage	Charge pump	Charge pump	Mechanical switch	Capacitor pass-on
Min. startup voltage	650mV	360mV	180 mV	35mV	95mV
Typical input (V_{IN})	100mV	180mV	180mV	50mV	100mV
Process	130nm CMOS	350nm SOI-BCD	65nm CMOS	350nm CMOS	65nm CMOS

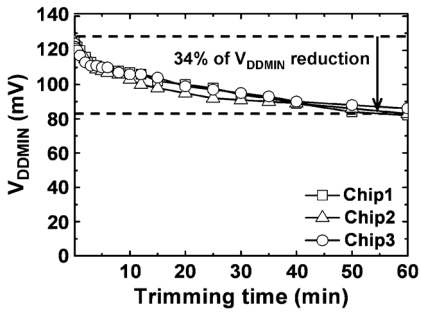

Fig. 17. Measured dependence of V_{DDMIN} of V_{TH}-tuned oscillator with fixed charge programming on trimming time for 3 dies.

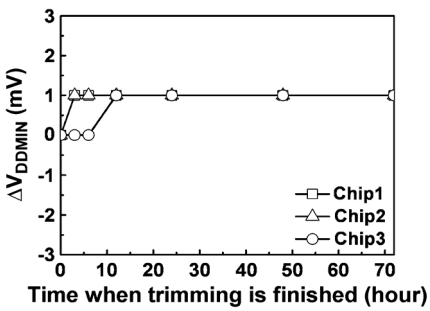

Fig. 18. Measured dependence of V_{DDMIN} change on time when trimming is finished.

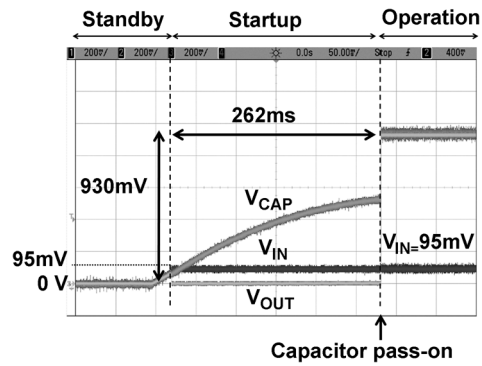

Fig. 19. Measured startup waveforms of the proposed step-up converter.

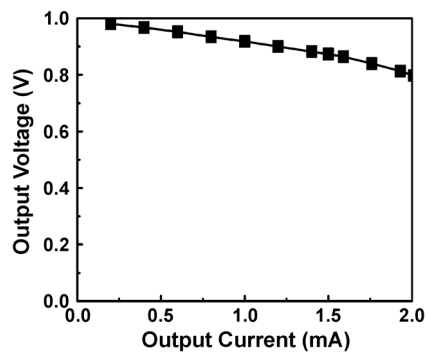

Fig. 20. Measured dependence of the output voltage on load current.

voltage is provided without any high reverse body bias. Even after the high reverse body bias is removed, the change is as small as 1 mV after 3 days of stress and becomes stable.

Fig. 19 shows measured startup waveforms of the proposed step-up DC-DC converter with the capacitor pass-on scheme. The circuit is measured with a 95 mV ideal power supply without any external clocks or mechanical switches. The CP for startup pumps up the external capacitor and passes on the capacitor to the boost converter after 262 ms. The output voltage V_{OUT} is obtained after the circuit is operating under operation mode. The waveforms during warm-up mode cannot be obtained in the measurement because the warm-up time is too short. The oscilloscope waveform demonstrates that the proposed converter is successfully started from the 95 mV input.

In this system, the start-up voltage is limited by both V_{DDMIN} of the oscillator and driving capability of the charge pump. The 95 mV startup voltage in this design is limited by the charge pump because the V_{DDMIN} of the oscillator can be reduced to 82 mV. If the clock amplitude is too small, the charge pump can not provide enough current to supply the output load. In addition, the external capacitor can not be charged to the preset trigger voltage and the system fails to startup. In the trigger voltage, the simulated leakage current of the power transistor is 1.1 nA (M_{P1} and M_{P2}). The current consumed by D1 and D2 is 3.5 nA and 0.7 nA, respectively. 5.1 nA is consumed by the CP for PSC and 0.05 nA is consumed by control circuit during startup. Therefore, the CP needs to provide at least 10.5 nA output current to charge the output loads and an output capacitor.

The measured output voltage versus the current delivered to the load under 100 mV input is shown in Fig. 20. The output voltage is up-converted to higher than 0.8 V in our target output current.

The performance comparison between our circuit and the state-of-the-art step-up DC-DC converters with a startup mechanism is shown in Table I. The proposed startup mechanism achieves the lowest startup voltage except reference [8], which requires mechanical switch to assist the startup. By using the capacitor pass-on scheme, the startup voltage of 95 mV is achieved by using the CMOS technology only without any external clocks or mechanical switches.

VII. Conclusion

A step-up DC-DC converter with low startup-voltage for energy harvesting applications is proposed. Capacitor pass-on scheme enabled by the low power voltage detector reduces the startup voltage from 180 mV to 95 mV. In addition, the number of off-chip capacitors can be reduced from 2 to 1. The proposed circuit also demonstrates the feasibility of countermeasures for the die-to-die process variation that limits the minimum startup voltage of an on-chip ring oscillator. The V_{DDMIN} of the oscillator can be reduced from 125 mV to 82 mV. As a result, the lowest startup voltage of 95 mV is achieved by using the on-chip startup mechanism.

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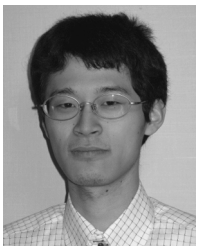

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