A 1-V-Input Switched-Capacitor Voltage Converter With Voltage-Reference-Free Pulse-Density Modulation

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***Abstract*—A 1-V-input 0.45-V-output switched-capacitor (SC) voltage converter with voltage-reference-free pulse-density modulation (VRF-PDM) is proposed. The all-digital VRF-PDM scheme improves the efficiency from 17% to 73% at 50-μA output current by reducing the pulse density and eliminating the voltage reference circuit. An output voltage trimming by the hot-carrier injection to a comparator and a periodic activation scheme of the SC voltage converter are also proposed to solve the problems attributed to VRF-PDM. The proposed voltage converter is fabricated in 65-nm CMOS and achieves an efficiency value of 73%–86% at 50 μA–10 mA output current range.**

***Index Terms*—Offset canceling, pulse-density modulation (PDM), switched capacitor (SC), voltage converter, voltage reference.**

I. Introduction

In RECENT years, exploiting near-threshold and subthreshold circuits has become a major trend in low-power applications, which puts forward more critical requirements for low-output-voltage, small-area, and high-efficiency voltage converters. In modern system on chips (SoCs), multiple power domains are required for various circuit blocks. Fig. 1 shows an example of an energy-efficient SoC that utilizes energy-efficient near-threshold logic circuits. Targeting low-power applications, the SoC system uses a 1-V power supply for the overall system. The 1-V power supply is directly supplied to analog/RF and I/O circuits. In order to utilize near-threshold operation, a voltage converter is required to generate a 0.5-V power supply from the 1-V input for the logic circuits, with 50-μA to 10-mA output current range and high power efficiency.

Compared with buck/boost dc–dc converters that use inductors, switched-capacitor (SC) voltage converter is a preferable solution for low-voltage power supplies because of great potential to be fully integrated on-chip. The design challenges

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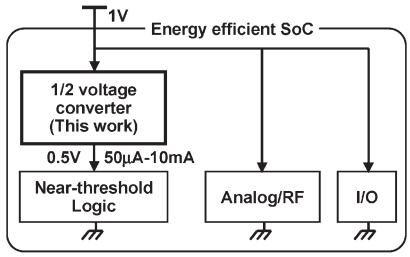

Fig. 1. Power plan of energy-efficient SoC.

of the SC voltage converter are: 1) the degraded efficiency at low output current I_{OUT}; and 2) the implementation of 0.5-V voltage reference circuit (VREF) and the power penalty due to VREF. In addition, the design of sub-1-V VREF is difficult because a typical VREF operates above 1 V. In order to solve the problems, a low-voltage high-efficiency SC voltage converter with voltage-reference-free pulse-density modulation (VRF-PDM) is proposed for high power efficiency at low I_{OUT} by both reducing the pulse density and eliminating VREF [1].

II. VRF-PDM

Two major types of conventional SC voltage converters are shown in Fig. 2(a) and (b). The first type in Fig. 2(a) uses constant pulse density (CPD) for the switch matrix [2]–[4]. In this scheme, a nonoverlap clock generator is employed to drive the switch matrix with a fixed clock frequency, as shown in Fig. 2(c). Therefore, it suffers from severe efficiency drop when output current decreases due to excessive clock pulses for small current demand. Fig. 2(b) shows the other type of conventional SC voltage converter, which relies on VREF and a comparator for pulse-density modulation (PDM) [5]–[9]. The comparator compares the output voltage with the reference voltage to perform PDM. Therefore, the pulse density is adjusted according to different I_{OUT}, thus preventing the efficiency drop due to excessive clock pulses, as shown in Fig. 2(c). Note that the VREF is often omitted in the previous works by simply using an off-chip voltage supply. This way, the power loss introduced by the VREF is overlooked. Moreover, a sub-1-V voltage reference may bring extra design complexity to the voltage converter. Therefore, this scheme costs extra power and area, and it makes the circuit design complicated with low power supply voltage due to the use of an on-chip voltage reference.

Fig. 3 shows the proposed VRF-PDM voltage converter and a timing diagram. The key concept of VRF-PDM is to replace

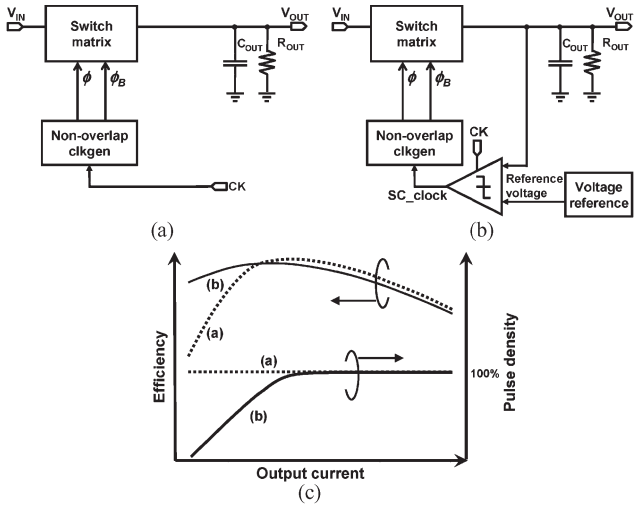

Fig. 2. (a) Conventional SC converter with CPD. (b) Conventional SC converter with PDM. (c) Pulse density and efficiency of (a) and (b).

the reference voltage in Fig. 2(b) with the past output voltage $V_{\rm OUT}$, thereby eliminating VREF. The proposed scheme uses two sampling clocks, i.e., CK and $\rm CK_{UPDATE}$, to sample output voltage at different times. $V_{\rm OUT}$ is sampled as $V_{\rm NOW}$ and $V_{\rm PAST}$ at each falling edge of CK and $\rm CK_{UPDATE}$, respectively. Then, sampled voltages $V_{\rm NOW}$ and $V_{\rm PAST}$ are compared by a comparator with an offset voltage of ΔV. When $V_{\rm PAST} - V_{\rm NOW}$ is larger than ΔV, the comparator output COMP_out is set to high, and then an expanded pulse signal is generated as SC_enable. Applying an AND gate to CK and SC_enable, a pulse signal SC_clock is to be generated and then fed to the nonoverlap clock generator to drive the switch matrix. The $\rm CK_{UPDATE}$ generator is used to generate the required $\rm CK_{UPDATE}$ from CK and SC_enable.

Fig. 4 illustrates the operation of the proposed VRF-PDM voltage converter with different $I_{\rm OUT}$ conditions. Two cases of large $I_{\rm OUT}$ and small $I_{\rm OUT}$ are shown in Fig. 4(a) and (b), respectively. In both cases, $V_{\rm OUT}$ is at first sampled by CK and $\rm CK_{UPDATE}$ and stored as $V_{\rm NOW}$ and $V_{\rm PAST}$, respectively. Then, $V_{\rm OUT}$ goes down due to the current load. $V_{\rm NOW}$ always tracks $V_{\rm OUT}$ with the sampling frequency of CK. A comparator with offset voltage ΔV is used to compare $V_{\rm NOW}$ and $V_{\rm PAST}$ with the sampling frequency of CK. Whenever $V_{\rm PAST} - V_{\rm NOW}$ is bigger than ΔV, a pulse of SC_enable is generated to evoke the switch matrix. Note that the pulse of SC_enable is expanded by the pulse expander shown in Fig. 3 so that $V_{\rm OUT}$ is assured to be fully charged up within each SC_enable pulse signal. At the end of each SC_enable pulse signal, $\rm CK_{UPDATE}$ is generated by the $\rm CK_{UPDATE}$ generator to store the recharged $V_{\rm OUT}$ as a new $V_{\rm PAST}$. Comparing Fig. 4(a) and (b), it is clearly observed that the pulse density of the switch matrix is modulated by the proposed VRF-PDM.

However, in the case of a very small or no output current, VRF-PDM will be problematic because the leak current on the sampling capacitor of $V_{\rm PAST}$ will not be negligible, then the stored $V_{\rm PAST}$ will slowly go down. As shown in Fig. 5(a), $V_{\rm PAST}$ is slowly decreasing together with $V_{\rm NOW}$; hence, $V_{\rm PAST} - V_{\rm NOW}$ is always less than ΔV and SC_enable will be never triggered by the comparator. As a result, there will be no pulse for the switch matrix and $V_{\rm OUT}$ will continuously go down to 0 V due to the output current.

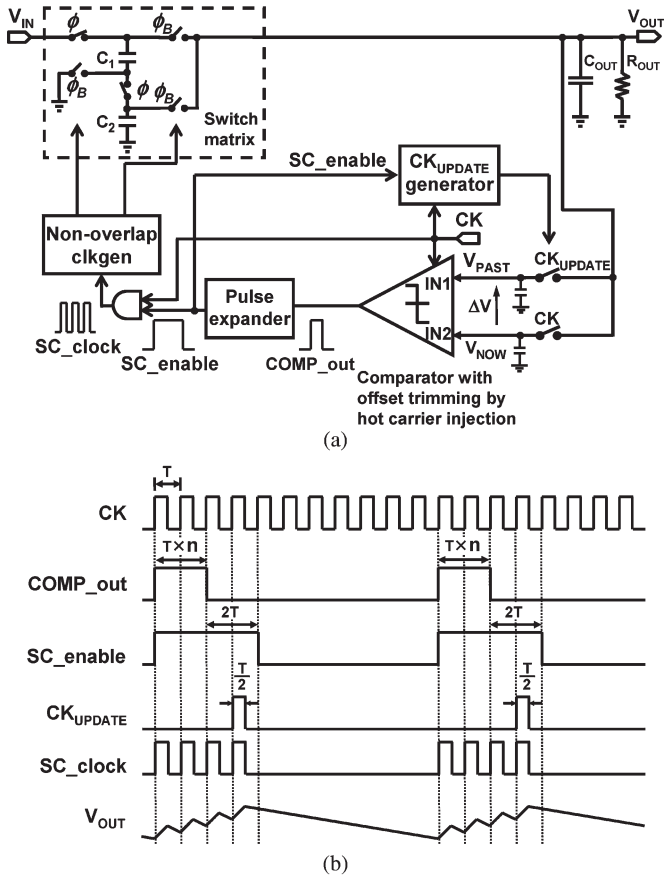

Fig. 3. (a) Block diagram of proposed SC voltage converter with VRF-PDM. (b) Timing diagram.

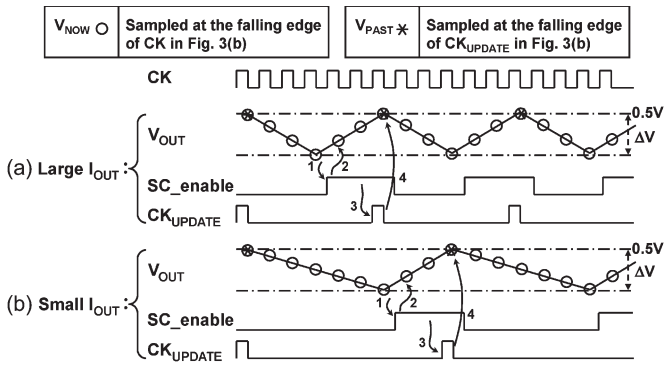

Fig. 4. Operation of proposed SC voltage converter with different $I_{\rm OUT}$.

In order to avoid abnormal $V_{\rm OUT}$ lowering, a periodic activation scheme (PAS) of the SC voltage converter is proposed. The timing diagram of the proposed PAS in VRF-PDM is shown in Fig. 5(b). A 5-bit counter is embedded in PAS; even if COMP_out is always low, SC_enable and $\rm CK_{UPDATE}$ pulses are generated at every 32 clock cycles. Because the SC_enable pulse activates the switch matrix, $V_{\rm OUT}$ is charged up to $V_{\rm IN}/2$. After this, $\rm CK_{UPDATE}$ is generated and $V_{\rm PAST}$ is refreshed to the new $V_{\rm OUT}$. This way, the output voltage will be recharged rather than smoothly lowering to 0 V, preventing the abnormal $V_{\rm OUT}$ lowering problem. Fig. 6 shows the pulse density of VRF-PDM with PAS in comparison with the conventional CPD [see Fig. 2(a)] and PDM [see Fig. 2(b)]. Three dots in Fig. 6 correspond to Figs. 4(a) and (b) and 5(b). The proposed

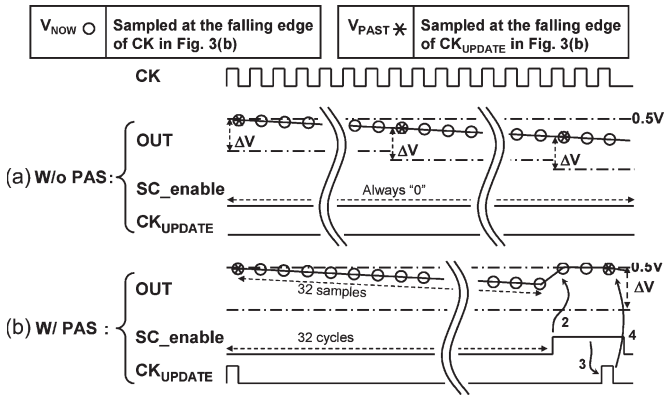

Fig. 5. (a) Abnormal $V_{\rm OUT}$ lowering problem. (b) Proposed PAS to solve the $V_{\rm OUT}$ lowering problem.

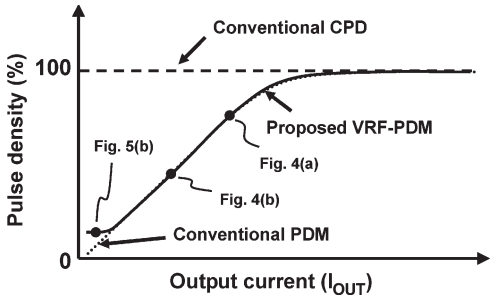

Fig. 6. Analysis of pulse density of conventional and proposed schemes.

VRF-PDM with PAS has the same pulse density with the conventional PDM except for a lower bound at very low $I_{\rm OUT}$.

III. Offset Trimming by Hot-Carrier Injection

In the proposed VRF-PDM converter, $V_{\rm OUT}$ is determined by ΔV because the trigger voltage is set by the offset voltage ΔV of the comparator. In order to enable $V_{\rm OUT}$ tuning and the compensation for the random mismatch of the comparator without fuse trimming, a novel trimming method with a hot-carrier-injected (HCI) comparator is proposed. Fig. 7 shows a schematic of the HCI comparator. A clocked comparator with cross-coupled latches is employed because of its low static power consumption. Transistors (M3–M5) and two NAND gates are added to trim the offset between M1 and M2. Two current paths through input differential pair M1 and M2 are formed by M4 and M5. By applying a large current through M4 or M5, the threshold voltage $V_{\rm TH}$ of M2 or M1 is increased due to HCI, respectively. Fig. 8 shows a flowchart of the trimming with the HCI comparator using a tester, and Table I shows bias conditions for Fig. 8. The goal of the trimming is to make the comparator to flip at IN1 $=$ IN2 $+ \Delta V$. At first, the comparator trip point is checked at IN1 $=$ IN2 $+ \Delta V$. Depending on the comparator output (OUT), $V_{\rm TH}$ of M1 or M2 is increased using HCI by applying a high voltage to 1.2-V 65-nm CMOS transistors. HCI is repeated with a time iteration of 5 s until the comparator output flips, meaning trimming is finished. This way, $V_{\rm OUT}$ trimming is achieved, and the random mismatch of the comparator is compensated without the fuse.

On the other hand, the proposed HCI comparator is also effective in terms of offset canceling. By applying HCI trimming according to the flowchart shown in Fig. 9, ΔV of the comparator can be effectively canceled out. At first, the comparator

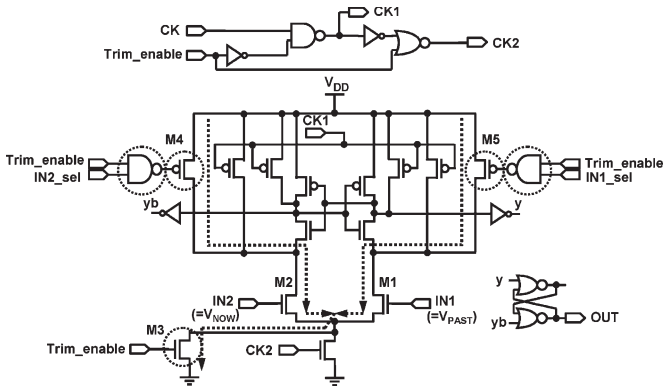

Fig. 7. Comparator with offset trimming by hot-carrier injection.

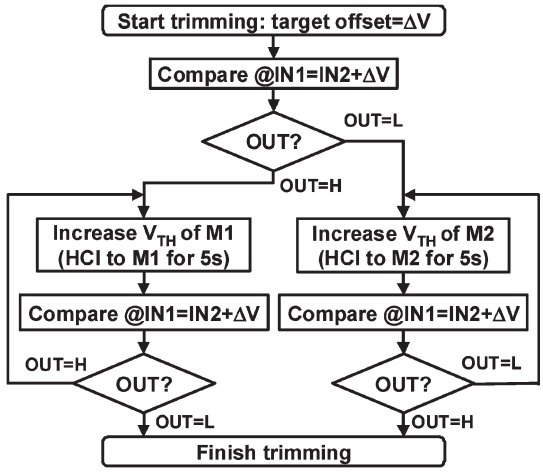

Fig. 8. Flowchart of offset trimming with HCI comparator using a tester.

TABLE I
Bias Conditions for Fig. 8

Mode	Compare @IN1=IN2+ΔV	Increase V_{TH} of M1 (HCI to M1 for 5s)	Increase V_{TH} of M2 (HCI to M2 for 5s)
V_{DD} (V)	1	2.5	2.5
IN1 (V)	0.5 + ΔV	2.5	0
IN2 (V)	0.5	0	2.5
Trim_enable	L	H	H
CK1	⊓⊓	H	H
CK2	⊓⊓	L	L
IN1_sel	X	H	L
IN2_sel	X	L	H

trip point is checked at IN1 $=$ IN2. Depending on the output, $V_{\rm TH}$ of M1 or M2 is increased using HCI repetitively until the comparator output flips, meaning offset canceling is finished.

IV. Measurement Results and Analysis

The proposed VRF-PDM converter is fabricated with a 65-nm CMOS process. Fig. 10 shows the die micrograph. The active area of the proposed voltage converter is 240 μm $\times$ 330 μm. Off-chip capacitors C1 and C2 in Fig. 3(a) of 4.7 nF are used in this design due to limited chip area. For fully integrated implementation in the future, capacitor size should be reduced by increasing the clock frequency. The proposed

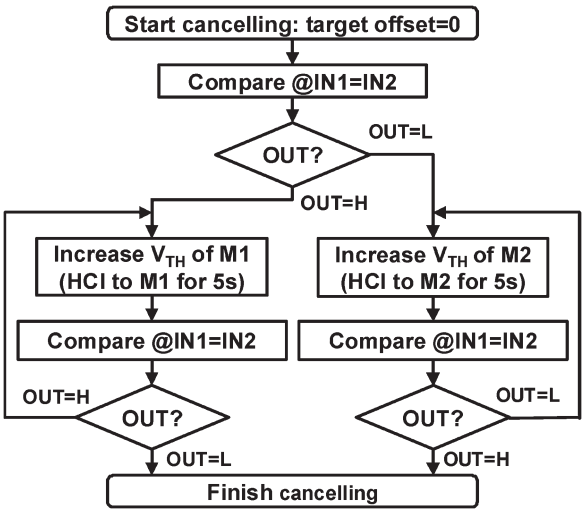

Fig. 9. Flowchart of offset canceling with HCI comparator using a tester.

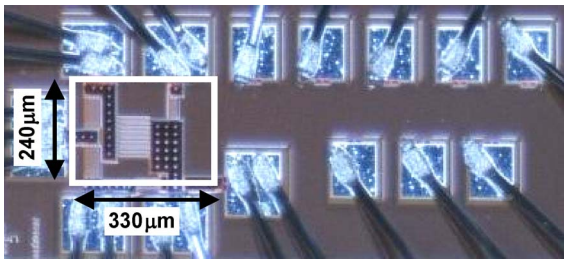

Fig. 10. Chip micrograph.

VRF-PDM can be easily extended to any other switch matrices with no matter on- or off-chip capacitors. Fig. 11(a) shows the measured dependence of the pulse density on the output current of the proposed VRF-PDM converter. The pulse density linearly goes with the output current until the output current reaches 3 mA, which indicates good PDM function. Fig. 11(b) shows the measured output voltage versus the output current. By connecting SC_clock to CK and muting other control blocks for proposed VRF-PDM, the conventional SC voltage converter with CPD is also measured for comparison. Fig. 11(c) shows the measured dependence of the output ripple on the output current compared with the conventional SC voltage converter with CPD. A less-than-3-mV ripple increase is imposed to carry out PDM in the proposed VRF-PDM converter.

Fig. 12 shows the measured waveforms of $V_{\rm OUT}$ and SC_enable at different $I_{\rm OUT}$. Since SC_clock is generated from CK and SC_enable by an AND gate, the duty cycle of SC_enable is exactly equal to the pulse density of SC_clock. By observing the duty cycle of SC_enable, the pulse density of the SC voltage converter is clearly observed. As $I_{\rm OUT}$ decreases, the duty cycle of SC_enable also decreases, which shows the PDM operation and corresponds to Fig. 11(a). A ripple of 14 mV is observed, which shows ΔV of the measured converter.

Fig. 13 shows the measured trimming of the offset voltage of the HCI comparator and the retention characteristics for 6 dies. The 6 dies are trimmed to different target offset voltages of 50, 100, 150, and 200 mV, respectively. Good linearity is observed within the total stress time, indicating good controllability of trimming. The retention after trimming is finished is also measured, and no significant retention is observed. Fig. 14 shows

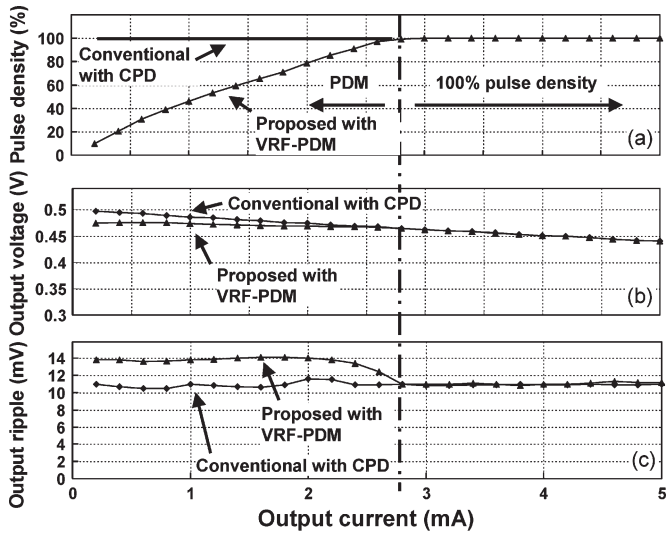

Fig. 11. Measured results of conventional SC converter with CPD and proposed SC converter with VRF-PDM: (a) output voltage; (b) pulse density; and (c) output ripple.

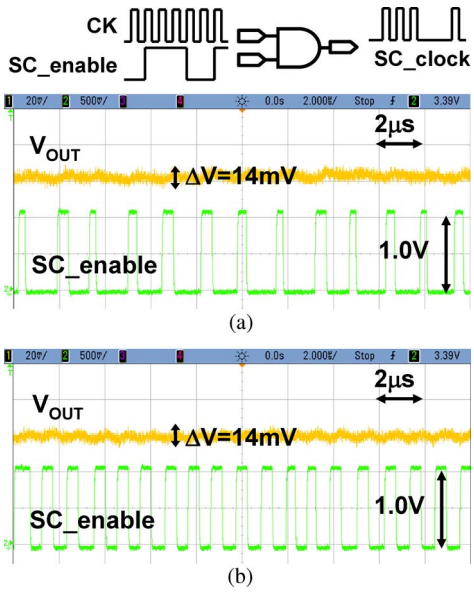

Fig. 12. Measured waveform of $V_{\rm OUT}$ and CK_enable. (a) $I_{\rm OUT} = 0.5$ mA; pulse density $= 26\%$. (b) $I_{\rm OUT} = 1$ mA; pulse density $= 47\%$.

measured offset canceling of the HCI comparator of 10 dies. Before offset canceling, due to random mismatch and within-die variation, comparators have large offset varying from -75 to 90 mV. After offset canceling is finished, the offset voltages of 10 dies are reduced to -3.1 to 3.3 mV. The retention after offset canceling is also measured, and no significant retention is observed. The offset of the comparator due to random mismatch and within-die variation is effectively reduced.

Fig. 15 shows the measured efficiency versus the output current of the proposed and conventional schemes. The efficiency of the conventional SC voltage converter with PDM is calculated based on the measured efficiency of the proposed scheme, with subtraction of the power consumed by state-of-the-art low-voltage and low-power (14-μW) band-gap voltage reference [10]. Severe efficiency degradation is observed on the conventional scheme with CPD at less than 3-mA output

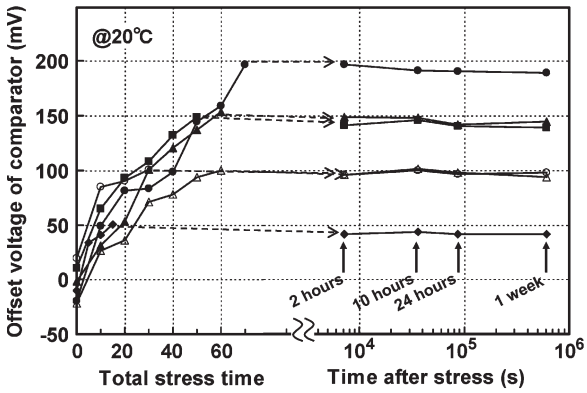

Fig. 13. Measured trimming of offset voltage of HCI comparator (see Fig. 8) and retention characteristics for 6 dies.

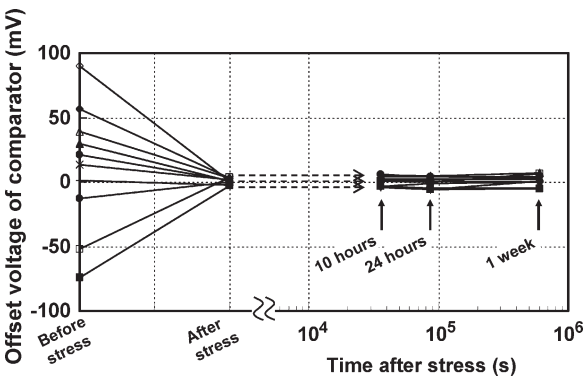

Fig. 14. Measured offset canceling of HCI comparator (see Fig. 9) and retention characteristics for 10 dies.

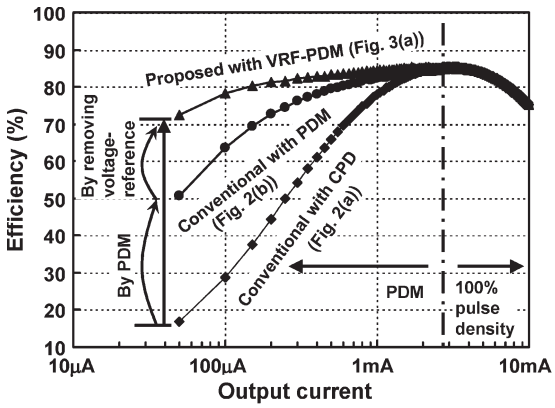

Fig. 15. Efficiency of (1) conventional SC converter with CPD (measured), (2) conventional SC converter with PDM [calculated from (1)], and (3) proposed SC converter with VRF-PDM (measured).

current. In contrast, the proposed VRF-PDM converter achieves above 73% efficiency over the $I_{\rm OUT}$ range from 50 μA to 10 mA, with a peak value of 86% at 3 mA. Compared with the conventional scheme with CPD, an efficiency improvement from 17% to 73% is obtained at 50-μA $I_{\rm OUT}$. The performance summary of the proposed VRF-PDM converter is shown in Table II.

V. Conclusion

In this brief, a VRF-PDM voltage converter with 1-V input and 0.45-V output has been proposed and fabricated in 65-nm CMOS. By virtue of the proposed VRF-PDM, efficiency is significantly increased at low $I_{\rm OUT}$ by reducing the pulse density and eliminating the VREF. A PAS of the voltage converter is proposed to solve the problem of $V_{\rm OUT}$ abnormal lowering to 0 V. A comparator with offset trimming by HCI is also proposed for output voltage trimming. Both offset voltage trimming and offset canceling have been proven effective by measurement with 16 dies. The proposed VRF-PDM voltage converter provides above 73% efficiency over the output current range from 50 μA to 10 mA, with a peak value of 86%. An improvement of efficiency from 17% to 73% is achieved at 50-μA output current.

TABLE II
Performance Summary

Process	65-nm CMOS
Input voltage	1.0V
Output voltage	0.45V
Output current	50μA-10mA
Max. output ripple	14mV
Max. power efficiency	86% at 3mA
Frequency	10MHz
Active area	0.079mm^2

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