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A 315 MHz Power-Gated Ultra Low Power Transceiver in 40 nm CMOS for Wireless Sensor Network

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SUMMARY A 315 MHz power-gated ultra low power transceiver for wireless sensor network is developed in 40 nm CMOS. The developed transceiver features an injection-locked frequency multiplier for carrier generation and a power-gated low noise amplifier with current second-reuse technique for receiver front-end. The injection-locked frequency multiplier implements frequency multiplication by edge-combining and thereby achieves 11 μW power consumption at 315 MHz. The proposed low noise amplifier achieves the lowest power consumption of 8.4 μW with 7.9 dB noise figure and 20.5 dB gain in state-of-the-art designs.

key words: *injection lock, power gating, low noise amplifier, ultra low power*

1. Introduction

An ad hoc wireless sensor network refers to a group of spatially distributed sensors, or nodes, linked by a wireless medium to report on the physical world. To protect safety and security, promote healthcare and welfare, and provide entertainment and convenience, 1000–10,000 sensor nodes are distributed around the user's environment. These sensor nodes are usually powered either by batteries or through energy harvesting and thus each of the nodes should be implemented at a minimal power level.

Figure 1 shows the block diagram of the proposed low-power transceiver for wireless sensor network [1]. To reduce the power consumption, carrier frequency should be as low as possible. Due to the well-known fundamental limits of antenna miniaturization, 315 MHz is chosen for this work and a commercial $\varphi 12 \times 86$ mm antenna is assumed in this work. The transceiver employs on-off keying (OOK) modulation. Typically in a transmitter, a carrier wave is generated by a phase-locked loop which usually consists of a phase-frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator and a frequency divider and therefore consumes a lot of power. To reduce the power consumption, this work employs injection-locked frequency multiplier for carrier generation. As shown in Fig. 1, on the transmitter side, the 39.375 MHz reference frequency is multiplied to 315 MHz by injection locking and then the generated 315 MHz carrier is modulated by input data and amplified by power amplifier for transmission. On the receiver side, the received signal is first amplified by the front-end power-gated low noise amplifier (LNA) where the power gating signal ϕ_{PG} comes from offchip and then the envelope of the signal is detected by the envelope detector. This envelope detection based architecture can eliminate the need for a local oscillator in the receiver and therefore most of the power in the receiver is consumed the front-end low noise amplifier. In this work a power-gated LNA with current second-reuse technique is proposed to minimize the power consumption.

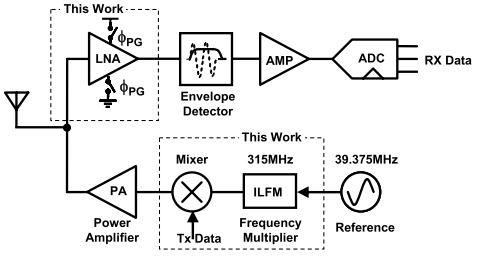

Fig. 1 Proposed injection-locked OOK transmitter and power-gated receiver for wireless sensor network.

This paper is organized as follows. Section 2 describes the power-gated LNA with current second-reuse technique. Section 3 explains the proposed 315 MHz injection-locked frequency multiplier. Experimental results are presented in Sect. 4 and Sect. 5 concludes the paper.

2. Current Second-Reused Amplifier with Power Gating

2.1 Current Second-Reuse Technique

To achieve low noise figure and 50-Ω input match, a large current is required at the first stage of the front-end amplifier. Current reuse technique can halve the current by stacking NMOS and PMOS transistors as amplifying devices [2]. On the left of Fig. 2(a) a NMOS with aspect ratio W_n/L and drain current I is split to two NMOS with aspect ratio $W_n/2L$ and drain current $I/2$. Thus, the transconductance of the compound device with $W_n/2L$ is the same as the transconductance of the device with W_n/L. On the right of Fig. 2(a), one of the $W_n/2L$ NMOS is substituted by a PMOS with drain current $I/2$. By sizing the aspect ratio of the PMOS, its transconductance can be the same as NMOS with $W_n/2L$ and thereby the total voltage gain of the current-reused amplifier with drain current $I/2$ can be the same as a single

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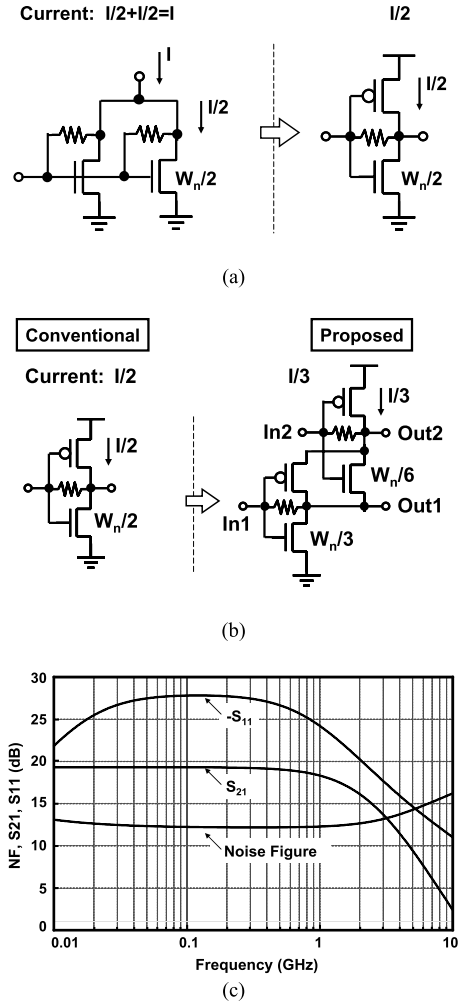


Fig. 2 Shunt-shunt feedback amplifier. (a) Conventional current reused [2]. (b) Proposed current second-reused. (c) Simulated noise figure and S parameter of the proposed current second-reused amplifier.

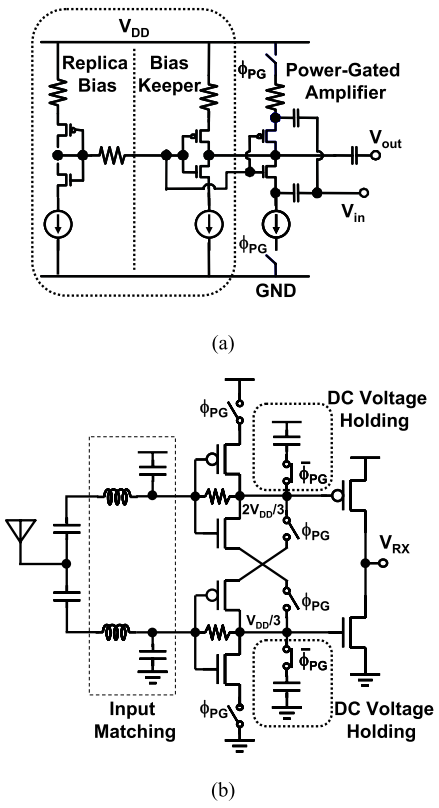


Fig. 3 (a) Conventional power-gated amplifier [4]. (b) Receiver front-end with proposed power-gated LNA. (© 2011 IEEE)

NMOS amplifier with drain current I.

As shown in Fig. 2(b), the drain current can be further reduced to 1/3 by overlapping the NMOS and PMOS pairs. The outputs of the two overlapped MOS pairs can be summed at the second stage. Shunt-shunt feedback can not only prevent amplitude distortion and self-bias at the first stage but also eliminate the bias voltage generator for the second stage. The width of the overlapped transistors in the first stage is half of the top and the bottom transistors so the DC voltages at the overlapped points are $V_{DD}/3$ and $2V_{DD}/3$ respectively which can be used as voltage bias for the second stage.

Without narrowband matching network, the proposed topology can be directly used as wideband amplifier [3]. Figure 2(c) shows the simulated noise figure and S-parameters with 50 Ω input and output impedance of the proposed current second-reused amplifier. The simulated power gain, IIP3 and noise figure are 19 dB, −10 dBm and 12 dB from 200 MHz to 960 MHz while in [3] the power gain, IIP3 and noise figure are 13 dB, −10 dBm and 3.6 dB respectively. Compared with the conventional current-reuse technique, for the same voltage gain the DC current is decreased by 1.5 times and thus the performance deterioration due to process variation is also increased by 1.5 times due to the stacked topology.

2.2 Power Gating Technique

Power gating is an effective low-power design technique which originally stems from logic circuits where a circuit block is cut off from voltage supply when the block is not switching. In [4] power gating is introduced to the design of front-end LNA for pulse receiver. As shown in Fig. 3(a), to keep the additional DC bias point when the amplifier is cut off, a replica of the amplifier, called bias keeper is used. Power consumption of the amplifier is reduced by power gating but the bias keeper is not power-gated and thus the power consumption of the receiver is dominated by the bias keeper.

This bias keeper can be eliminated by two $\bar{\phi}_{PG}$ controlled capacitors in Fig. 3(b). During start-up, the voltage of the two capacitors is charged to $V_{DD}/3$ and $2\,V_{DD}/3$ respectively. When the amplifier is cut off, DC bias voltage is held on the capacitors dynamically. The capacitance for DC voltage holding is 750 fF. The resistors for feedback are implemented by CMOS transmission gates operating in deep triode-region. The proposed LNA achieves low power con-

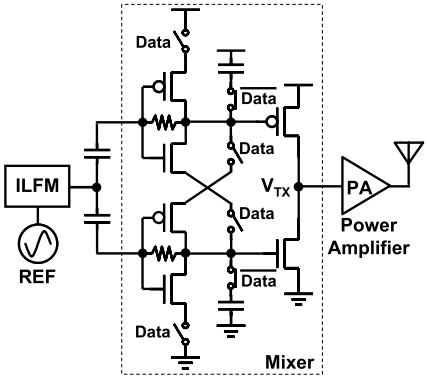


Fig. 4 Proposed fast-settling OOK transmitter. (© 2011 IEEE)

sumption at the cost of doubled impedance matching networks due to the stacked NMOS and PMOS pairs. As shown in Fig. 4, this technique can also be applied to the mixer design to enable fast modulation and thus high energy efficiency.

3. Injection-Locked Frequency Multiplier

3.1 Conventional Injection-Locked Frequency Multiplier

Principle of conventional injection-locked frequency multiplier based on LC oscillator is shown in Fig. 5(a) [5]–[7]. The frequency multiplier consists of an LC tank and a current source clocked at the reference frequency, which injects the LC tank with a stream of current pulses. Assuming that the free running frequency of the oscillator is very close to the *N*th harmonic of the reference, the oscillator will lock to that harmonic such that its average frequency becomes *N* times the reference frequency. These characteristics are similar to the action of an integer-N phase-locked loop frequency synthesizer. However, since no phase detector, loop filter, and frequency divider are required in this system, in principle, an injection-locked frequency multiplier provides a very simple and low power means of achieving frequency multiplication.

Ring oscillator based injection locked frequency multiplier is shown in Fig. 5(b) where an NMOS modulator is inserted between two output nodes of three inverters [8], [9]. When the NMOS turns on, the output nodes in the ring oscillator are connected through the NMOS so the gain of the third inverter decreases and the output amplitude is modulated. As a result, the output waveform is distorted and the spurious tones become large, and thus the locking range is reduced. To reduce waveform distortion and spurious tones, the injected pulse width should be as narrow as possible.

3.2 Proposed Injection-Locked Frequency Multiplier

In practice, there are several challenges in building the frequency multiplier shown in Fig. 5. The first issue is that the free running frequency of the oscillator must be very close to the desired harmonic of the reference in order to

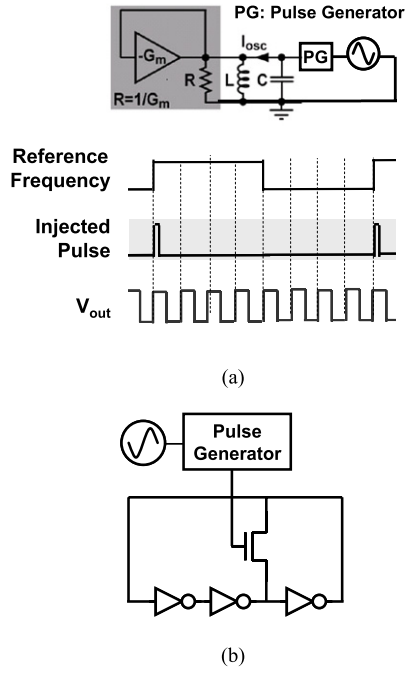


Fig. 5 Conventional Injection-locked frequency multiplier. (a) LC oscillator based [5]–[7]. (b) Ring oscillator based [8], [9].

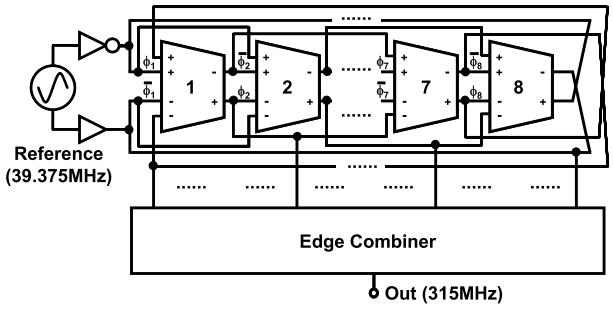
achieve injection-locking. For the LC oscillator based frequency multiplier, locking has been traditionally achieved by first tuning the LC resonant frequency of the oscillator with a varactor such that its value is sufficiently close to the desired harmonic as determined with the aid of a frequency detector [5]–[7]. Without off-line tuning V_{tune}, the locking range of an 8×315 MHz frequency multiplier designed in this way is less than 1 MHz.

The second issue is that the oscillator operates at the multiplied frequency so the power consumption is increased by the same multiplication factor.

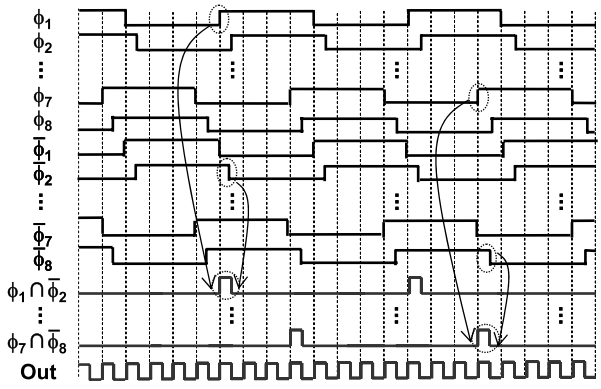
To address these issues, an edge-combing based injection-locked frequency multiplier is proposed in Fig. 6(a). In the proposed frequency multiplier, the 315 MHz output frequency is achieved by combining the 16-phase edges of the eight delay cells. Figure 6(b) shows the timing diagram. Each of the delay cells [10], [11] operates at 39.375 MHz and thus the power is reduced to 1/8 of conventional way without the consideration of the power consumption of the edge combiner. Since the delay-cell frequency is the same as reference frequency, wide locking range can be achieved by full-period forced oscillation instead of narrow-pulse injection-locked oscillation.

4. Measurement Results

The proposed transmitter with injection-locked frequency multiplier and power-gated receiver front-end without inductors were designed and fabricated in 40 nm CMOS process. Chip micrographs and layouts of LNA and frequency multiplier are shown in Fig. 7. By disabling the on-chip capacitors of the LNA, the same chip is used as the mixer for

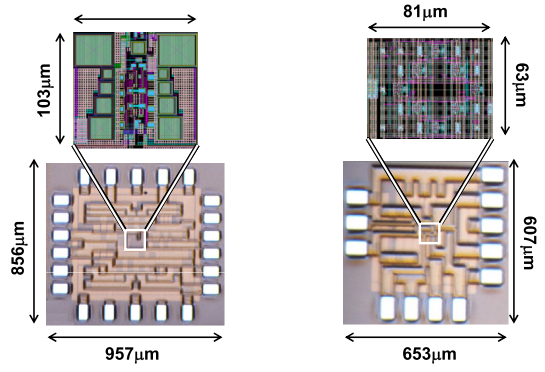


(a)



(b)

Fig. 6 Proposed injection-locked frequency multiplier. (a) Circuit schematic. (b) Timing diagram. (© 2011 IEEE)



(a) LNA. (b) Frequency multiplier

Fig. 7 Chip micrographs and layouts. (a) LNA. (b) Frequency multiplier. (© 2011 IEEE)

measurement. To measure the performance of the transmitter, an evaluation printed circuit board (PCB) is prepared. The chip is bonded to the PCB by bonding-wire machine and the off-chip inductor for impedance matching is welded to the board. The waveforms of the LNA are measured by Agilent DSO91304A infiniium high performance oscilloscope and the noise figure is measured by Agilent ESA series spectrum analyzer.

Figure 8 shows the measured LNA noise figure and

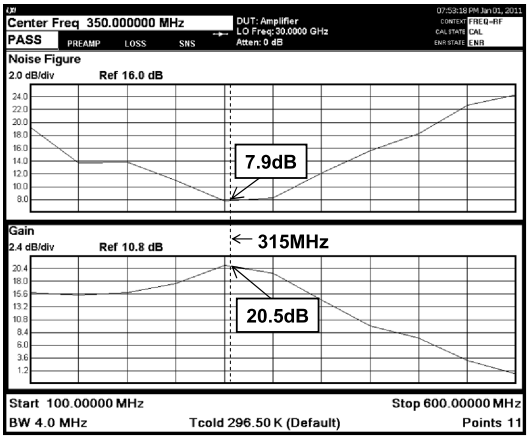


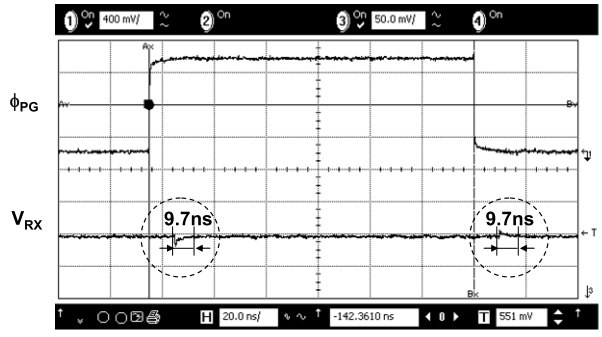
Fig. 8 Measured LNA noise figure and gain. (© 2011 IEEE)

gain. At the target frequency 315 MHz, the noise figure and gain are 7.9 dB and 20.5 dB respectively. Power gating ratio of Fig. 8 is 100% because it takes more than one second for Agilent ESA series spectrum analyzer to calculate the noise figure for each frequency point. To measure the noise figure for 3.12% power gating ratio, the response time of the measurement equipment should be less than 31.2 ns. The measured LNA waveforms for data "0" and data "1" are shown in Fig. 9(a) and Fig. 9(b) respectively. ϕ_{PG} is power gating control signal and V_{RX} is the LNA output. From the measured waveforms for data "0", it can be seen that the settling time of power gating is 9.7 ns which is determined by the time constant of the power-gating node. The time constant is the product of the input capacitance of the second stage and the output resistance of the first stage. This short settling time enables fast power gating in receiver and fast modulation in transmitter. As shown in Fig. 9(b), the data rate is 1 Mb/s and the power-gating duty is 3.12% so the pulse width is only 31.2 ns. The measured transmitter waveforms are shown in Fig. 10. DATA is the modulation input and V_{TX} is the mixer output.

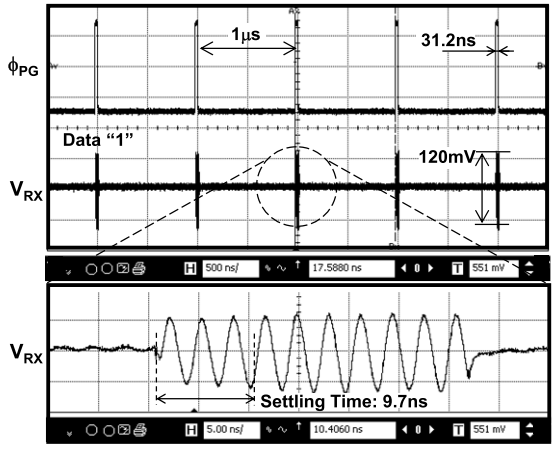
The measured LNA power dependency on duty is shown in Fig. 11. Power consumption is reduced linearly with the power-gating duty and thereby achieves 8.4 μW at 3.12% duty. The minimum detectable power for the oscilloscope is 5 μW.

The frequency multiplier waveforms and spectrum are shown in Fig. 12(a) and Fig. 12(b) respectively. The reference frequency is 39.375 MHz and output frequency is 315 MHz. The measured power consumption at 0.6 V are 11 μW. The measured locking range of the proposed full-period injection-locked frequency multiplier is 5 MHz which is limited by the phase asymmetry due to the single-phase injection. Compared with the conventional pulse injection locked frequency multiplier, the locking range is increased by five times.

Table 1 shows the transmitter performance summary and comparisons with state-of-the-art ultra low power transmitter for wireless sensor network. In this work, the supply voltage for the mixer is 1.2 V while the supply voltage for



(a)



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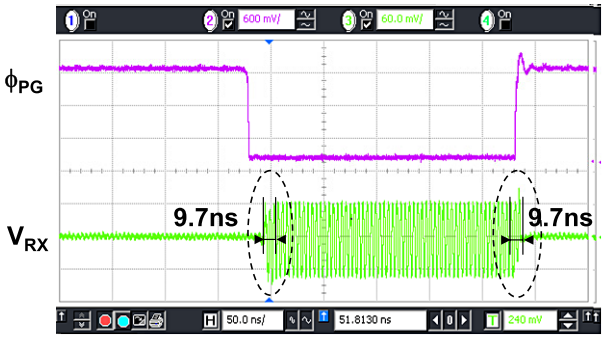


(c)

Fig. 9 Measured LNA waveforms. (a) Data "0". (b) 31.2 ns Data "1". (c) 250 ns Data "1".

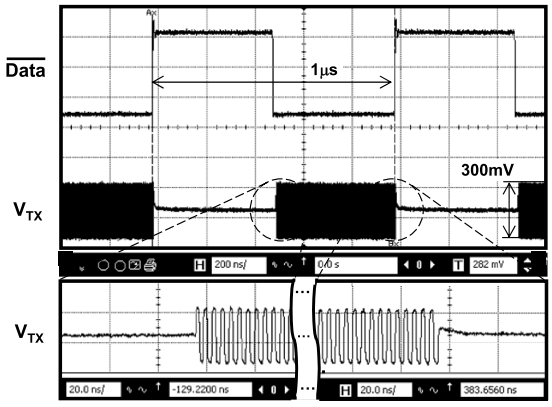


Fig. 10 Measured transmitter waveforms. (© 2011 IEEE)

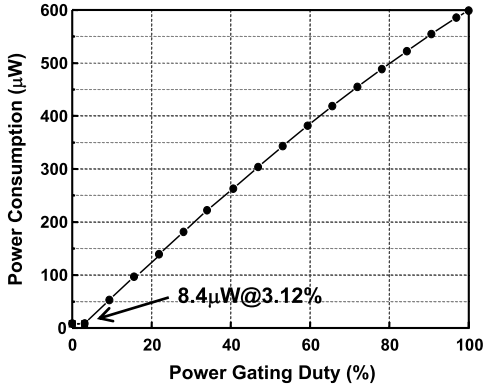


Fig. 11 Measured LNA power dependency on power-gating duty. (© 2011 IEEE)

Table 1 Transmitter performance summary and comparisons.

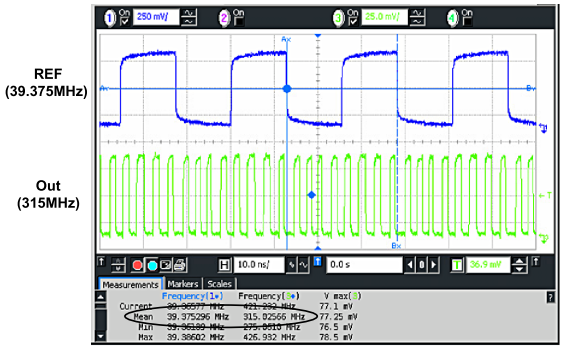
		JSSC'07 [12]	This Work
Technology		0.18μm	40nm
Voltage		1.8V	1.2V
Carrier		916MHz	315MHz
Data Rate		1Mb/s	1~2Mb/s
Modulation		OOK	OOK
Power	Carrier Gen.	0.8mW	11μW @0.6V
	Mixer	2.5mW	320μW
Settling Time		270ns	9.7ns

the injection-locked carrier generator is 0.6 V. Compared to conventional work with 1.8 V supply voltage, the carrier frequency is reduced to 34.4% but power consumption of the carrier generator and the mixer are reduced to 1.38% and 12.8% respectively. The settling time is reduced to 3.59%.

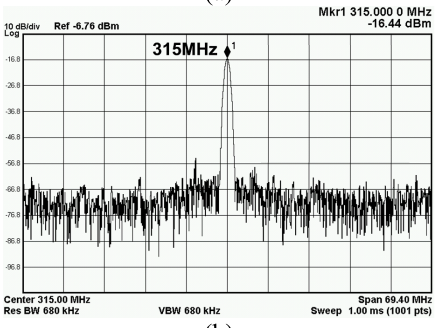
The LNA performance summary and comparisons with state-of-the-art design is shown in Table 2. Without power gating, power consumption of the LNA with the proposed current second-reuse technique is 598 μw. With power gating, power consumption of the LNA can be reduced with power gating duty and thereby achieves the lowest power consumption of 8.4 μW with 7.9 dB noise figure and 20.5 dB gain.

5. Conclusions

This paper presents a 315 MHz injection-locked OOK transmitter and a power-gated receiver front-end for wireless ad hoc network in 40 nm CMOS. To address the issues of power consumption and locking range in the conventional injection-locked frequency multiplier, the proposed frequency multiplier achieves frequency multiplication by edge-combining. It can reduce power consumption to



(a)



(b)

Fig. 12 Measurement results for frequency multiplier. (a) Waveforms. (b) Spectrum. (© 2011 IEEE)

Table 2 LNA performance summary and comparison.

	VLSI'04 [13]	VLSI'09 [14]	VLSI'10 [15]	This Work
Technology (CMOS)	90nm	90nm	65nm	40nm
Supply Voltage	0.6V	2V	0.6V	1.2V
Frequency	5.5GHz	470MHz	900MHz	315MHz
Noise Figure	3.2dB	3.9dB	9.9dB	7.9dB
Gain	11.2dB	26.2dB	32.6dB	20.5dB
Architecture	Differential 1-Stage	Single-Ended 2-Stages	Differential 1-Stage	Single-Ended 2-Stages
Power	2.1mW	10mW	4.8mW	8~598μW

11 μW at 315 MHz and increase the locking range by five times. The proposed power-gated LNA with the current second-reuse technique achieves the lowest power consumption of 8.4 μW with 7.9 dB noise figure and 20.5 dB gain.

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