An All 0.5V, 1Mbps, 315MHz OOK Transceiver with 38-μW Career-Frequency-Free Intermittent Sampling Receiver and 52-μW Class-F Transmitter in 40-nm CMOS

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Abstract

An all 0.5V, 1Mbps, 315MHz OOK transceiver in 40-nm CMOS for body area networks is developed. Both a 38-pJ/bit career-frequency-free intermittent sampling receiver with -55dBm sensitivity and a 52-pJ/bit class-F transmitter with -21dBm output power achieve the lowest energy in the published transceivers for wireless sensor networks.

Introduction

A low power OOK transceiver for short-range wireless sensor networks (e.g. body area networks) is developed in this paper. The target receiver (RX) sensitivity and transmitter (TX) output power is -55dBm and -20dBm, respectively, assuming -25dB propagation loss at the 1-m communication distance and -5dB x 2 loss at TX/RX antennas. The target power consumption is 50μW at 1Mbps. In order to reduce the power, (1) sampling circuits are used instead of continuous analog circuits, (2) the power supply voltage (V_{DD}) is reduced to 0.5V, (3) the RX input is directly sampled without LNA, because high sensitivity is not required for the 1-m communication, (4) low career frequency of 315MHz instead of 2.4GHz is used to reduce the required bandwidth of the sampler, (5) a career-frequency-free (CFF) intermittent sampling (IS) is newly proposed to reduce the number of sampling, thereby reducing the power of the sampler to 1/315 of that of the conventional continuous sampling.

Career-Frequency-Free Intermittent Sampling Receiver

A conventional continuous sampling [1-2] and the proposed IS concept for RX are compared in Fig. 1. The proposed IS reduces the number of the sampling in 1 symbol in order to reduce the power consumption of the sampler. Fig. 2 shows a block diagram of the proposed all 0.5V CFF IS RX. Only 1-MHz clock instead of a 315-MHz career frequency is supplied to RX. RX input (V_{IN}) is directly sampled by intermittent samplers without LNA. Fig. 3 shows a schematic of the intermittent sampler. Fig. 4 shows a timing chart of CFF IS RX. V_{IN} is sampled by quadrature 315-MHz clocks (ϕ_0, ϕ_{90}, ϕ_{180}, and ϕ_{270}). The timing difference of ΔT is generated by digitally controlled delay lines instead of a conventional quadrature 315-MHz PLL, thereby reducing the power consumption. In the 315-MHz, 1-Mbps CFF IS RX, the number of sampling of V_{IN} per bit is 4, while that of the conventional continuous sampling is 4x315, thereby reducing the power consumption of the sampler to 1/315. By the clock of ϕ_{HPF}, the sampled V_{IN}'s are subtracted for a high pass filter function in order to increase the RX sensitivity by 3dB [3]. The outputs of the samplers (V_1 , $\overline{V_1}$, V_2 , and $\overline{V_2}$) are amplified by 5-stage IF amplifiers with an offset cancellation [4]. Then, the outputs of the amplifiers (V_{2A}) are compared by proposed variable offset comparators clocked by ϕ_{CMP}, and the data is demodulated. V_{2A} is not constant, because the DC component is eliminated in the offset cancel amplifier [4]. In CFF IS RX, the degradation of RX sensitivity due to ΔT variations is a design concern. In order to clarify the effect of ΔT variations on the RX sensitivity, Fig. 5 shows a calculated dependence of maximum amplitude of V_1 or V_2 on ΔT. In the ideal case of ΔT=T/4=0.8ns, the amplitude is 1. The amplitude, however, is reduced to $1/\sqrt{2}$ =0.7, when the sampling phase is changed. In CFF IS RX, the RX sensitivity is determined by the worst case (=minimum) amplitude, because the phase is not synchronized. The worst case amplitude depends on ΔT. For example, at ΔT=T/2=1.6ns, the worst case amplitude is 0, which is unacceptable. In order to suppress the amplitude degradation within 10% and 50%, the ΔT variation should be less than ± 11% and ± 41%, respectively. In this design, ΔT variation is controlled within ± 41% by the digitally controlled delay lines.

Building Blocks

In CFF IS RX, instead of a variable gain amplifier, the clocked variable offset comparator is used to keep the received signal amplitude constant with low power consumption. The variable offset comparator eliminates the need for a voltage reference circuit, which is very important, because the voltage reference circuit operating at 0.5V is difficult to implement. Fig. 6 shows a schematic of the digitally variable offset comparator. The comparator has 2 sets (C_{LEFT} and C_{RIGHT}) of 63 switched capacitors controlled by 6 bits to change the offset voltage. The offset of the comparator itself can also be compensated by the digital control.

The design challenge of TX is to increase the efficiency at the target low output power of -20dBm and 0.5V, because the efficiency of a power amplifier (PA) decreases with reducing output power and V_{DD}. A class-F PA instead of a class-D or class-E PA is used in this work, because the class-F PA achieved the highest efficiency at the target specification. Fig. 7 shows a schematic of a class-F transmitter. All inductors and capacitors are implemented in off-chip.

Experimental Results

The proposed transceiver is fabricated in 40-nm CMOS process. Fig. 8 shows a die photo and layout of RX and TX. Table I shows a performance summary. Thanks to the proposed IS, the power consumption of the samplers in RX is 3μW and the total RX consumes 38 μW. Without IS, the continuous sampler will consume 945μW (=3μW x 315). Therefore, the proposed IS is a key technology to reduce the RX power consumption. Fig. 9 shows a measured dependence of the offset voltage on the number of connected capacitors in C_{RIGHT} in the proposed digitally variable offset comparator. C_{LEFT} is fixed. The horizontal axis corresponds to the 6-bit digital control. The measured tuning range of the offset is 65mV. Fig. 10 shows measured waveforms of CFF IS RX. 1-Mbps data is successfully demodulated. Fig. 11 shows a measured dependence of BER on RX input signal power. At BER of 10^{-3}, the RX sensitivity is -55dBm. Fig. 12 shows a measured TX output spectrum. The TX output power is -21dBm at 315MHz. The TX efficiency is 16%. Fig. 13 shows a comparison of power and data rate with published transceivers [4-8] for wireless sensor networks. Both the 38-pJ/bit CFF IS RX and the 52-pJ/bit class-F TX achieve the lowest energy to date.

Acknowledgment

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References

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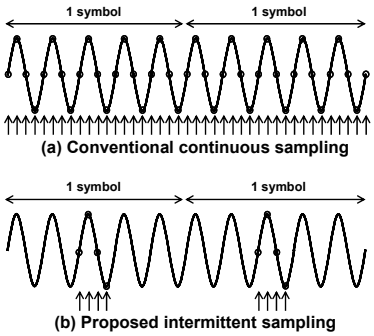

Fig. 1. Proposed intermittent sampling (IS) concept.

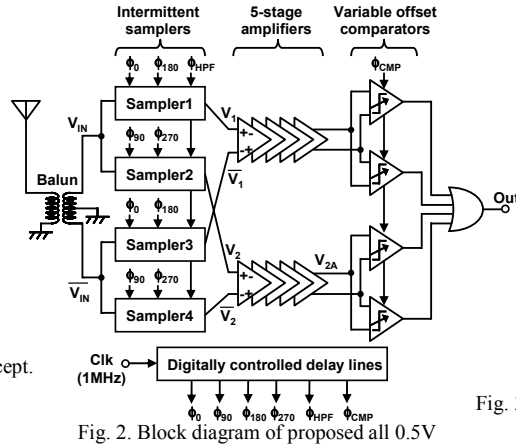

Fig. 2. Block diagram of proposed all 0.5V career-frequency-free (CFF) IS RX.

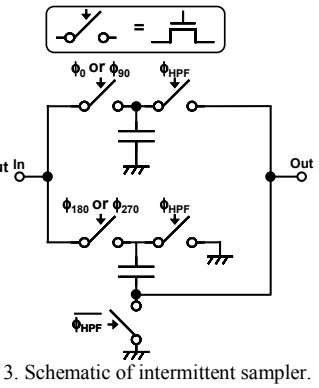

Fig. 3. Schematic of intermittent sampler.

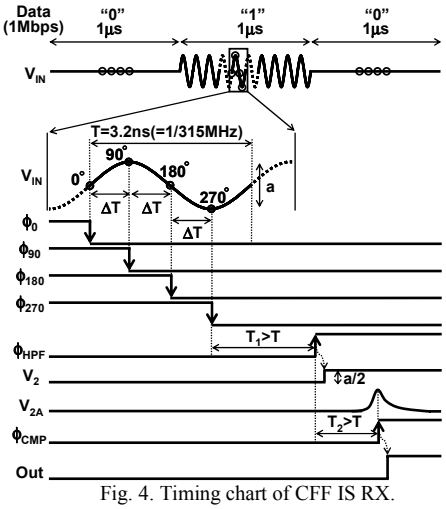

Fig. 4. Timing chart of CFF IS RX.

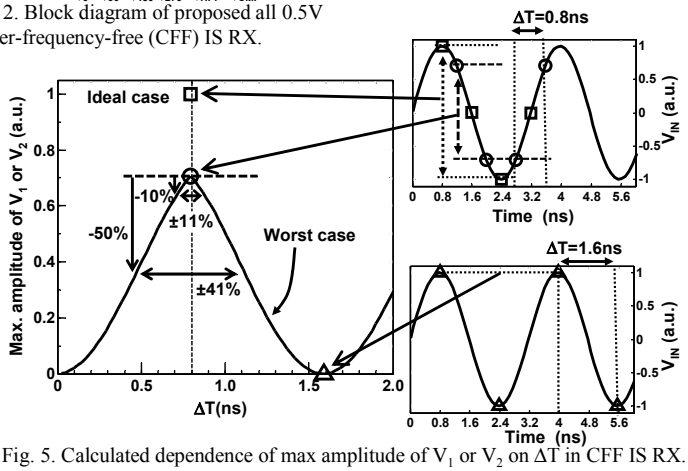

Fig. 5. Calculated dependence of max amplitude of V_1 or V_2 on ΔT in CFF IS RX.

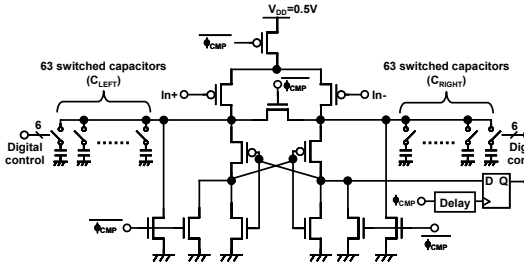

Fig. 6. Schematic of digitally variable offset comparator.

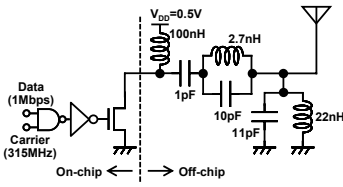

Fig. 7. Schematic of 0.5V class-F TX.

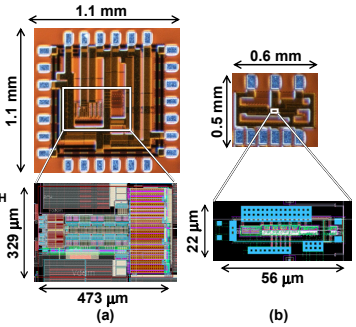

Fig. 8. Die photo and layout of (a) RX and (b) TX.

Table I Performance summary.

CMOS			40nm
Supply voltage			0.5V
Carrier frequency			315MHz
Data rate			1Mbps
Clock frequency		RX	1MHz
		TX	315MHz
Modulation			OOK
RX sensitivity			-55dBm
TX output power			-21dBm
Power	RX	Sampler	3μW
		Amplifier	30μW
		Comparator	2μW
		Delay lines	3μW
		Total	38μW
	TX	Total	52μW
Energy		RX	38pJ/bit
		TX	52pJ/bit
Core area		RX	156000μm²
		TX	1230μm²

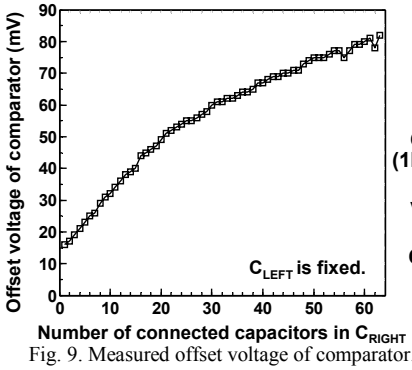

Fig. 9. Measured offset voltage of comparator.

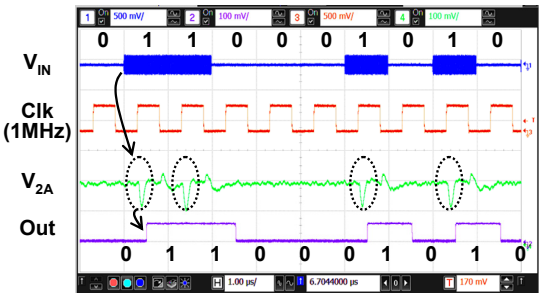

Fig. 10. Measured waveforms of CFF IS RX.

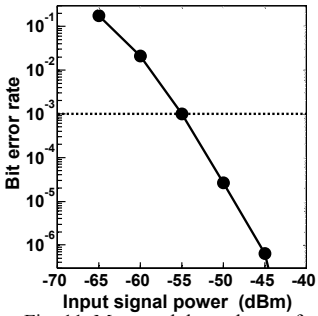

Fig. 11. Measured dependence of BER on RX input signal power.

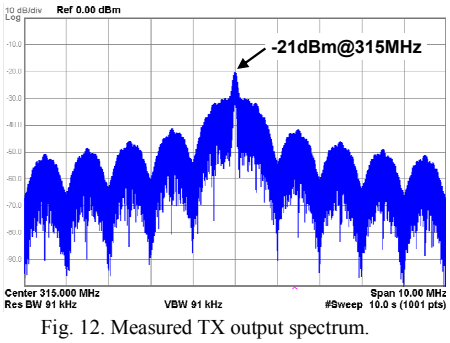

Fig. 12. Measured TX output spectrum.

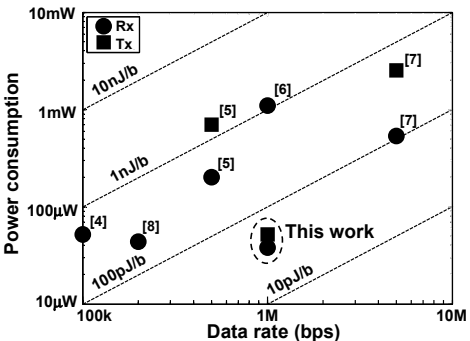

Fig. 13. Comparison with published transceivers for wireless sensor networks.