# A 120-mV Input, Fully Integrated Dual-Mode Charge Pump in 65-nm CMOS for Thermoelectric Energy Harvester

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***Abstract* - In this paper, a fully integrated low voltage charge pump for thermoelectric energy harvesters is presented. The proposed dual-mode architecture achieves both the low startup voltage in a startup mode and high conversion efficiency in a normal operation mode without off-chip inductors and capacitors. In the measurement, the proposed circuit successfully converts 120-mV input to 770-mV output with 38.8% conversion efficiency.**

## I Introduction

The power management circuit applying thermoelectric generators (TEG) for battery-free body-wearable applications is a focus of this paper. The output voltage of TEG is usually on the order of tens to hundreds of mV and is too low to power the electronic devices. To up-covert the harvested energy to useable output, a low input voltage DC-DC converter is required.

The key technique of such a DC-DC converter is the startup mechanism, which kicks-start the system from low input voltage. The previous works uses the boost converter with additional startup mechanism such as mechanical switch [1] or charge pump [2] to kick start the system. The boost converter requires large inductor and startup mechanism. Therefore, area overhead is a problem.

To solve this problem, the ultra low voltage, fully integrated charge pump is proposed. The novel dual-mode architecture achieves both low startup voltage and high efficiency without off-chip inductors and capacitors.

## II System Architecture of Dual-Mode Charge Pump

The main challenges of the low input voltage charge pump are low conversion efficiency and small output current. The low conversion efficiency is caused by high threshold voltage of CMOS transistor (300-500mV). Operating under low supply voltage makes the on-resistance of transistors increases and decreases conversion efficiency. The small output current is caused by low switching frequency. The low supply voltage limits operation frequency. Since the available output current of the charge pump is proportional to the switching frequency, the low operation voltage limits the available output power. Therefore, we proposed novel dual-mode architecture to overcome these problems.

Fig. 1 shows the block diagram of the proposed dual-mode charge pump. It includes the startup oscillator, the operation oscillator, drivers, $\phi$ selector (for gate switch), CK selector (for pumping switch) and the proposed 10-stage dual-mode charge pump. The operation sequences of the proposed dual-mode charge pump are illustrating in Fig. 2. At the startup

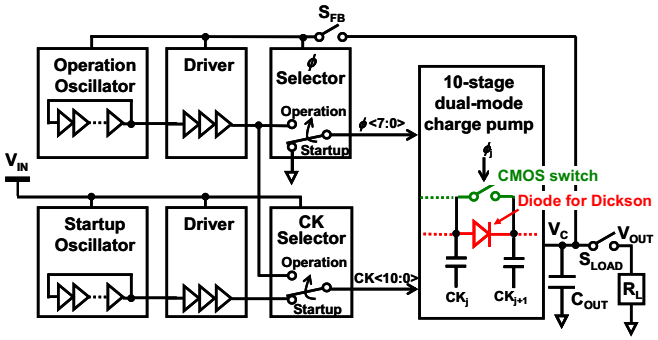


Fig.1 Block diagram of proposed dual-mode charge pump.

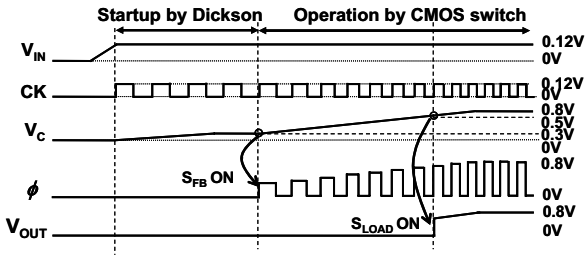


Fig.2. Operation sequences of proposed dual-mode charge pump.

mode, the input voltage $V_{IN}$ directly powers the startup oscillator and drives the charge pump with 120mV clock amplitude through CK selector. The output capacitor $C_{OUT}$ is charged by charge pump and $V_C$ rises. As $V_C$ is charged to the preset voltage (~0.3V), the switch $S_{FB}$ turns on and the charge stored in $C_{OUT}$ activates the operation oscillator. The $\phi$ selector and CK selector selects the signal from operation oscillator and provided to the charge pump. The clock frequency and clock amplitude in operation oscillator is higher than that of startup oscillator (Startup: ~1MHz/120mV, Operation: ~20MHz/770mV). Therefore, the $C_{OUT}$ can be charged to the higher voltage with high conversion efficiency. When $V_C$ is higher than 0.5V, the switch $S_{LOAD}$ turns on and output voltage is obtained. The switch $S_{FB}$ and $S_{LOAD}$ can be implemented by using the voltage detector in [2].

## III Implementation of Dual-Mode Charge Pump

The proposed dual-mode 10-stage charge pump combines the 5-stage Dickson charge pump and 10-stage CMOS charge pump. The simplified schematic and operation sequence is shown in Fig. 3. $M_1$ and $M_2$ forms Dickson charge pump and are used to charge $C_{OUT}$ at startup as shown in Fig. 3(a). At operation mode, the CMOS switches (M3-M6) are driven with high amplitude clock and on-resistance decreases as shown in

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Fig. 3(b). The first half stages of the CMOS charge pump is constructed from the NMOS transistors ($M_3$, $M_4$) and the back half stages are constructed from PMOS transistors ($M_5$, $M_6$). This scheme ensures the maximum overdrive voltage can be provided to each transistor when gate is driven by high-voltage clocks ($\phi$). The transistors $M_1$ and $M_2$ are still functional but most of the current flows through the CMOS switch ($M_3$, $M_4$) because the on-resistance is much smaller than that of diode connected MOSFETs ($M_1$, $M_2$). As a result, the CMOS charge pump improves the conversion efficiency while Dickson charge pump achieves low voltage startup.

## IV. Measurement Results

The proposed circuit was designed and fabricated in 65nm CMOS process. Fig. 4 shows the chip micrograph with active area of 0.78mm$^2$. Each pumping capacitor is 28.6pF and MIM capacitor is used.

The measured dependence of the output voltage and conversion efficiency on output power is shown in Fig. 5. The proposed charge pump successfully converts a 120mV input to 770mV output with the conversion efficiency of 38.8%. Table I compares the performance of fully-integrated charge pumps. Ref [3] and [4] achieve high conversion efficiency but the operation voltage is high. On the other hand, [5] achieves low voltage operation but the conversion efficiency is low. The proposed charge pump achieved the lowest operation voltage with moderate conversion efficiency.

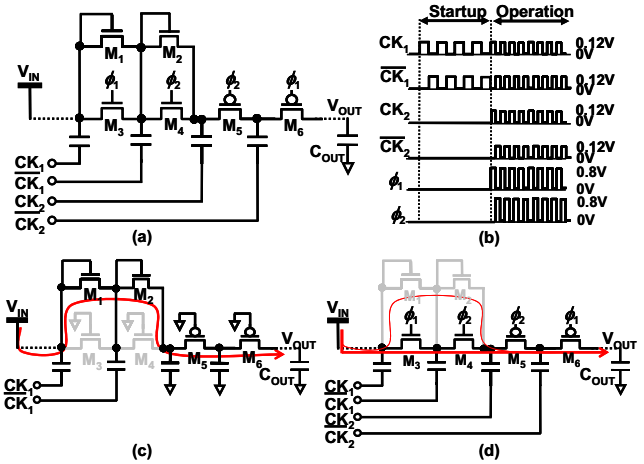


Fig.3. (a) Simplified circuit schematic and (b) operation sequences of the proposed dual-mode charge pump. (c) Startup mode and (d) Operation mode.

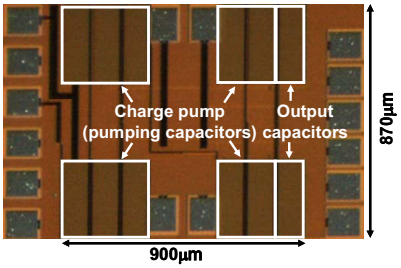


Fig.4. Chip micrograph of proposed dual-mode charge pump.

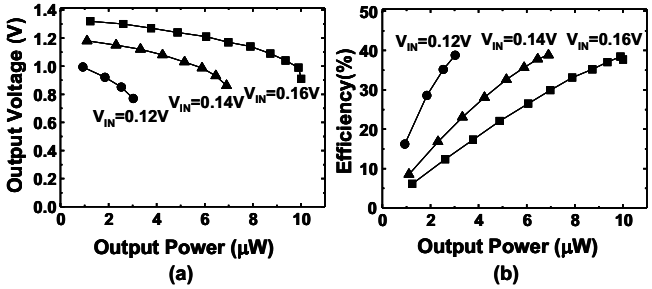


Fig.5. Measured dependence of (a) output voltage and (b) conversion efficiency on output power.

TABLE I
Performance comparison of fully integrated charge pump

| Ref. | ISSCC'07 [3] | ISSCC'09 [4] | CICC'10 [5] | This work |
|---|---|---|---|---|
| CMOS Process | 350nm | 350nm | 65nm | 65nm |
| $V_{IN}$ (min) | 1V | 0.6V | 0.18V | 0.12V |
| Efficiency | 50% | 70% | N/A | 38.8% |
| External excitation | No | Yes (2V battery) | No | No (Dual-mode) |

## V. Conclusion

We have demonstrated a 120-mV fully-integrated charge pump using novel dual-mode architecture. The dual-mode architecture achieves both low startup voltage and high conversion efficiency at the same time without using additional inductor/capacitor. It converts 120mV input to 770mV output with 38.8% conversion efficiency. To the best of our knowledge, it is the lowest operation voltage in CMOS charge pump circuit.

## Acknowledgments

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