

Increase of Crosstalk Noise Due to Imbalanced Threshold Voltage between NMOS and PMOS in Sub-Threshold Logic Circuits

Hiroshi Fuketa¹, Ryo Takahashi¹, Makoto Takamiya¹, Masahiro Nomura², Hirofumi Shinohara², Takayasu Sakurai¹

¹ University of Tokyo, Japan

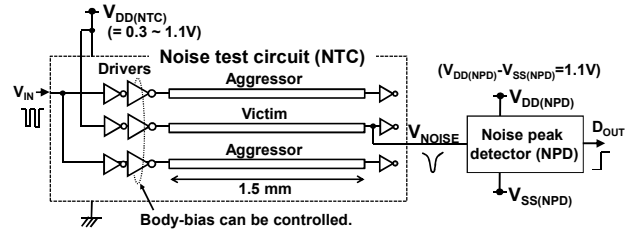
² Semiconductor Technology Academic Research Center (STARC), Japan

Abstract- Abnormal increase of the crosstalk noise in the sub-threshold logic circuits is found for the first time. When the threshold voltages (V_{TH}) of nMOS and pMOS are imbalanced and the on-resistance of the aggressor driver is much lower than that of the victim driver, the large crosstalk noise is observed, because the on-resistance has an exponential dependence on V_{TH} in the sub-threshold circuits. In this paper, the large crosstalk noise due to the imbalanced V_{TH} is measured. A new crosstalk noise model is also proposed and verified with SPICE simulations. In a crosstalk noise test chip with 1.5-mm wire in a 40-nm CMOS at the power supply voltage (V_{DD}) of 0.3V, the measured noise amplitude increases from 32% of V_{DD} to 71% of V_{DD} , when the imbalanced V_{TH} is realized by tuning a body bias in pMOS. In the worst case fast-nMOS/slow-pMOS corner simulations, the noise amplitude increases from 47% of V_{DD} to 68% of V_{DD} , when V_{DD} is reduced from 1.1V to 0.3V, which is explained by the proposed model.

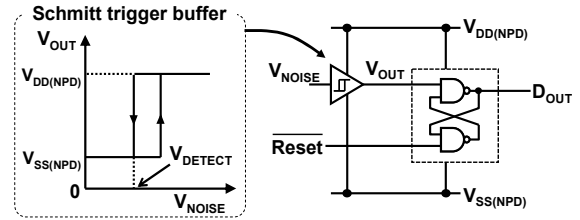
I. INTRODUCTION

Sub-threshold circuits, which operate at a lower supply voltage (V_{DD}) than threshold voltage (V_{TH}), are one of promising solutions to achieve ultra-low power operation [1]. Delay of sub-threshold circuits, however, has large variations due to V_{TH} variation, since the transistor current in the sub-threshold region has an exponential dependence on V_{TH} . Therefore, many researchers have focused on investigating circuit techniques to cope with such large delay variation [2,3]. In contrast, there are few reports on a crosstalk noise in sub-threshold circuits [4], though a lot of paper is published on the crosstalk noise in above-threshold circuits [5-7]. In these previous works, the dependence of the crosstalk noise on V_{DD} is not clear. If the crosstalk noise in sub-threshold circuits is larger than that of the crosstalk noise in above-threshold circuits, a new sign-off condition for the crosstalk check should be developed. Therefore, in this paper, the crosstalk noise in sub-threshold circuits is measured in a 40-nm CMOS test chip. In addition, a new crosstalk noise model is proposed and verified with SPICE simulations. An abnormal increase of the crosstalk noise in the sub-threshold operation is found for the first time.

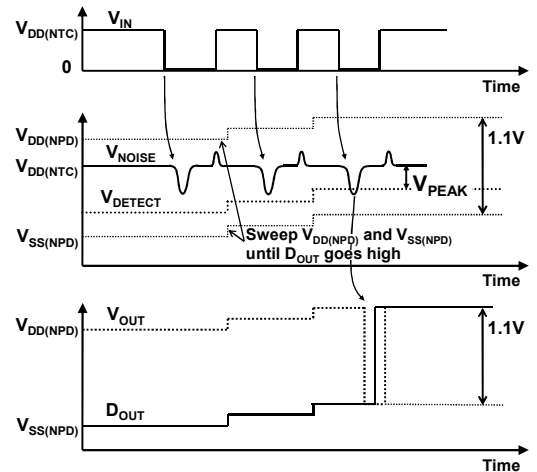
This paper is organized as follows. Section II describes silicon measurements of the crosstalk noise and shows its dependence on the balance of V_{TH} . In order to investigate the dependence, a new crosstalk noise model for sub-threshold circuits is proposed in Section III. Finally, Section IV concludes this paper.



(a) Circuit diagram of crosstalk noise measurement circuit.



(b) Schematic of noise peak detector (NPD) for falling noise.



(c) Timing chart of peak noise detection.

Fig. 1. Measurement circuit and mechanism to detect peak voltage of falling crosstalk noise. Rising noise can be also measured by the similar mechanism.

II. MEASUREMENT OF CROSSTALK NOISE

A. Test Chip Design

In order to measure the dependence of the crosstalk noise on V_{DD} and V_{TH} 's of nMOS and pMOS, a crosstalk noise test chip is designed and fabricated in a 40-nm CMOS. Fig. 1(a) shows a circuit diagram to measure the peak noise voltage

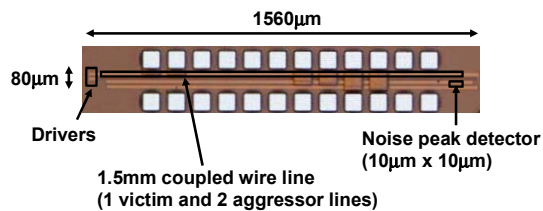


Fig. 2. Chip micrograph in 40-nm CMOS.

induced by crosstalk. The measurement circuit consists of noise test circuit (NTC), which includes 1.5mm coupled wire lines, and noise peak detector (NPD). The long (1.5mm) wire is used in the measurement, because the resistance of the wire is much smaller than that of the driver in the sub-threshold region and hence a lot of repeaters are not required. The crosstalk noise is measured over a wide range of the supply voltage of the NTC ($V_{DD(NTC)}$). In addition, body-bias voltage of the wire line drivers can be controlled in order to investigate the dependence of the balance of V_{TH} between nMOS and pMOS on the crosstalk noise.

Fig. 1(b) shows a schematic of the NPD, which detects the peak voltage of crosstalk noise induced by the falling transition on the aggressor lines. The Schmitt trigger buffer converts a noise that exceeds the logical threshold voltage of the buffer (V_{DETECT}) to a pulse, and then the pulse is captured by the RS latch. The Schmitt trigger buffer is used to make the pulse wider. The voltage difference between the supply voltage ($V_{DD(NPD)}$) and the ground ($V_{SS(NPD)}$) of the NPD is fixed to 1.1V regardless of $V_{DD(NTC)}$. V_{DETECT} is varied by changing both $V_{DD(NPD)}$ and $V_{SS(NPD)}$. As shown in Fig. 1(c), the falling noise peak voltage (V_{PEAK}) is measured by the following procedure:

1. $V_{DD(NPD)}$ and $V_{SS(NPD)}$ are set to low voltages.
2. A falling transition signal is given to the aggressor lines, while the victim line is kept high.
3. If the output of the latch (D_{OUT}) goes high, $V_{DD(NTC)} - V_{DETECT}$ is the peak noise voltage (V_{PEAK}). On the other hand, if D_{OUT} remains low, $V_{DD(NPD)}$ and $V_{SS(NPD)}$ are increased to raise V_{DETECT} . Then, steps 2 and 3 are repeated until the noise is detected.

In order to measure V_{PEAK} , the calibration of V_{DETECT} is required, because V_{DETECT} has die-to-die variations. During the calibration, the crosstalk noise is not generated and $V_{PEAK} = 0V$. Therefore, the exact value of V_{DETECT} is measured by sweeping both $V_{DD(NPD)}$ and $V_{SS(NPD)}$, because V_{DETECT} is equal to $V_{DD(NTC)}$ at the rising edge of D_{OUT} .

The noises occurring in the sub-threshold region are slow, and hence they can be easily measured with the noise peak detector. However, it is difficult for the noise peak detector to accurately measure the peak voltages of fast and sharp noises which often occur at around nominal supply voltage region. The relative error is estimated to be 10% at more than 0.8V.

It should be noted that the rising crosstalk noise can be measured by the similar mechanism (NOR RS latch is used instead of NAND RS latch in Fig. 1(b)). We also implemented

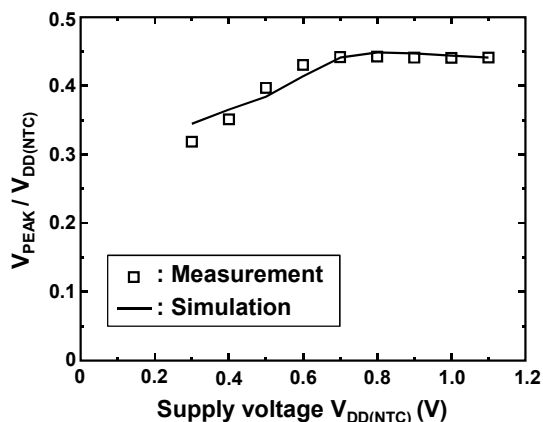


Fig. 3. Measured and simulated peak voltage (V_{PEAK}) of the falling crosstalk noise as a function of the supply voltage of the NTC ($V_{DD(NTC)}$).

the measurement circuit for the rising crosstalk noise and verified its functionality on silicon.

The chip micrograph is shown in Fig. 2. The measurement circuit was fabricated in a 40-nm CMOS process with 7 metal layers. M6 is used for the 1.5mm coupled wire lines.

B. Measurement Results

Fig. 3 shows the measured and simulated peak voltage of the falling crosstalk noise as a function of the supply voltage. The SPICE simulations are conducted with the parasitic wire resistance and capacitance extracted from the layout data. V_{TH} used in the simulations is based on the measured single transistors provided by the foundry. The simulation results agree with the measurement results. Fig. 3 shows that $V_{PEAK} / V_{DD(NTC)}$ decreases as $V_{DD(NTC)}$ is reduced. The details of this dependence will be discussed in Section III.

In order to examine how the balance of V_{TH} between nMOS and pMOS affects the peak noise voltage, the dependence of the peak noise voltage on the body-bias voltage of the victim driver is measured. The measurement results are illustrated in Fig. 4. The peak noise voltage at the nominal supply voltage of 1.1V does not depend on the n-well body-bias voltage of the victim driver, whereas the reverse body-bias voltage significantly increases the peak noise voltage at $V_{DD(NTC)}$ of 0.3V. The noise amplitude increases from 32% of V_{DD} to 71% of V_{DD} , when the imbalanced V_{TH} is realized by tuning a body bias in pMOS. This indicates that the peak noise voltage is extremely sensitive to the balance of V_{TH} between nMOS and pMOS in sub-threshold circuits. The reason why the balance of V_{TH} significantly affects the peak noise voltage is discussed in the next section.

III. MODELING OF CROSSTALK NOISE IN SUB-THRESHOLD REGION

At first, the crosstalk noise by one aggressor line is investigated. Fig. 5 illustrates the equivalent circuit of the coupled wire lines with one aggressor and one victim for the falling noise. In this paper, R_{5N} (R_{5P}) and R_{3N} (R_{3P}) are equivalent resistances of nMOS (pMOS), and the definition

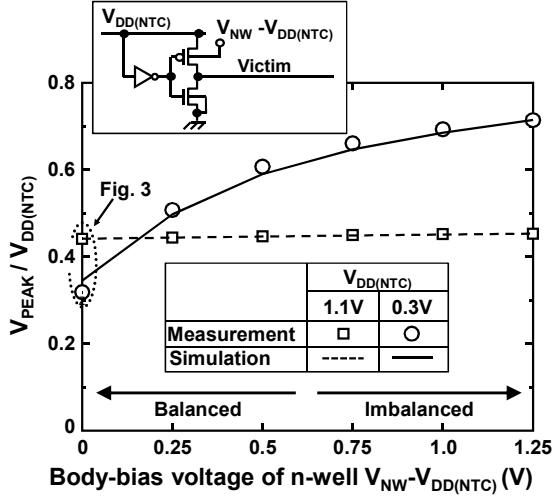


Fig. 4. Measured and simulated dependence of the peak noise voltage (V_{PEAK}) on the n-well body-bias voltage of the victim driver. The noise peak voltage is significantly sensitive to the balance of V_{TH} in sub-threshold circuits.

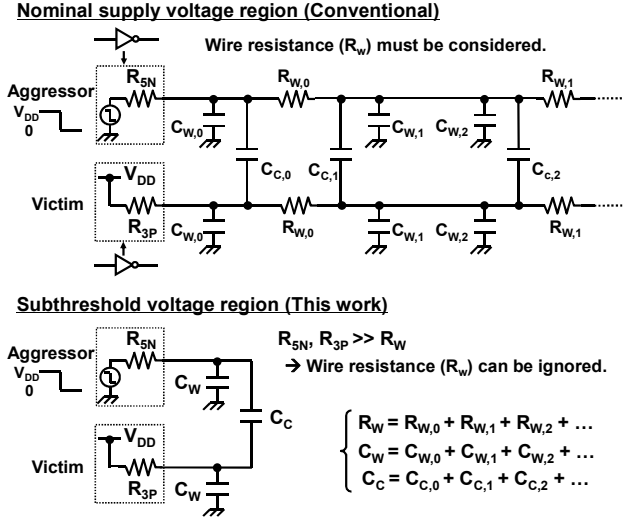


Fig. 5. Equivalent circuit of the coupled wire lines with one aggressor and one victim.

for nMOS is explained in Fig. 6. R_{5N} and R_{3P} are pentode resistance (on-resistance) and are given by,

$$R_{5N(P)} = \frac{V_{DS}}{I_{DS,N(P)} @ (V_{DS} = V_{GS} = V_{DD})}, \quad (1)$$

where $I_{DS,N(P)}$ is a drain-source current of nMOS (pMOS), which is a function of the drain voltage (V_{DS}) and the gate voltage (V_{GS}).

R_{3N} and R_{3P} are triode resistance and are defined as,

$$R_{3N(P)} = \frac{V_{DS}}{I_{DS,N(P)} @ (V_{GS} = V_{DD}, V_{DS} = V_{DD}/4)}. \quad (2)$$

In this paper, a critical peak noise voltage is assumed to half V_{DD} . Therefore, the resistance at $V_{DS}=V_{DD}/4$, which is an intermediate voltage between half V_{DD} and the ground, is used.

In the nominal supply voltage region, the equivalent resistances of the wire line drivers (R_{5N} and R_{3P}) are so small

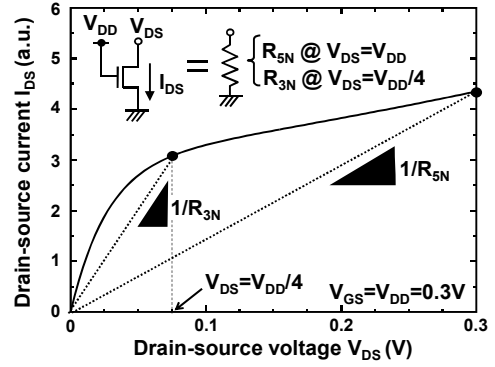


Fig. 6. Definition of equivalent resistance of nMOS.

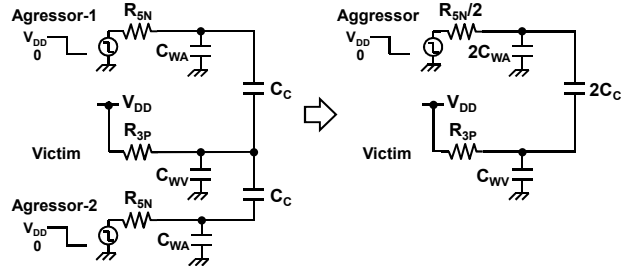


Fig. 7. Equivalent circuit of the coupled wire lines with two aggressors and one victim. This circuit can be converted to circuit with one aggressor.

that the wire resistance (R_W) must be taken into consideration as shown in the upper figure of Fig. 5. On the other hand, R_W can be ignored in the sub-threshold region, since R_{5N} and R_{3P} are much larger than R_W . Therefore, the equivalent circuit in the sub-threshold region can be easily analyzed as illustrated in the lower figure of Fig. 5.

For the circuit of the wire lines with two aggressors as shown in Fig. 1(a), the equivalent circuit in the sub-threshold region is depicted in Fig. 7. When the wire capacitances of the victim (C_{WV}) and aggressors (C_{WA}) are identical ($C_W=C_{WV}=C_{WA}$), the peak noise on the victim line voltage (V_{PEAK}) is derived using the wire capacitance (C_W) and the coupling capacitance between the aggressor and the victim (C_C) as follows,

$$V_{PEAK} = V_{DD} \frac{2r_f c}{r_f (3c+1)} \frac{1}{\alpha - \beta} \left(\left(\frac{\alpha}{\beta} \right)^{\alpha - \beta} - \left(\frac{\alpha}{\beta} \right)^{\beta - \alpha} \right), \quad (3)$$

where $c=C_C/C_W$ and $r_f=R_{3P}/R_{5N}$. Here, r_f is the equivalent resistance ratio for the falling noise. For the rising noise, $r_f=R_{3N}/R_{5P}$ is used instead of r_f . α and β are solutions of the following quadratic equation,

$$r_f (3c+1)x^2 + (2r_f c + r_f + c+1)x + 1 = 0. \quad (4)$$

Equation (3) is too complicated to discuss the V_{PEAK} dependence on V_{TH} , and hence the following simple approximation model of V_{PEAK} is introduced in this paper.

$$V_{PEAK, approx} = V_{DD} \left(\frac{r_f}{r_f + 0.5} \cdot \frac{c}{c + 0.5} \right)^{1.3}. \quad (5)$$

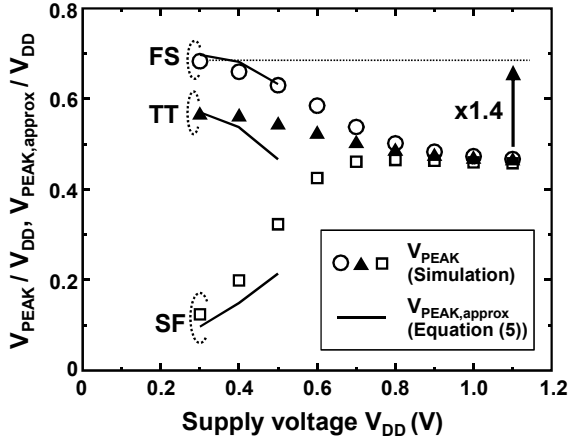


Fig. 8. Peak voltage of falling noise on 1.5mm coupled wire line with two aggressors and one victim at TT, FS, and SF process corners. V_{PEAK} is obtained by SPICE simulations and $V_{PEAK,approx}$ is calculated by the proposed approximation model equation (5).

The relative error ($|V_{PEAK} - V_{PEAK,approx}|/V_{DD}$) is less than 3.9% in the case of $0.5 < r_f < 10$ and $0.5 < c < 5$.

If the wire capacitances of the victim and aggressors are different, a slight modification of (5) is required. For example, when the wire capacitance of the aggressor is two times larger than that of the victim ($C_{WA} = 2C_{WV}$), V_{PEAK} can be approximated by using 1.5th power instead of 1.3th power in (5). In this case, the relative error is less than 4.9% at the condition of $0.5 < r_f < 10$ and $0.5 < c < 5$.

In the sub-threshold region, $I_{DS,N}$ in (1) and (2) is given by [8],

$$I_{DS,N} = I_{0,N} e^{\frac{V_{GS} - V_{TH,N} + \eta V_{DS}}{nU_T}} \left(1 - e^{-\frac{V_{DS}}{U_T}} \right), \quad (6)$$

where n is the sub-threshold slope parameter, η is the DIBL coefficient, U_T is the thermal voltage, $V_{TH,N}$ is V_{TH} of nMOS, and $I_{0,N}$ is the technology dependent parameter.

From (1), (2), and (6), r_f can be expressed as,

$$r_f = \frac{R_{3P}}{R_{5N}} \propto e^{\frac{|V_{TH,P} - V_{TH,N}|}{nU_T}}, \quad (7)$$

where $V_{TH,P}$ is V_{TH} of pMOS. This equation indicates that r_f has an exponential dependence on the V_{TH} difference between nMOS and pMOS. According to (5), the peak noise voltage depends on r_f . Thus, the peak noise voltage is strongly affected by the balance of V_{TH} between nMOS and pMOS, which means that it is especially crucial at the process corners, such as FS (fast-nMOS/slow-pMOS) and SF (slow-nMOS/fast-pMOS).

Fig. 8 shows the simulated peak noise voltage (falling noise) on the coupled wire line with one victim and two aggressors at the typical process condition (TT) and the corner conditions (SF and FS). The approximated peak noise ($V_{PEAK,approx}$) calculated by (5) is also shown, and it agrees with the simulated results. The measured V_{PEAK} dependence shown in Fig. 3 is different from the simulated one shown in

Fig. 8 because the V_{TH} balance of the measured chip is between TT and SF.

In the worst case FS corner simulations, V_{PEAK}/V_{DD} at 0.3V is 1.4 times larger than that at 1.1V. The reason why the crosstalk noise at the nominal supply voltage region does not depend on the balance of V_{TH} is 1) the dependence of the equivalent resistances of the drivers on V_{TH} is much smaller than that in the sub-threshold region, and 2) the influence of the wire resistances is not ignored. In contrast, the peak noise voltage in the sub-threshold region is much more sensitive to the balance of V_{TH} . This is because the peak noise voltage depends on the equivalent resistance ratio (r_f and r_r), which has an exponential dependence on the V_{TH} difference between nMOS and pMOS as indicated in (7). Therefore designers must take the process corner condition, such as SF and FS, into consideration as the worst-case condition for signal integrity in sub-threshold circuits.

IV. CONCLUSION

In this paper, the dependence of the peak noise voltage induced by crosstalk on the V_{TH} difference between nMOS and pMOS in sub-threshold circuits was presented. The large crosstalk noise due to the imbalanced V_{TH} was measured in the test chip with 1.5-mm coupled wires fabricated in a 40-nm CMOS process. A new crosstalk noise model was proposed and verified with SPICE simulations. In the worst case FS corner simulations, the noise amplitude increased by 1.4 times when V_{DD} was reduced from 1.1V to 0.3V, which was explained by the proposed model.

ACKNOWLEDGMENTS

This work was carried out as a part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO).

REFERENCES

- [1] A.W. Wang, et al., *Sub-threshold Design For Ultra Low-Power Systems*, New York: Springer, 2006
- [2] K. Hirairi, et al., "13% Power Reduction in 16b Integer Unit in 40nm CMOS by Adaptive Power Supply Voltage Control with Parity-Based Error Prediction and Detection (PEPD) and Fully Integrated Digital LDO," *ISSCC*, pp. 486-487, 2012.
- [3] H. Fuketa, et al., "Adaptive Performance Compensation with In-Situ Timing Error Prediction for Subthreshold Circuits," *CICC*, pp. 215-218, 2009.
- [4] M. Nanua and D. Blaauw, "Investigating Crosstalk in Sub-Threshold Circuits," *ISQED*, pp. 539-646, 2007.
- [5] T. Sakurai, "Closed-form Expressions for Interconnection Delay, Coupling, and Crosstalk in VLSIs," *IEEE Trans. Electron Devices*, vol. 40, pp. 118-124, Jan. 1993.
- [6] S.C. Wong, et al., "Modeling of Interconnect Capacitance, Delay, and Crosstalk in VLSI," *IEEE Trans. Semiconductor Manufacturing*, vol. 13, pp. 108-111, Feb. 2000.
- [7] T. Sato, et al., "Accurate In Situ Measurement of Peak Noise and Delay Change Induced by Interconnect Coupling," *IEEE JSSC*, vol. 36, pp. 1587-1591, Oct. 2001.
- [8] M. Alioto, "Understanding DC Behavior of Subthreshold CMOS Logic Through Closed-Form Analysis," *IEEE Trans. Circuits and Systems I*, vol. 7, pp. 1597-1607, Jul. 2010.