2.1 Times Increase of Drain Efficiency by Dual Supply Voltage Scheme in 315MHz Class-F Power Amplifier at Output Power of -20dBm

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***Abstract*—Dual power supply voltage (V_{DD}) scheme is proposed to increase the efficiency of a power amplifier (PA) with small output power (P_{OUT}) for short-range wireless sensor networks (e.g. body area networks). At P_{OUT} of -20dBm, compared with the conventional single V_{DD} PA, the drain efficiency (DE) and the global efficiency (GE) of the proposed dual V_{DD} PA increase by 2.1 times and 1.5 times, respectively. A class-F PA fabricated in 40-nm CMOS with the proposed dual V_{DD} (0.2V and 0.56V) achieves the highest DE of 42% at P_{OUT} of -20dBm in the published PA's. The PA is applied to a 315MHz OOK transmitter (TX) and the TX achieves the highest GE of 28% at P_{OUT} of -20dBm and the lowest energy of 36pJ/bit (= 36μW@1Mbps) in the published TX's.**

I. INTRODUCTION

In short-range wireless sensor networks (e.g. body area networks), an ultra low power transmitter (TX) with small output power (P_{OUT}) is required. In this paper, the target P_{OUT} is -20dBm and the target communication distance is 1m, assuming -25dB propagation loss at the 1-m distance, -5dB x 2 loss at TX/RX antennas, and -55dBm receiver sensitivity [1]. The target TX power consumption (P_{TOTAL}) is less than 50μW at 1Mbps and 315-MHz carrier frequency. In order to reduce P_{TOTAL} of TX less than 50μW at P_{OUT} of -20dBm (= 10μW), the global efficiency (GE) (= P_{OUT}/P_{TOTAL}) of a TX should be larger than 20% (= 10μW/50μW). Increasing the efficiency at small P_{OUT}, however, is a design challenge.

Fig. 1 shows the dependence of drain efficiency (DE) on P_{OUT} in previously published power amplifiers (PA's) [1-7]. As P_{OUT} decreases, DE also decreases, because various losses become non-negligible. In PA's [4,5] for the conventional wireless communications (e.g. cell-phone and WLAN) where the communication distance is 100m~1km, P_{OUT} is +20dBm ~ +30dBm and DE is higher than 60%. In contrast, in PA's [1-3,7] for the short-range wireless sensor networks (e.g. body area networks) where the communication distance is 1m~10m, P_{OUT} is -20dBm ~ -10dBm and DE is less than 30%. For example, in our previous work [1], DE is 20% and GE is 16%, which does not meet our design target (GE > 20%). Therefore, the purpose of this paper is to achieve DE higher than 40% and GE higher than 20% at P_{OUT} of -20dBm. A newly proposed dual power supply voltage (V_{DD}) scheme increases DE and GE by 2.1 times and 1.5 times, respectively, compared with the conventional single V_{DD} scheme [1].

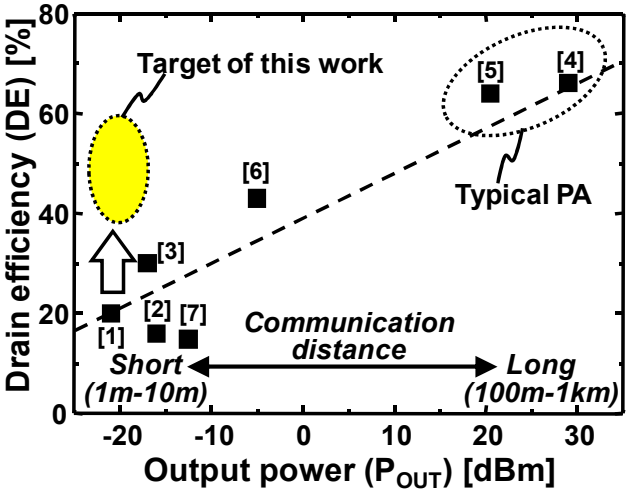

Fig. 1. Dependence of drain efficiency on output power in previously published PA's and target of this work.

II. DESIGN OF DUAL V_{DD} CLASS-F POWER AMPLIFIER

In this section, the dual V_{DD} scheme is introduced to increase DE of PA at P_{OUT} of -20dBm. In this paper, a class-F PA instead of a class-D or class-E PA is used, because the class-F PA achieved the highest efficiency at our design target.

Fig. 2 (a) shows a schematic of the class-F PA. V_{DD1} is the amplitude of the input (In) and V_{DD2} is the power supply voltage of PA. L_{DC} is a choke coil, C_{DC} is an AC-coupling capacitor, L_1 and C_1 resonate at the fundamental frequency (= 315MHz), and L_3 and C_3 resonate at the third harmonic (= 3 x 315MHz). Fig. 2 (b) shows an equivalent circuit of Fig. 2 (a) [8]. A transformer is formed by the L and C networks in Fig. 2 (a) equivalently. The transformer ratio is defined as n. P_{OUT} of the class-F PA in Fig. 2 (b) is given by [9]

$$P_{OUT} = \frac{\left(\frac{4}{\pi}\times V_{DD2}\right)^2}{2n^2\times 50(\Omega)} \propto \left(\frac{V_{DD2}}{n}\right)^2. \quad (1)$$

Fig. 3 shows a dependence of P_{OUT} on V_{DD2} calculated with Eq. (1), when n is varied from 0.01 to 100. DE is the highest at n = 1, because the loss of the transformer in Fig. 2 (b) is proportional to n (n > 1) or 1/n (n < 1) [9]. Therefore, a PA design with n = 1 is the best design. The PA design with

P_{OUT} of -20dBm in this work is quite different from the typical PA design with P_{OUT} of +20dBm ~ +30dBm. In the latter design, n is less than 1, while n is larger than 1 in the former design. In order to increase DE in the typical PA, V_{DD2} should be increased and n should be increased to 1. In contrast, in order to increase DE in the PA with P_{OUT} of -20dBm in this work, V_{DD2} should be decreased and n should be decreased to 1. In the conventional PA's with small P_{OUT} [2, 3], however, V_{DD2} is not decreased (= 1V) and large n is used, thereby DE is reduced. In this work, V_{DD2} is decreased to 0.2V and n is decreased to 4.2, which will be shown in Fig. 5 (b). If V_{DD1} is also decreased to 0.2V, the on-current of the transistor in Fig. 2 (a) is greatly reduced, because the transistor operates in the sub-threshold region. In order to solve the problem, the dual V_{DD} scheme is proposed in this paper.

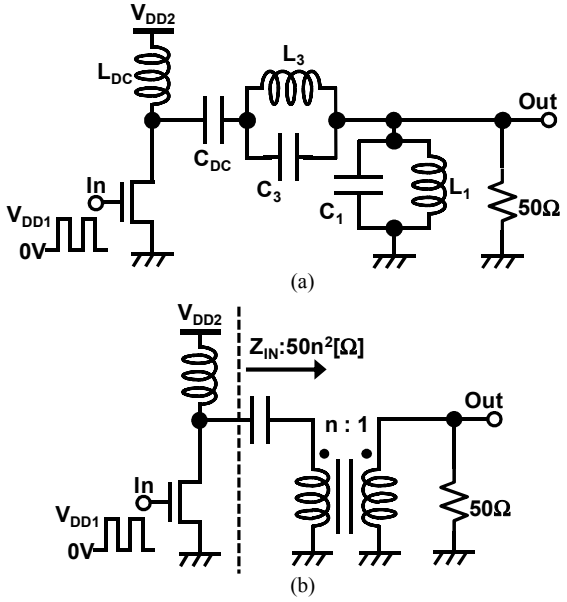

Fig. 2. (a) Schematic of a class-F PA. (b) Equivalent circuit of (a).

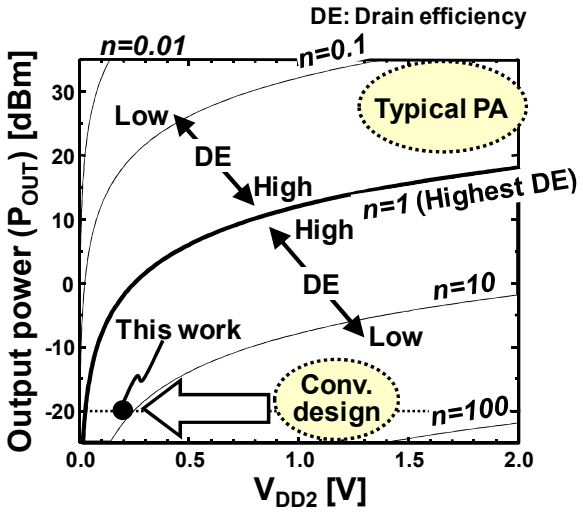

Fig. 3. Dependence of output power on V_{DD2} calculated with Eq. (1). Transformer ratio (n) in Fig. 2 (b) is varied from 0.01 to 100.

III. Design of Transmitter with Dual V_{DD} Power Amplifier

In this section, the dual V_{DD} scheme is optimized to maximize GE of TX at P_{OUT} of -20dBm. Fig. 4 shows a schematic of TX including the dual V_{DD} class-F PA. The carrier frequency is 315MHz for a radio communication standard of ARIB STD-T93 (315MHz band) in Japan and the data rate is 1Mbps. As shown in Fig. 4, P_{TOTAL} is the sum of the buffer, the mixer, and the PA powers. In the PA design with P_{OUT} of -20dBm, the buffer power is not negligible and the PA-only (=DE only) design optimization is inadequate. Therefore, GE is maximized at P_{OUT} of -20dBm by optimizing n. In the design optimization, V_{DD1}, V_{DD2}, C_{DC}, and L_{DC} are varied according to n, and L_1, C_1, L_3, C_3, and transistor size are fixed.

Figs. 5 (a), (b), and (c) show the SPICE simulated n dependence in TX with P_{OUT} of -20dBm. Fig. 5 (a) shows the simulated dependence of P_{TOTAL}, the buffer power, and the PA power on n. Fig. 5 (b) shows the simulated dependence of V_{DD1} and V_{DD2} on n. Fig. 5 (c) shows the simulated dependence of C_{DC} and L_{DC} on n. C_{DC} and L_{DC} are decided by n and the impedance matching. The power consumption in Fig. 5 (a) is simulated at V_{DD1} and V_{DD2} shown in Fig. 5 (b) and C_{DC} and L_{DC} shown in Fig. 5 (c). As shown in Fig. 5 (b), the conventional TX with single V_{DD} is designed at n = 9.6 and V_{DD1} = V_{DD2} = 0.47V. In contrast, as shown in Fig. 5 (a), P_{TOTAL} is minimum at n = 4.2, thereby GE is maximum at n = 4.2. The corresponding V_{DD1} = 0.56V and V_{DD2} = 0.2V. Table I shows the optimum parameters in the conventional single V_{DD} design and the dual V_{DD} design.

The reason for the optimum dual V_{DD} is discussed. When n is reduced from 10 to 2, V_{DD2} is reduced (Fig. 5 (b)) and the PA power is reduced (Fig. 5 (a)). In contrast, V_{DD1} is increased (Fig. 5 (b)) and the buffer power is increased (Fig. 5 (a)). When n is reduced below 3, V_{DD1} drastically increases (Fig. 5 (b)), because the transistor operation changes from the saturation region to the linear region, thereby the corresponding buffer power drastically increases (Fig. 5 (a)). Therefore, P_{TOTAL} is minimum at n = 4.2 (Fig. 5 (a)), thereby GE is maximum at n = 4.2.

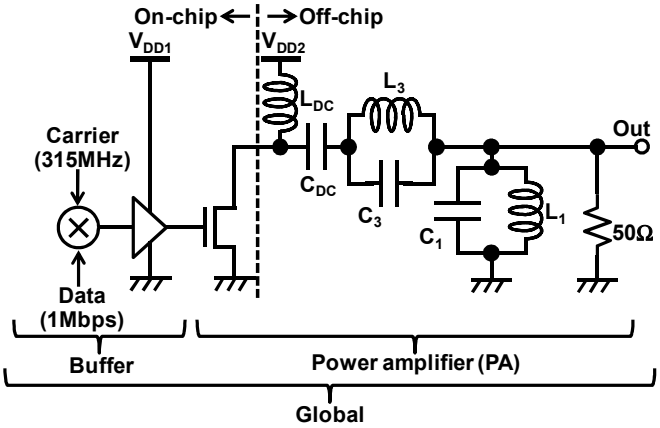

Fig. 4. Schematic of a dual V_{DD} TX with a class-F PA.

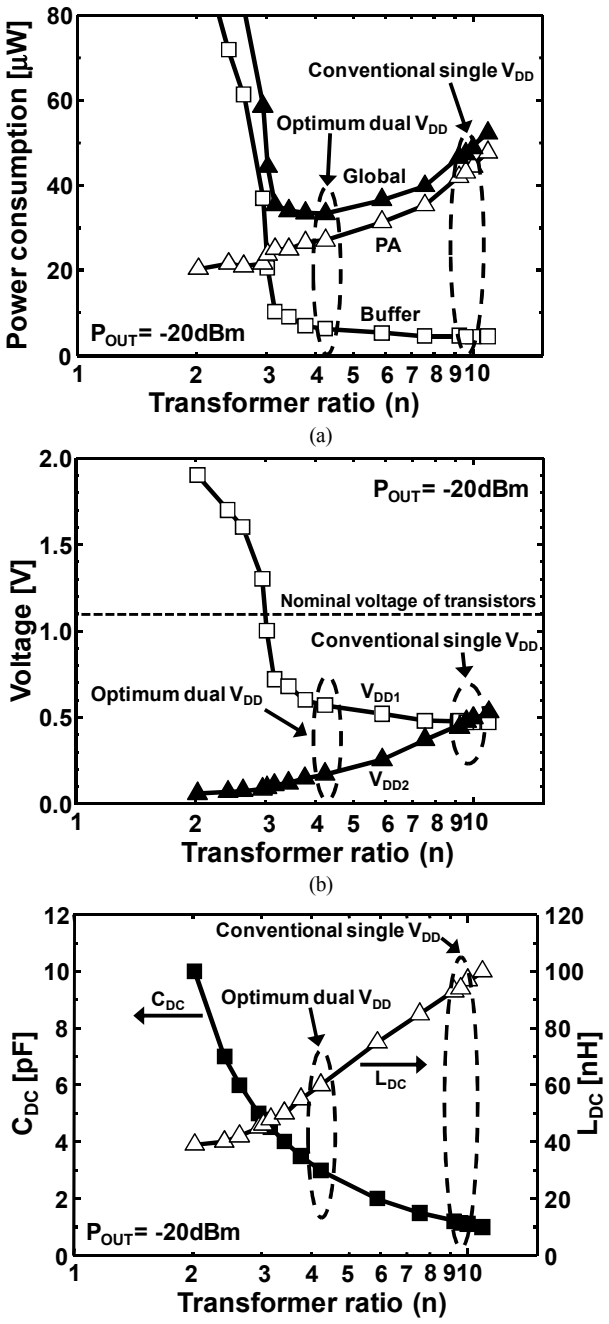

Fig. 5. SPICE simulated transformer ratio (n) dependence in TX with P_{OUT} of -20dBm. (a) Power consumption vs. n. (b) V_{DD1} and V_{DD2} vs. n. (c) C_{DC} and L_{DC} vs. n.

TABLE I PARAMETERS IN CONVENTIONAL SINGLE V_{DD} DESIGN AND PROPOSED DUAL V_{DD} DESIGN.

	Conventional single V_{DD}	Proposed dual V_{DD}
V_{DD1} [V]	0.47	0.56
V_{DD2} [V]	0.47	0.2
C_{DC} [pF]	1	3
L_{DC} [nH]	100	60

IV. MEASUREMENT RESULTS

To demonstrate the advantage of the proposed dual V_{DD} scheme, a test chip is fabricated in 1.1V, 40-nm CMOS process. Fig. 6 shows the die microphotograph and the layout. The die size is 0.5mm x 0.6mm and the core area of TX is 56μm x 22μm. The measured parameters of the conventional and the proposed PAs are given in Table I, while the same two resonators are used as follows: L_1 = 22nH, C_1, = 11pF, L_3, = 2.7nH, and C_3 = 12pF.

Fig. 7 shows the measured GE and P_{OUT} of TX in the proposed dual V_{DD} scheme, when V_{DD1} and V_{DD2} are varied. At the target P_{OUT} of -20dBm, the maximum GE is 28% at V_{DD1} = 0.56V and V_{DD2} = 0.2V, which consists with the simulated results in Fig. 5. As P_{OUT} increases from -20dBm to -10dBm, the optimum V_{DD1} and V_{DD2} also increase. When V_{DD1} is below 0.52V, the buffer fails to work at the 315-MHz carrier frequency.

Fig. 8 shows the measured output spectrum of the TX. The 314MHz carrier is modulated by 1Mbps OOK. The measured P_{OUT} of -20dBm meets the radio communication standard of ARIB STD-T93 (315MHz band) which specifies the operating frequency of 312-315.25MHz in Japan.

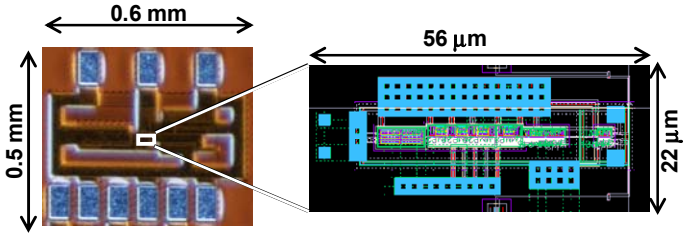

Fig. 6. Die microphotograph and layout of proposed dual V_{DD} PA in 40-nm CMOS.

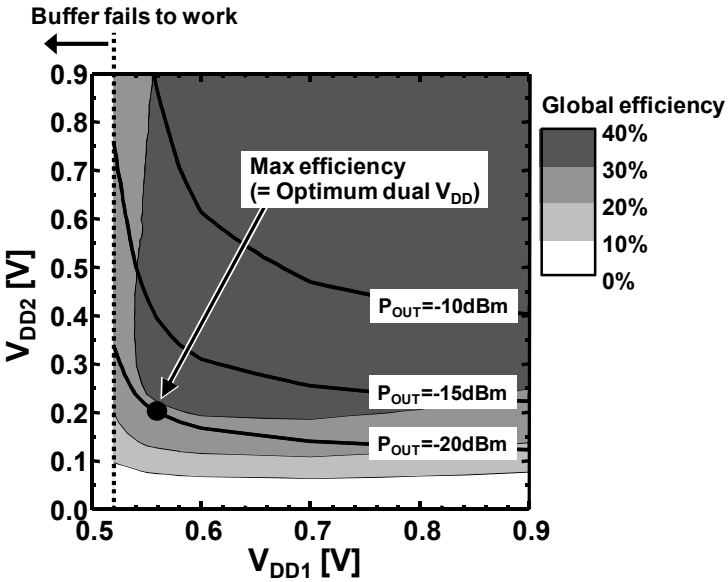

Fig. 7. Measured contours of global efficiency (GE) and P_{OUT}, when V_{DD1} and V_{DD2} are varied. Gray levels represent the values of GE. The lines are the contour of P_{OUT}. At target P_{OUT} of -20dBm, maximum GE is 28% at V_{DD1} = 0.56V and V_{DD2} = 0.2V.

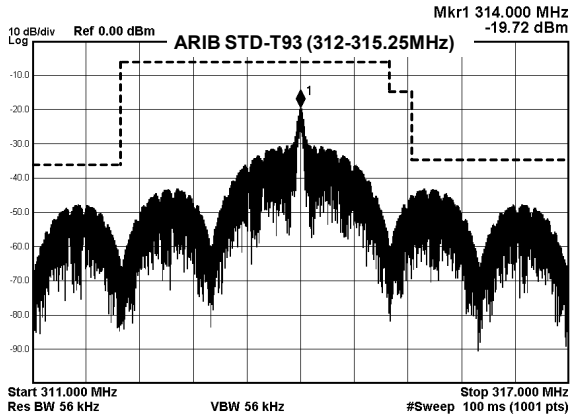

Fig. 8. Measured output spectrum of the TX. The 314MHz carrier is modulated by 1Mbps OOK.

Fig. 9 shows the measured dependence of DE and GE on P_{OUT}. The conventional single V_{DD} scheme and the proposed dual V_{DD} scheme are compared. In the single V_{DD} PA, V_{DD1} and V_{DD2} are varied with same value. In the dual V_{DD} PA, V_{DD1} and V_{DD2} are varied according to the optimum V_{DD1} and V_{DD2} in Fig. 7, respectively. At the target P_{OUT} of -20dBm, compared with the conventional single V_{DD} PA, DE and GE of the proposed dual V_{DD} PA increases by 2.1 times and 1.5 times, respectively.

The design issue of the proposed dual V_{DD} scheme is a DC-DC converter required for the additional V_{DD}. If the power conversion efficiency of the DC-DC converter is less than 66%, GE of the proposed dual V_{DD} PA with the DC-DC converter has no advantage over the conventional single V_{DD} PA. For example, however, a 0.45-V input buck converter with more than 90% efficiency from 2μW to 50μW [10] is reported. The proposed dual V_{DD} PA is still available with such converters.

In Fig. 9 and Table II, this work is compared with the previously published TX's with small P_{OUT} [1-3]. The proposed dual V_{DD} scheme achieves the highest DE of 42% and the highest GE of 28%, thereby achieving the lowest energy of 36pJ/bit (= 36μW@1Mbps) in the published TX's.

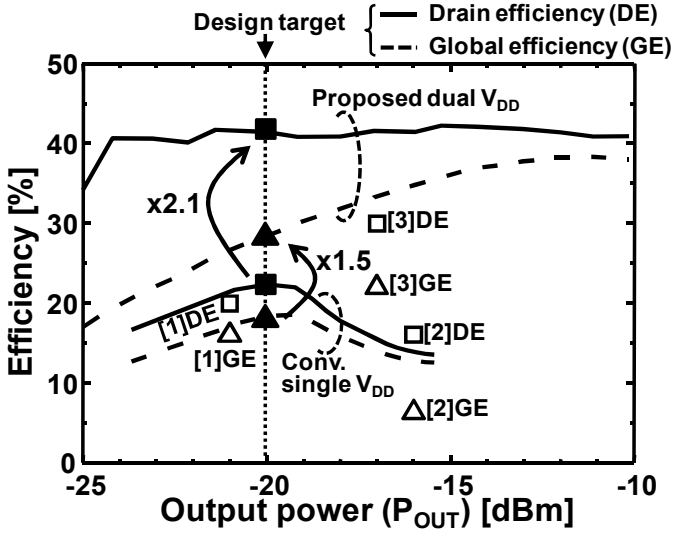

Fig. 9. Measured dependence of drain efficiency and global efficiency on output power. Conventional single V_{DD} PA and proposed dual V_{DD} PA are compared. Previous papers are also shown.

TABLE II COMPARISON WITH PREVIOUS PAPERS.

	Unit	[2]	[3]	[1]	This work
CMOS technology	nm	130	130	40	40
Supply voltage	V	1	1	0.5	V_{DD1}:0.56 V_{DD2}:0.2
Frequency	MHz	300-450	400	315	315
Data rate	Mbps	0.1	0.2	1	1
PA class	-	Edge-combiner	Edge-combiner	Class F	Class F
Output power (P_{OUT})	dBm	-16	-17	-21	-20
Drain efficiency	%	16	30	20	42
Power consumption of TX (P_{TOTAL})	μW	400	90	52	36
Global efficiency (P_{OUT}/P_{TOTAL})	%	6.3	22	16	28
Energy	pJ/bit	4000	450	52	36
TX includes	-	Osc.+PLL+ Mixer+PA	Osc.+PLL+ Mixer+PA	Mixer+ Buffer+PA	Mixer+ Buffer+PA

V. CONCLUSIONS

The dual V_{DD} scheme is proposed to increase the efficiency of PA with small P_{OUT}. At P_{OUT} of -20dBm, compared with the conventional single V_{DD} PA, DE and GE of the proposed dual V_{DD} PA increases by 2.1 times and 1.5 times, respectively. Compared with the previously published papers, the proposed dual V_{DD} PA achieves the highest DE of 42% and the highest GE of 28% at P_{OUT} of -20dBm, thereby achieving the lowest energy of 36pJ/bit (= 36μW@1Mbps) in the published TX's.

ACKNOWLEDGMENT

This work was carried out as a part of the Extremely Low Power (ELP) project supported by the Ministry of Economy, Trade and Industry (METI) and the New Energy and Industrial Technology Development Organization (NEDO).

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