18.1 Insole Pedometer with Piezoelectric Energy Harvester and 2V Organic Digital and Analog Circuits

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Energy harvesting is an enabling technology for realizing an ambient power supply for wireless sensor nodes and mobile devices. By using flexible photovoltaic cells and piezoelectric films, we can readily harvest ambient energy if flexible energy harvesters can be realized. Conventional silicon circuits, however, are not best suited to realizing flexible large-area energy harvesters because they are not mechanically conformable to uneven surfaces such as shoes. To address this challenge, we propose an organic insole pedometer with a piezoelectric energy harvester in this paper as the first step toward ambient energy harvesting using organic flexible electronics.

The main challenge in the design of organic circuits for piezoelectric energy harvesting is the robust operation of PMOS-only circuits at a low supply voltage. In energy-harvesting applications, the harvested power is small and the rectified voltage is low (e.g., 2V). In organic circuit design, PMOS-only circuits are often used, because the mobility of PMOS transistors is much higher than that of NMOS transistors in our process. The operation of PMOS-only circuits is not robust and the noise margin is small because of their rationed-logic nature. A Pseudo-CMOS inverter that consists of four PMOS transistors [1] has high gain, but it requires a negative voltage bias. In energy-harvesting applications, however, a single power supply is typical. Therefore, in this work, to increase the noise margin of PMOS-only logic circuits, a negative voltage is generated by a charge pump and is applied as the bias of Pseudo-CMOS inverters. We use a 2V PMOS process with self-aligned monolayer (SAM) technology [2] and DNTT [3] for PMOS transistors.

Figure 18.1.1 shows a photograph of the proposed insole pedometer including the piezoelectric energy harvester and the 2V organic PMOS rectifier and counter. A polyvinylidene difluoride (PVDF) sheet is used as the piezoelectric energy harvester. Twenty-one rolls of PVDF film are embedded in the insole. Each time the insole is pressed by the foot during walking, the harvested energy is rectified by the organic rectifier and the number of the steps is counted by the organic counter.

Figure 18.1.2 shows a block diagram of the proposed organic insole pedometer. It consists of four circuit blocks. The all-PMOS full-wave rectifier supplies a voltage V_{DD} of approximately 2V to all circuit blocks. In the clock generator, the output of the PVDF harvester is half-wave-rectified and a Schmitt trigger inverter converts the half-wave-rectified signal into a clock signal. The generated clock signal is sent to both the PMOS negative voltage generator and a 14-bit Pseudo-CMOS counter with gate-boosted PMOS switches. The negative voltage generator supplies a voltage V_{SS} (e.g., -2V) to the counter.

Figure 18.1.3(a) shows a schematic of the all-PMOS full-wave rectifier [4]. A 100V sinusoidal wave was rectified in [4], while a 2V sinusoidal wave is rectified in this work. Figure 18.1.3(b) shows the measured waveform of the 2V full-wave rectifier without a smoothing capacitor. The output is open and the output amplitude of the rectifier is approximately 2V with 1Hz, 4V peak-to-peak sinusoidal input signals. Figure 18.1.3(c) shows the measured output voltage versus the output current of the rectifier with a 1μF smoothing capacitor. The proposed PMOS rectifier (W/L of each transistor is 144) can provide a power of at least 10μW to the circuit. Figure 18.1.3(d) shows the measured waveforms for a 20×28cm^2 sheet of PVDF energy harvester and the rectified output. The 1μF smoothing capacitor can be charged by providing a mechanical force to the PVDF energy harvester.

Figure 18.1.4(a) shows a schematic of the proposed all-PMOS negative voltage generator, which consists of a Pseudo-CMOS inverter [1], two diode-connected PMOS transistors, and two MIM capacitors. To charge the left capacitor, the output buffer of the Pseudo-CMOS inverter consists of transistors with width of 2mm (W/L=100) and 6mm (W/L=300). The performance of the negative voltage generator strongly depends on the threshold voltage of the PMOS diode-connected transistors. To reduce the reverse leakage current, the gate width of each diode-connected transistor is smaller (W/L=50) than that of the inverter. The measured waveforms and output voltage versus the output current are shown in Figs. 18.1.4(b) and 18.1.4(c), respectively. The output voltage (V_{OUT}) of the negative voltage generator is -1.6V in the case of 10Hz clock pulses and can provide a power of at least 10μW power to the load circuit.

To generate clean clock signals from noisy input signals using the PVDF energy harvester, a PMOS-only Schmitt trigger inverter based on pseudo-CMOS logic is proposed. Figure 18.1.5 shows the schematics and output waveforms of the proposed Schmitt trigger inverter. Unlike conventional CMOS Schmitt trigger inverters that can use both PMOS and NMOS transistors to generate hysteresis, in the proposed PMOS-only Schmitt trigger inverter, the first stage is used to adjust the lower bound (VM-) of the hysteresis, while the second stage is for adjusting the upper bound (VM+). When the input signal is swept from low to high, the top PMOS transistor of the second stage (M_1), which is controlled by the third-stage Pseudo-CMOS inverter output, pushes the high-to-low switching point toward the right, as can be seen in Fig. 18.1.5(c); on the other hand, when the input is swept from high to low, the ground-connected PMOS transistor (M_2) of the first stage weakens the pull-up force of the top two PMOS transistors, which forces the low-to-high switching point to move toward the left and widen the hysteresis, as shown in Fig. 18.1.5(c). On the basis of the measured waveform in Fig. 18.1.5(d), we can find that the switching points for the high-to-low and low-to-high transients have approximately 0.3V difference, and this characteristic plays a key role in supplying clean clock signals for the counter.

Figure 18.1.6 shows the schematics and measured waveforms of a single-stage 2V Pseudo-CMOS binary counter with asynchronous reset. By connecting fourteen such stages, we can build a 14-bit binary counter for the proposed pedometer. On the basis of a divide-by-two frequency divider, a new gate-boosting technique is applied in this counter to compensate for the poor conductivity of PMOS-only transmission gates. By employing a level-shifted clock buffer, as shown in Fig. 18.1.6(a), we can effectively overdrive PMOS transmission gates by applying negative voltages though the V_{SS} terminal in the clock buffer. Compared with Fig. 18.1.6(b), where the gate-boosting technique is not applied and the PMOS transmission gates suffered from poor conductivity, the output waveform of the gate-boosted counter in Fig. 18.1.6(c) is clean owing to the larger clock signal swing from V_{DD} to V_{SS}. Note that Fig. 18.1.6 only shows the signals from output Q1, while QB1 is used for connecting to the next stage of the binary counter. Figure 18.1.7 shows photographs of the organic circuits and summarizes their key features. The organic insole pedometer consists of 462 transistors and its size is 22×7cm^2.

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Dinaphtho[2,3-b:2',3'-f]chalcogenopheno[3,2-b]chalcogenophenes, and Their Application to Field-Effect Transistors," *Journal of American Chemical Society*, vol. 129, no. 8, pp. 2224-2225, Aug. 2007.
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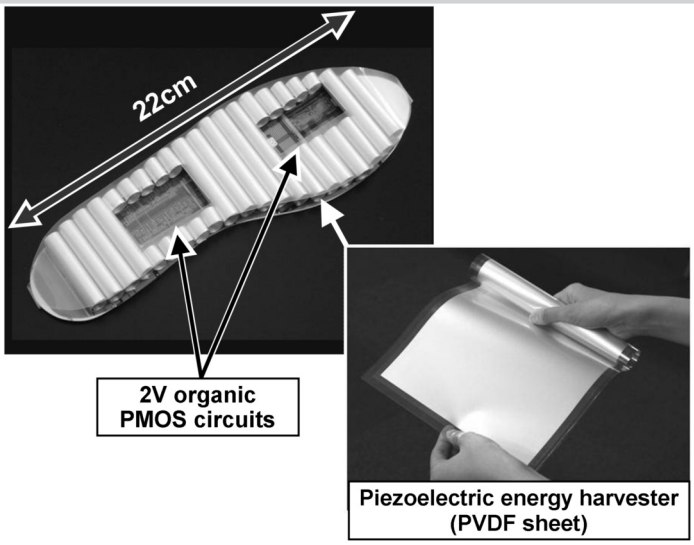

Figure 18.1.1: Prototype of the organic insole pedometer with piezoelectric energy harvester and 2V digital and analog circuits.

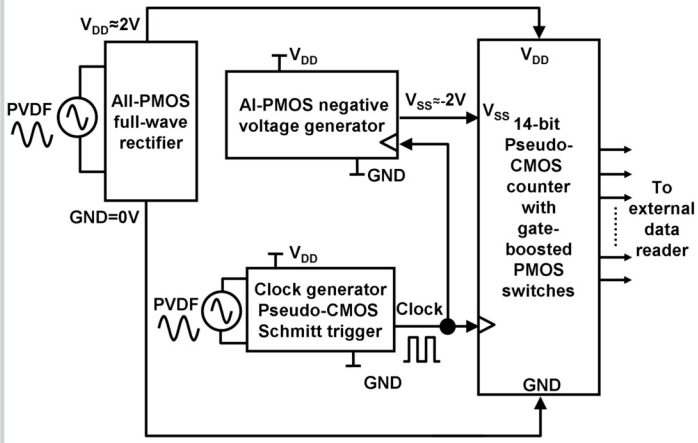

Figure 18.1.2: System block diagram of the organic insole pedometer.

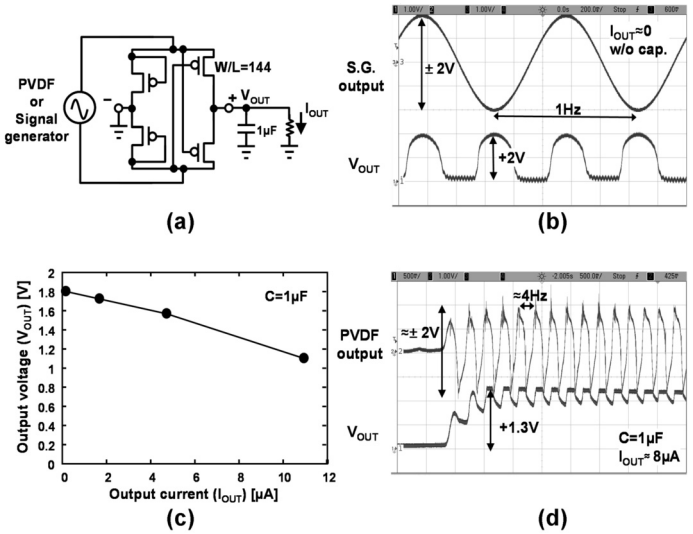

Figure 18.1.3: 2V organic all-PMOS rectifier.

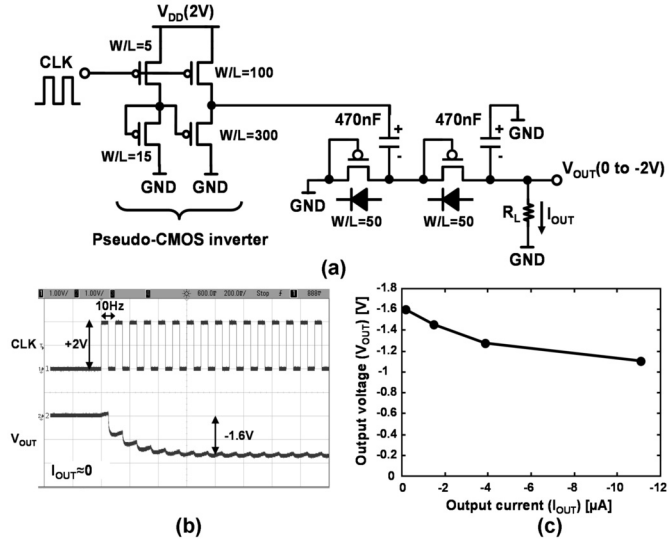

Figure 18.1.4: All-PMOS negative voltage generator.

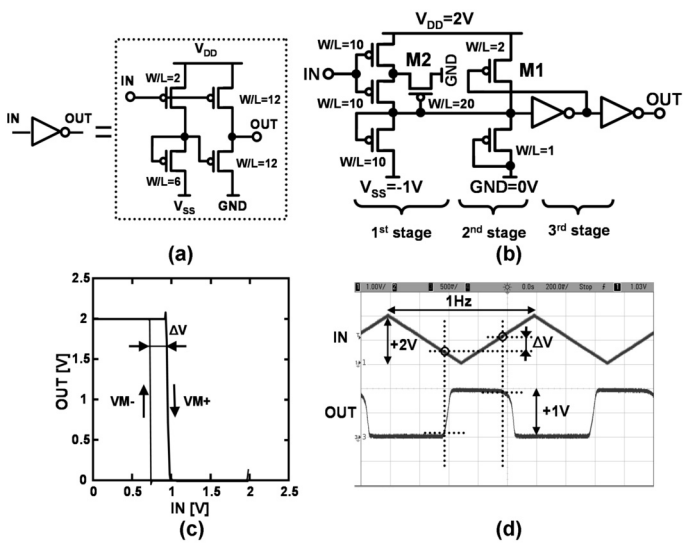

Figure 18.1.5: Pseudo-CMOS Schmitt trigger inverter.

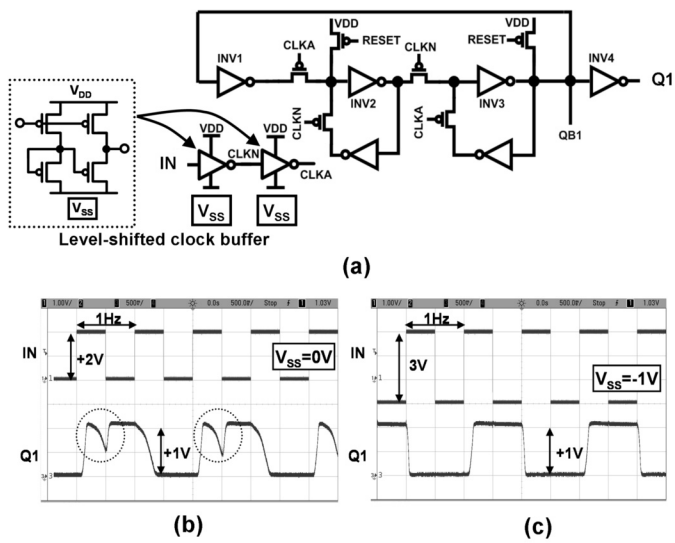

Figure 18.1.6: Pseudo-CMOS counter with gate-boosted PMOS switches.

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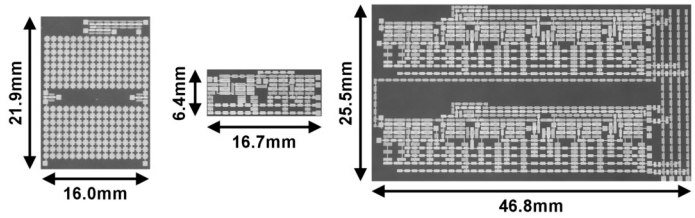

(a) All-PMOS negative voltage generator (b) Pseudo-CMOS Schmitt trigger (c) Pseudo-CMOS 2bit counter with gate-boosted PMOS switches

Organic transistors	
Semiconductor material	DNTT(1.0 cm^2/Vs)
Gate oxide material, thickness	SAM* 2nm + AlOx 4nm = 6nm
Minimum gate length	20μm (analog), 50μm (digital)
Energy harvester and pedometer	
Harvester	Piezoelectric energy harvester (PDFV)
Number of transistors	462Tr.
Pedometer size	22x7cm^2

*SAM: Self assembled monolayer

Figure 18.1.7: Photographs and key features.

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