28.5 13% Power Reduction in 16b Integer Unit in 40nm CMOS by Adaptive Power Supply Voltage Control with Parity-Based Error Prediction and Detection (PEPD) and Fully Integrated Digital LDO

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Scaling power supply voltages (V_{DD}'s) of logic circuits down to the sub/near-threshold region is a promising approach to achieve significant power reductions. Circuit delays in the ultra-low voltage region, however, are extremely sensitive to process, voltage, and temperature (PVT) variations, and hence, large timing margins are required for worst-case design. Since such large timing margins reduce the energy efficiency benefits of lower V_{DD}, adaptive V_{DD} control to cope with PVT variations is indispensable for ultra-low voltage circuits. In this paper, an adaptive V_{DD} control system with parity-based error prediction and detection (PEPD) and 0.5-V input fully-integrated digital LDO (DLDO) is proposed.

In conventional adaptive V_{DD} control systems [1], a critical-path replica is used for the PWM controller of a Buck converter to control V_{DD}. In ultra-low voltage logic circuit design, however, the replica approach is not effective, because the delay mismatch between the actual data path and the critical-path replica is large due to within-die random delay variations. To address such problems, this paper proposes an adaptive V_{DD} control managed by PEPD. Figure 28.5.1 shows a block diagram of the proposed adaptive V_{DD} control system with PEPD and DLDO. Adaptive V_{DD} control is applied to a 16b integer unit (IU). 20 IU's are implemented, and the V_{DD}'s of 20 IU's ($V_{DD(IU)}$) are regulated by DLDO operating at an external supply voltage ($V_{DD(EXT)}$). An LDO instead of a Buck converter or a switched capacitor DC-DC converter is used, because an LDO does not require an off-chip inductor and provides precise control of the output voltage. The timing margin of the IU is monitored with PEPD, and a setup error warning is generated when timing slack is not sufficient. The setup error warning rate is calculated with a warning rate calculator and an up/down signal from the calculator is given to DLDO to control $V_{DD(IU)}$, according to the warning rate. In this way, adaptive V_{DD} control at a constant setup error warning rate is achieved. The DLDO in [2] requires a voltage reference and a comparator, while the proposed adaptive V_{DD} control is a fully-digital approach, because a voltage reference is not required, which is important in the ultra-low voltage design.

Figure 28.5.2 shows the proposed PEPD and conventional techniques to predict setup errors and to detect functional errors in FFs. The proposed PEPD combines a conventional setup error prediction FF and error detection by parity. The setup error prediction FF [3] is used to monitor the timing margin and predict timing errors before they actually occur. In adaptive V_{DD} control systems for ultra-low voltage logic circuits, high path coverage of in-situ setup error prediction is required, because within-die random delay variations increase as V_{DD} is reduced. The conventional setup error prediction FF, however, can only predict timing errors on paths where the FF is inserted. In order to achieve high path coverage for setup error prediction, many setup error prediction FFs are required, resulting in significant area overhead. In contrast, the proposed PEPD achieves 100% path coverage of setup error predictions, with a 29% increase in FF count. In addition, functional errors in FFs are also a severe problem in ultra-low voltage logic circuits, because such errors determine the minimum operating voltage (V_{DDmin}) [4]. Therefore, the in-situ functional error detection for FFs is required. By utilizing the parity generators and checkers for setup error prediction, the proposed PEPD also can detect any functional error amongst each group of 4 FFs. The error detection granularity is thus finer than in the conventional parity case, which detects errors among groups of 17 FFs.

Figure 28.5.3 shows the measured dependence of error or warning rate of the IU on $V_{DD(IU)}$ at 1.5MHz. In order to check the validity of the setup error warning, the real setup error is measured with a tester. As $V_{DD(IU)}$ increases, error or warning rates decrease exponentially. As temperature increases, the required $V_{DD(IU)}$ decreases. At a fixed rate, $V_{DD(IU)}$ of the setup error warning is higher than that of the real setup error, because the setup error warning has timing margins of T_1+T_2, where T_1 and T_2 represent the delays of the parity generator and delay buffers in the PEPD shown in Fig. 28.5.2, respectively. Similarly, at a fixed rate, $V_{DD(IU)}$ of the FF error detection is also higher than that of the real setup error, because the FF error detection has a timing margin of T_1. These timing margins enable accurate prediction of timing errors. In the proposed adaptive V_{DD} control system with PEPD, $V_{DD(IU)}$ is adaptively controlled such that the setup error warning rate is held steady at 2×10^{-4} for a given clock frequency. For example, when temperature changes from 0°C to 25°C, $V_{DD(IU)}$ adaptively changes from 407mV to 375mV.

Figure 28.5.4 shows the measured adaptive $V_{DD(IU)}$ control with DLDO at the fixed setup error warning rate of 2×10^{-4}. Dependence of $V_{DD(IU)}$ on clock frequency and temperature are shown in Figs. 28.5.4 (a) and (b), respectively. In Fig. 28.5.4 (a), as the clock frequency increases, $V_{DD(IU)}$ increases. In Fig. 28.5.4 (b), as the temperature increases, $V_{DD(IU)}$ decreases at a fixed clock frequency of 6MHz. In this case, the highest $V_{DD(IU)}$ is 560mV in the worst case (slow die and –50°C).

Figure 28.5.5 shows the measured adaptively-controlled $V_{DD(IU)}$ waveform at different clock frequencies of the IU. $V_{DD(IU)}$ with a 5MHz clock is 412mV, while $V_{DD(IU)}$ with a 6MHz clock is 421mV. When the clock frequency changes from 5MHz to 6MHz, the setup error warning rate sharply increases, which produces the rise in $V_{DD(IU)}$ by 9mV. In Figs. 28.5.4 and 28.5.5, successful operations of the proposed adaptive V_{DD} control are demonstrated.

Finally, we consider the power characteristics of the proposed adaptive V_{DD} control using PEPD and DLDO. In conventional worst-case design, the worst case (=highest) $V_{DD(IU)}$ is 560mV at 6MHz, as shown in Fig. 28.5.4 (b). Therefore, 560mV is applied to all dies in conventional worst-case design. Figure 28.5.6 (a) shows the measured power comparison between conventional worst-case design and the proposed adaptive $V_{DD(IU)}$ control with PEPD and DLDO in a typical die at 6MHz and 85°C. The power dissipation of the IU with the proposed adaptive V_{DD} control is reduced by 38% compared with conventional worst-case design. As shown in Fig. 28.5.6 (b), the power and gate overheads of the proposed adaptive V_{DD} control are 7.9% and 12.5%, respectively. When the LDO switch loss is included, 13% power reduction was achieved. Figure 28.5.7 shows a die micrograph in 40nm CMOS and a performance summary.

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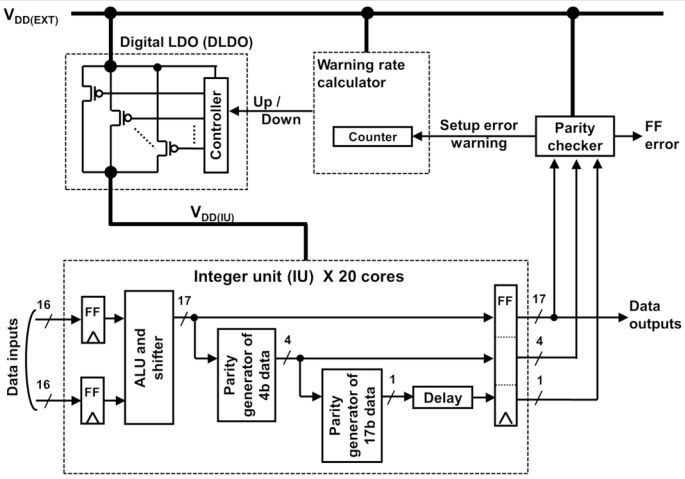


Figure 28.5.1: Block diagram of a proposed adaptive supply voltage control based on setup error prediction.

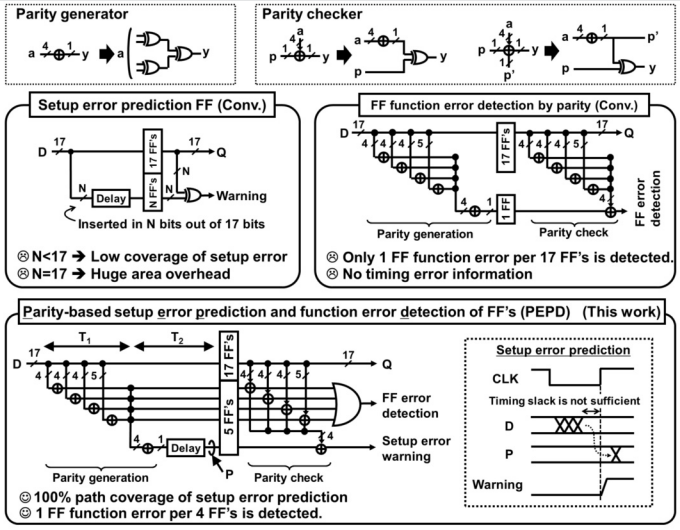


Figure 28.5.2: Proposed parity-based setup error prediction and function error of FF's (PEPD).

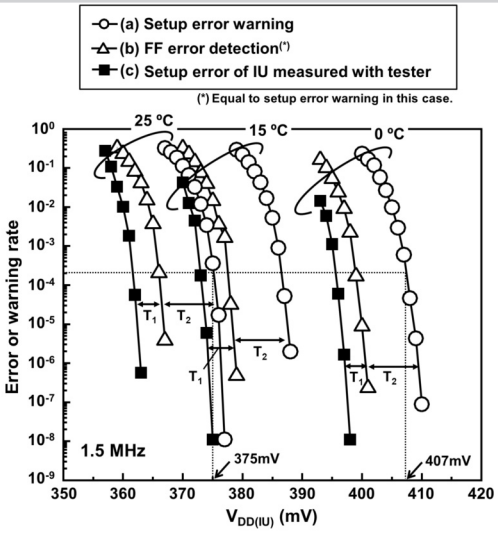


Figure 28.5.3: Measured dependence of error or warning rate of integer unit (IU) on $V_{DD(IU)}$ at 1.5MHz and 0°C, 15°C, and 25°C.

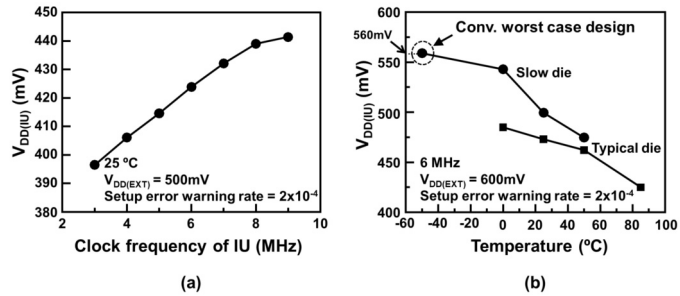


Figure 28.5.4: Measured adaptive $V_{DD(IU)}$ control with on-chip digital LDO at fixed setup error warning rate.

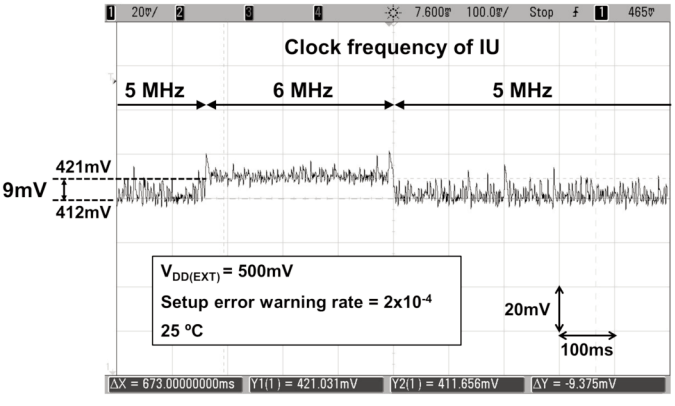
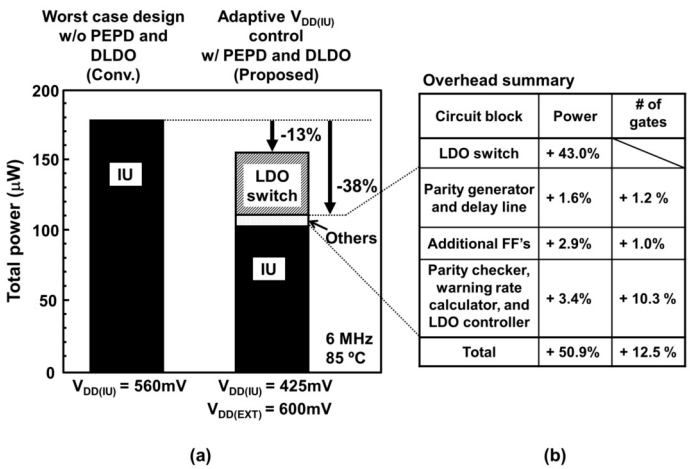


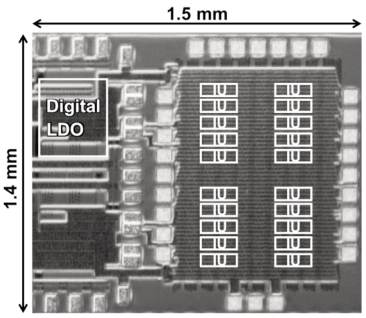
Figure 28.5.5: Measured adaptively-controlled $V_{DD(IU)}$ waveform at different clock frequencies of IU in Fig. 28.5.4 (a).



Overhead summary

Circuit block	Power	# of gates
LDO switch	+ 43.0%	
Parity generator and delay line	+ 1.6%	+ 1.2 %
Additional FF's	+ 2.9%	+ 1.0%
Parity checker, warning rate calculator, and LDO controller	+ 3.4%	+ 10.3 %
Total	+ 50.9%	+ 12.5 %

Figure 28.5.6: (a) Measured power comparison in typical die. (b) Overhead summary.



Technology	40nm CMOS
Core circuits	16-bit integer unit x 20 cores
$V_{DD(EXT)}$	500mV – 600mV
$V_{DD(IU)}$	390mV – 580mV
Power of IU (25 °C)	100μW @ 9MHz 63μW @ 6MHz 30μW @ 3MHz

Figure 28.5.7: Die micrograph and summary.

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