# 315MHz OOK Transceiver with 38-μW Receiver and 36-μW Transmitter in 40-nm CMOS

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***Abstract* – A 1-Mbps, 315MHz OOK transceiver in 40-nm CMOS for body area networks is developed. Both a 38-pJ/bit carrier-frequency-free intermittent sampling receiver with -55dBm sensitivity and a 36-pJ/bit transmitter applied dual supply voltage scheme with -20dBm output power achieve the lowest energy in the published transceivers for wireless sensor networks.**

## I Introduction

A low power 315MHz band (ARIB STD-T93) OOK transceiver for short-range wireless sensor networks is developed in this paper. The target receiver (RX) sensitivity and transmitter (TX) output power is -55dBm and -20dBm, respectively, assuming -25dB propagation loss at the 1-m communication distance and -5dB x 2 loss at TX/RX antennas. The target power consumption is 50μW at 1Mbps. In order to reduce the power, (1) sampling circuits are used instead of continuous analog circuits, (2) the RX input is directly sampled without LNA, because high sensitivity is not required for the 1-m communication, (3) a carrier-frequency-free (CFF) intermittent sampling (IS) is newly proposed to reduce the number of sampling, (4) a dual supply voltage ($V_{DD}$) scheme is newly proposed to increase the efficiency of a low output power ($P_{OUT}$) TX. The newly proposed IS [1] and dual $V_{DD}$ scheme [2] reduce the power of the transceiver to 1/315 and 2/3, respectively.

## II Carrier-Frequency-Free Intermittent Sampling Receiver

A conventional continuous sampling and the proposed IS concept for RX are compared in Fig. 1. The proposed IS reduces the number of the sampling in 1 symbol in order to reduce the power consumption of the sampler. Fig. 2 shows a block diagram of the proposed all 0.5V CFF IS RX. Only 1-MHz clock instead of a 315-MHz carrier frequency is supplied to RX. RX input ($V_{IN}$) is directly sampled by intermittent samplers without LNA. $V_{IN}$ is sampled by quadrature 315-MHz clocks ($\phi_0$, $\phi_{90}$, $\phi_{180}$, and $\phi_{270}$). The timing difference of $\Delta T$ is generated by digitally controlled delay lines instead of a conventional quadrature 315-MHz PLL, thereby reducing the power consumption. In the 315-MHz, 1-Mbps CFF IS RX, the number of sampling of $V_{IN}$ per bit is 4, while that of the conventional continuous sampling is 4x315, thereby reducing the power consumption of the sampler to 1/315. By the clock of $\phi_{HPF}$, the sampled $V_{IN}$'s are subtracted for a high pass filter function in order to increase the RX sensitivity by 3dB. The outputs of the samplers ( $V_1$, $\overline{V_1}$, $V_2$, and $\overline{V_2}$ ) are amplified by 5-stage IF amplifiers with an offset cancellation. Then, the outputs of the amplifiers ($V_{2A}$) are compared by proposed variable offset comparators clocked by $\phi_{CMP}$, and the data is demodulated. $V_{2A}$ is not constant, because the DC component is eliminated in the offset cancel amplifier.

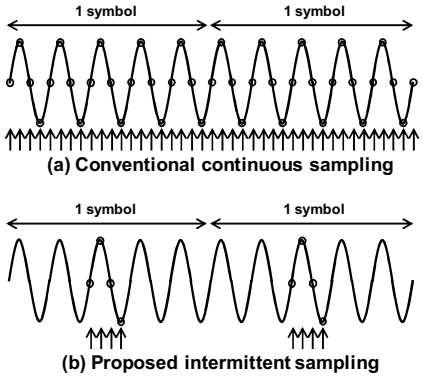


Fig. 1. Proposed intermittent sampling concept.

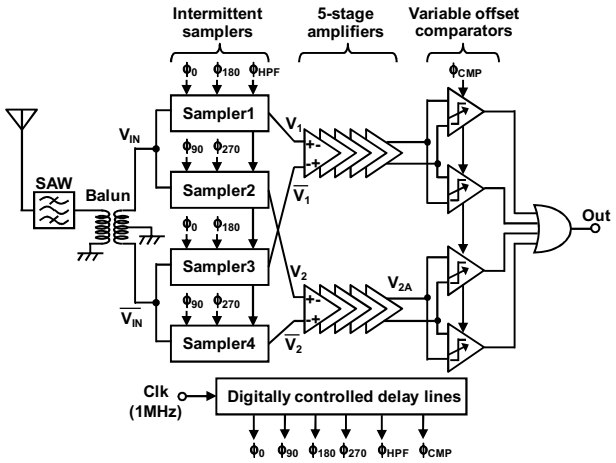


Fig. 2. Block diagram of proposed all 0.5V carrier-frequency-free intermittent sampling RX.

## III Transmitter with Dual $V_{DD}$ Class-F Power Amplifier

A dual $V_{DD}$ scheme is proposed to maximize global efficiency (GE) of TX at $P_{OUT}$ of -20dBm in this section. Fig. 3 shows a schematic of TX including the dual $V_{DD}$ class-F PA. As shown in Fig. 3, $P_{TOTAL}$ is the sum of the buffer, the mixer, and the PA powers. In the TX design with $P_{OUT}$ of -20dBm, the buffer power is not negligible and the drain efficiency (DE) of PA is quite low because the impedance transformation ratio (n) and the loss are much higher than conventional PA's designs ($P_{OUT}$: 10~30dBm). Therefore, GE should be maximized at $P_{OUT}$ of -20dBm by optimizing n. In the design

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optimization, $V_{DD1}$, $V_{DD2}$, $C_{DC}$, and $L_{DC}$ are varied according to n, and $L_1$, $C_1$, $L_3$, $C_3$, and transistor size are fixed.

Fig. 4 shows the SPICE simulated n dependence in TX with $P_{OUT}$ of -20dBm. Fig. 5 shows the simulated dependence of $P_{TOTAL}$, the buffer power, and the PA power on n. As shown in Fig. 4, the conventional TX with single $V_{DD}$ is designed at n = 9.6 and $V_{DD1}$ = $V_{DD2}$ = 0.47V. In contrast, $P_{TOTAL}$ is minimum at n = 4.2, thereby GE is maximum at n = 4.2. The corresponding $V_{DD1}$ = 0.56V and $V_{DD2}$ = 0.2V. The reason for the optimum dual $V_{DD}$ is discussed. When n is reduced from 10 to 2, $V_{DD2}$ is reduced and the PA power is reduced. In contrast, $V_{DD1}$ is increased and the buffer power is increased. When n is reduced below 3, $V_{DD1}$ drastically increases because the transistor operation changes from the saturation region to the linear region, thereby the corresponding buffer power drastically increases. Therefore, $P_{TOTAL}$ is minimum at n = 4.2, thereby GE is maximum at n = 4.2 [2].

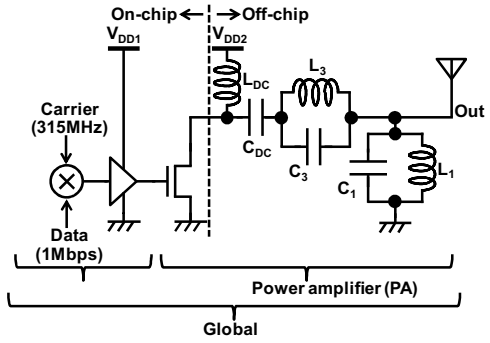


Fig. 3. Schematic of dual $V_{DD}$ TX with class-F PA.

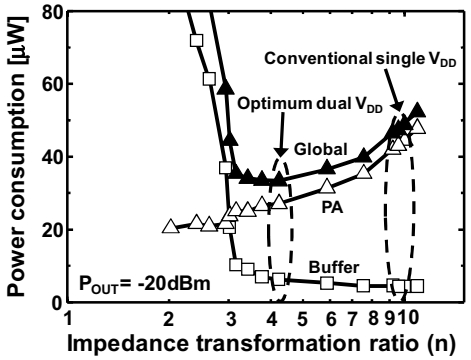


Fig. 4. SPICE simulated impedance transformation ratio dependence in TX with $P_{OUT}$ of -20dBm.

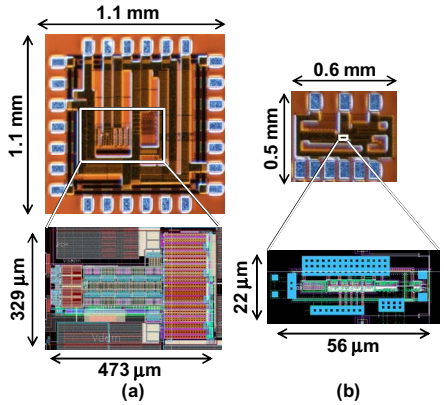


Fig. 5. Die microphotograph and layout of (a) RX and (b) TX.

Table I Performance summary and comparison

| | | Unit | [3] | [4] | This work |
|---|---|---|---|---|---|
| CMOS technology | | nm | 90 | 130 | 40 |
| Supply voltage | RX | V | 1, 1.2 | - | 0.5 |
| | TX | V | 1, 1.2 | 1 | 0.52, 0.2 |
| Carrier frequency | | MHz | 2400 | 400 | 315 |
| Data rate | | Mbps | 5 | 0.2 | 1 |
| Modulation | | - | OOK | FSK | OOK |
| RX sensitivity | | dBm | -75 | - | -55 |
| TX output power | | dBm | 0 | -17 | -20 |
| Power | RX | μW | 534 | - | 38 |
| | TX | μW | 253 | 90 | 36 |
| Energy | RX | pJ/bit | 134 | - | 38 |
| | TX | pJ/bit | 2530 | 450 | 36 |

## IV. Measurement Results

The proposed transceiver is fabricated in 40-nm CMOS process. Fig. 5 shows a die photo and layout of RX and TX. Table I shows a measured performance summary and comparison of performance with published transceivers for wireless sensor networks [3-4]. Thanks to the proposed IS, the power consumption of the samplers in RX is 3μW and the total RX consumes 38 μW. Without IS, the continuous sampler will consume 945μW (=3μW x 315). The TX efficiency (GE) increases from 16% to 28% due to the dual $V_{DD}$ scheme. Both the 38-pJ/bit CFF IS RX and the 36-pJ/bit dual $V_{DD}$ TX achieve the lowest energy to date.

## V. Conclusion

A low power OOK transceiver for short-range wireless sensor networks is developed in this paper. In order to reduce the power, CFF IS and dual $V_{DD}$ scheme are newly proposed. The newly proposed IS and dual $V_{DD}$ scheme reduce the power of the RX and TX to 1/315 and 2/3, respectively. Both the 38-pJ/bit CFF IS RX and the 36-pJ/bit dual $V_{DD}$ TX achieved the lowest energy to date.

## Acknowledgments

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## References

[1] A. Saito, K. Honda, Y. Zheng, S. Iguchi, K. Watanabe, T. Sakurai, and M. Takamiya, "An All 0.5V, 1Mbps, 315MHz OOK Transceiver with 38-μW Carrier-Frequency-Free Intermittent Sampling Receiver and 52-μW Class-F Transmitter in 40-nm CMOS," IEEE Symposium on VLSI Circuits, pp. 38-39, June 2012.

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