Insole Pedometer With Piezoelectric Energy Harvester and 2 V Organic Circuits

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***Abstract*—A shoe insole pedometer, which consists of a piezoelectric energy harvester and a 2 V organic pedometer circuit, has been developed as a first step toward the application of flexible large-area energy harvesting. A pseudo-CMOS 14 bit step counter records the number of steps up to 16383 steps using the harvested power. To increase the noise margin of the pseudo-CMOS logic circuits, a negative voltage is generated by an organic charge pump circuit and is applied to the pseudo-CMOS inverters and transmission gates in the flip-flops in the step counter. A pseudo-CMOS Schmitt trigger inverter used to feed clean square pulses to the step counter is presented. This paper describes the details of the insole pedometer and provides measurement results and some discussion.**

***Index Terms*—Charge pump, energy harvesting, organic large-area electronics, piezoelectric film, pseudo-CMOS, PVDF.**

I. Introduction

ENERGY harvesting is an enabling technology for realizing an ambient power supply for wireless sensor nodes and mobile devices. Using flexible photovoltaic cells and piezoelectric films, we can readily harvest ambient energy if flexible energy harvesters can be realized. This type of integration will broaden the range of applications of flexible, large-area electronics.

Conventional silicon circuits, however, are not the best candidates for realizing flexible large-area energy harvesters because they are mechanically hard, and therefore difficult to fit to curved surfaces such as shoes. In energy-harvesting applications, the harvested power is small and the voltage is low (e.g., 2 V) owing to the limited capability of harvesters. Organic circuits typically consume less power, since their operation speed is low. In addition, self-aligned monolayer (SAM) technology [1] realizing 2 V operation is available. Organic circuits are therefore suitable for energy-harvesting applications.

The stable pMOS semiconductor material DNTT [2] can be used in organic circuits. However, the mobility of organic nMOS transistors is almost one order of magnitude smaller than that of pMOS transistors in our current technology. In organic circuit design, all-pMOS circuits are often used. A pseudo-CMOS inverter, one of the all-pMOS circuits, has been proposed [3]. The output transistors in the pseudo-CMOS inverter operate complementarily. The pseudo-CMOS inverter, therefore, has high gain, but it requires a negative voltage bias. The operation of all-pMOS circuits without a negative voltage bias is not robust, and the noise margin is small because of their rationed-logic nature. Thus, the main challenge in the design of organic circuits for piezoelectric energy harvesting is the robust operation (e.g., the signal integrity in counters) of all-pMOS circuits at a low supply voltage.

To address this challenge, we have proposed an organic insole pedometer with a piezoelectric energy harvester as the first step toward ambient energy harvesting using organic electronics [4]. To increase the noise margin of all-pMOS logic circuits based on pseudo-CMOS inverters, a negative voltage is generated by an organic charge pump circuit and applied as the bias of pseudo-CMOS inverters. A pseudo-CMOS Schmitt trigger inverter used to feed clean square pulses to the logic circuits is also proposed. This paper describes the details of the insole pedometer and provides measurement results and some discussion. In Section II, we give an overview of the proposed insole pedometer. In Section III, we give a detailed description of the circuit design. In Section IV, we present the experimental results and discussion. Finally, conclusions are given in Section V.

II. Overview of Insole Pedometer

Fig. 1 shows an outline of the proposed insole pedometer. A polyvinylidene difluoride (PVDF) sheet is used as a piezoelectric energy harvester. Since the output current of the harvester is proportional to its area, the sheet is cut into small pieces and rolled to increase the total area. One of the PVDF rolls is used for pulse generation to detect steps. Each time the insole is pressed by the foot during walking, the PVDF roll generates a pulse. The

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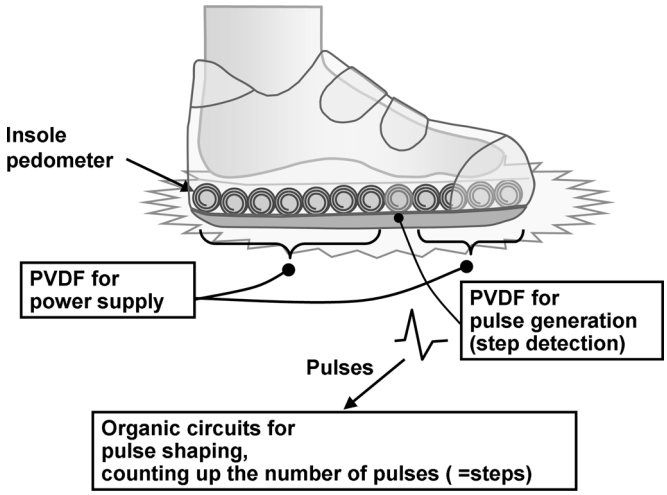

Fig. 1. Outline of the proposed insole pedometer.

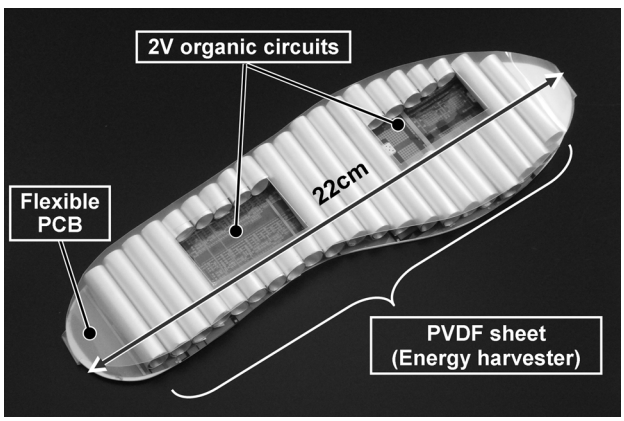

Fig. 2. Photograph of the prototype insole pedometer.

remaining PVDF rolls are used in the power supply for the organic circuits. The organic circuits are implemented with a 2 V pMOS process and are located under the array of PVDF rolls to shape the detected pulses into clean square waves and count the number of steps.

Fig. 2 shows a photograph of the prototype insole pedometer, including the piezoelectric energy harvester and 2 V organic circuits. Twenty-one PVDF rolls are embedded on the plastic baseboard. To show the organic circuits under the rolls, two rectangular areas have been cut out. The 2 V organic circuits are implemented separately and connected to each other by a flexible PCB. The total length of the pedometer is 22 cm.

A block diagram of the insole pedometer is shown in Fig. 3. The system consists of four circuit blocks. An all-pMOS full-wave rectifier supplies a voltage V_{DD} of approximately 2 V to all circuit blocks. The output current is approximately 10 μA. The pulse-shaping circuit, which consists of a pseudo-CMOS Schmitt trigger inverter, shapes the pulses obtained by the PVDF roll into clean square waves and feeds them to both the all-pMOS negative voltage generator and a 14 bit pseudo-CMOS step counter with gate-boosted pMOS switches. The pseudo-CMOS 14 bit step counter records the number of steps up to 16383 steps using the harvested power. To increase the noise margin of the pseudo-CMOS logic

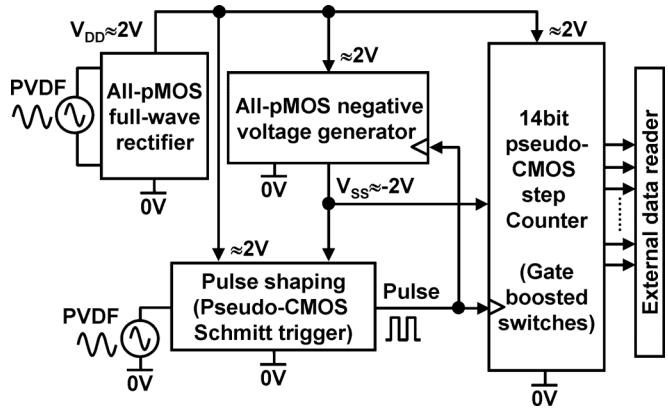

Fig. 3. Block diagram of the insole pedometer.

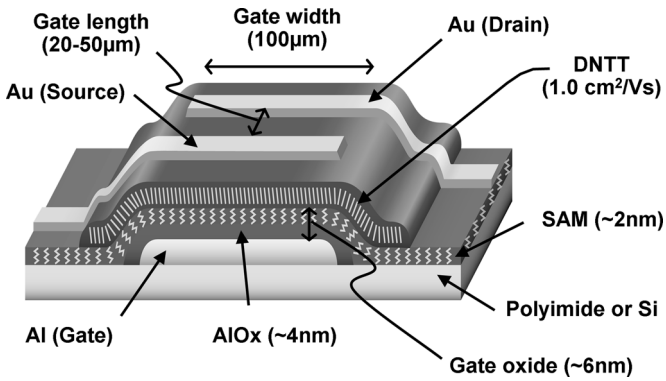

Fig. 4. Device structure of the 2 V organic pMOS transistor.

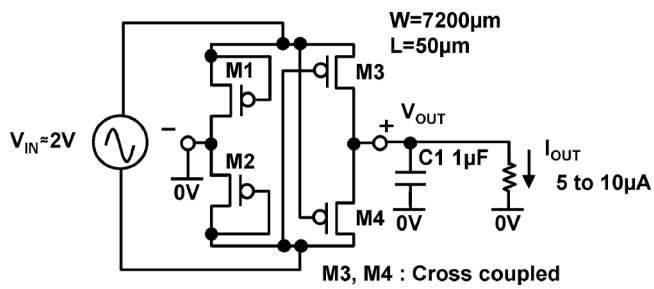

Fig. 5. Schematic of the all-PMOS full-wave rectifier.

circuits, the all-pMOS negative voltage generator provides a voltage V_{SS} (e.g., -2 V) to the pseudo-CMOS inverters and transmission gates in the flip-flops in the step counter. The circuit design of each building block is discussed in Section III.

In this work, we use an organic pMOS process with SAM technology and the semiconductor material DNTT as shown in Fig. 4. SAM technology enables a total gate oxide thickness of 6 nm and 2 V operation. DNTT is a stable material with a high mobility of 1.0 $\mathrm{cm}^2/\mathrm{Vs}$. The minimum gate length is 20 μm in the negative voltage generator and 50 μm in other circuit blocks.

III. Circuit Design

A. All-pMOS Full-Wave Rectifier

Fig. 5 shows a schematic of the all-pMOS full-wave rectifier, which was presented in our previous work [5]. In the left branch,

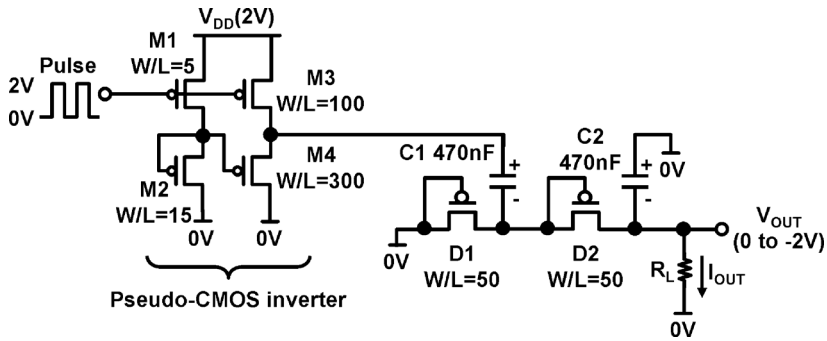

Fig. 6. Schematic of the proposed all-PMOS negative voltage generator.

diode-connected pMOS transistors (M1, M2) are used. On the other hand, the right branch consists of a pair of cross-coupled pMOS transistors (M3, M4) to increase the output current [5]. The maximum target output voltage is 2 V with a maximum output current of 10 μA, while the rectifier in [5] supplies a 20 V, 2 mA output. Their gate width W and length L are 7200 μm and 50 μm, respectively. Although the minimum gate length of 20 μm is better for obtaining high driving capability, a gate length of 50 μm instead of 20 μm is chosen here in consideration of the process yield.

B. All-pMOS Negative Voltage Generator

An organic Dickson-type DC to DC converter was presented in [6]. The converter in [6] handles an output current of 10 nA, while our negative voltage generator provides 10 μA. Furthermore, our voltage generator must operate at a low frequency (e.g., from 1 to 10 Hz). We, therefore employ 470 nF MIM capacitors for the charge pump circuit. To switch these large capacitors with a high on/off ratio, a high-gain pseudo-CMOS inverter and two diode-connected depletion pMOS transistors are used as shown in Fig. 6.

To charge/discharge the left capacitor (C1), the output buffer of the pseudo-CMOS inverter consists of transistors with widths of 2 mm ($\mathrm{W/L} = 100$) and 6 mm ($\mathrm{W/L} = 300$). The performance of the negative voltage generator strongly depends on the threshold voltage of the pMOS diode-connected transistors. To reduce the reverse leakage current, the gate width of each diode-connected transistor is smaller ($\mathrm{W/L} = 50$) than that of the inverter. These parameters are carefully determined through a SPICE simulation.

C. Pulse-Shaping Circuit (Pseudo-CMOS Schmitt Trigger Inverter)

To generate clean square waves from the noisy input pulses obtained by the PVDF energy harvester, a Schmitt trigger inverter is required as shown in Fig. 7. Here, a Schmitt trigger inverter based on pseudo-CMOS logic is proposed. Fig. 8 shows a schematic of the proposed Schmitt trigger inverter and its DC output characteristics obtained by SPICE simulation. Unlike conventional CMOS Schmitt trigger inverters, which can use both pMOS and nMOS transistors to generate hysteresis, in the proposed pseudo-CMOS Schmitt trigger inverter, the first

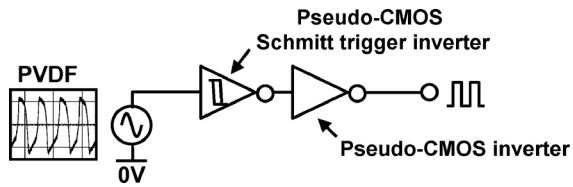

Fig. 7. Schematic of the pulse-shaping circuit.

stage is used to adjust the lower-bound ($\mathrm{VM}-$) of the hysteresis, while the second stage is used to adjust the upper-bound ($\mathrm{VM}+$).

When the input signal is swept from low to high, the top pMOS transistor of the second stage (M1), which is controlled by the third-stage pseudo-CMOS inverter output (A), pulls up the voltage of node (B), and therefore moves the high-to-low switching point to the right, as can be seen in Fig. 8(c). The upper-bound transition point is determined by the ratio of M1 to M2. On the other hand, when the input is swept from high to low, the ground-connected pMOS transistor (M3) of the first stage weakens the pull-up force of the top two pMOS transistors (M4, M5), which forces the low-to-high switching point to move to the left and widens the hysteresis, as shown in Fig. 8(c). The lower-bound transition point is determined by the ratio of M3 to M6.

D. 14 bit Pseudo-CMOS Step Counter

To count the number of steps taken while walking, we designed a pseudo-CMOS binary counter. The counter employs gate-boosted pMOS switches (M1-M4), while our previous counter in [5] employs CMOS transmission gates. Fig. 9(a) shows a schematic of a single-stage 2 V pseudo-CMOS binary counter with asynchronous reset. By connecting fourteen such stages, we can build a 14 bit binary counter for the proposed pedometer. On the basis of a divide-by-two frequency divider, a new gate-boosting technique is applied in this counter to compensate for the poor conductivity of the pMOS switches for the signal around the $\mathrm{V_{SS}}$ level. By employing a level-shifted clock buffer, as shown in Fig. 9(b), we can effectively overdrive pMOS switches by applying negative voltages though the $\mathrm{V_{SS}}$ terminal in the clock buffer.

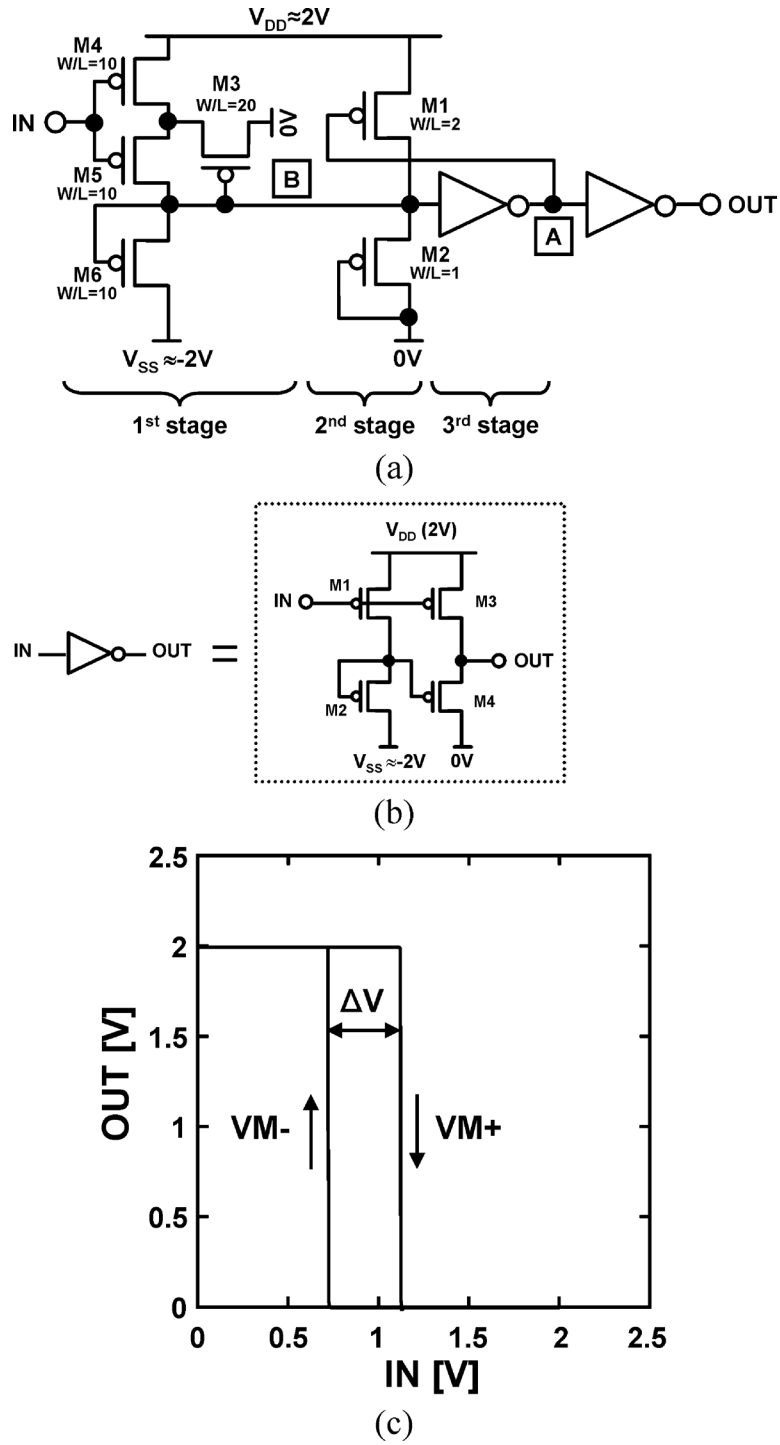

Fig. 8. All-pMOS negative voltage generator. (a) Overall schematic. (b) Schematic of pseudo-CMOS inverter. (c) DC characteristics of the Schmitt trigger inverter obtained by SPICE simulation.

IV. Measurement Results and Discussion

A. All-pMOS Full-Wave Rectifier

The proposed all-pMOS full-wave rectifier is fabricated by a 2 V organic pMOS process. Fig. 10(a) shows a chip photograph of the proposed full-wave rectifier. The chip area is $13.8 \times 24.9\ \mathrm{mm}^2$. Fig. 11 shows the measured waveform of the 2 V full-wave rectifier without a smoothing capacitor (C1 in Fig. 5); the output current is less than 1 μA. The input signal (V_{IN}) is a 4 V peak-to-peak sinusoidal wave. To clearly show the rectified waveform, we choose 1 Hz as the input frequency. Full-wave rectified waveforms (V_{OUT}) are clearly observed. The output frequency is 2 Hz, and the amplitude of the rectifier is approximately 2 V peak-to-peak when 1 Hz, 4 V peak-to-peak sinusoidal input signals are applied. Fig. 12 shows the measured output voltage versus the output current of the rectifier with a 1 μF smoothing capacitor. The proposed all-pMOS rectifier provides up to 12 μW power with 59% power efficiency. Fig. 13

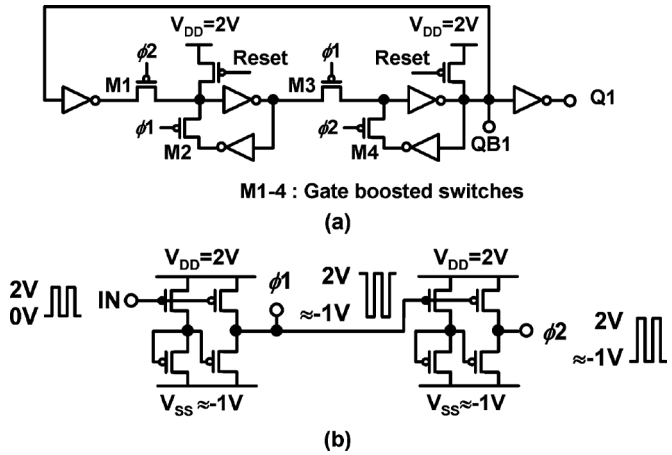

Fig. 9. Schematics of a single-stage 2 V pseudo-CMOS binary counter with asynchronous reset. (a) Binary counter. (b) Level-shifted clock buffer.

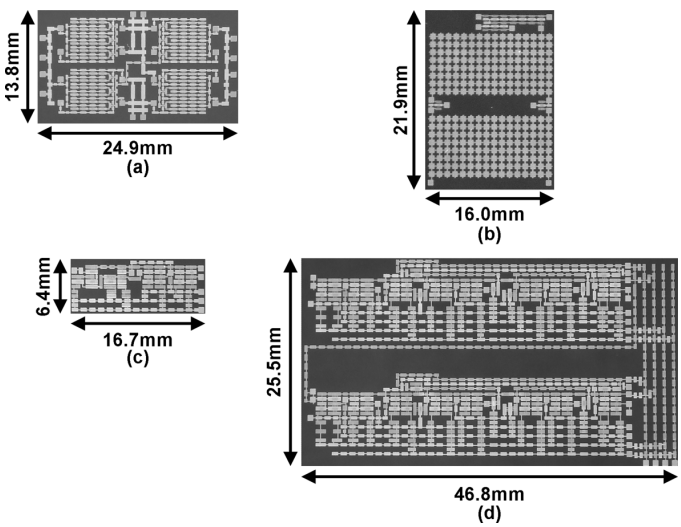

Fig. 10. Chip photographs. (a) Full-wave rectifier. (b) Negative voltage generator. (c) Pseudo-CMOS Schmitt trigger inverter. (d) 2 bit pseudo-CMOS step counter.

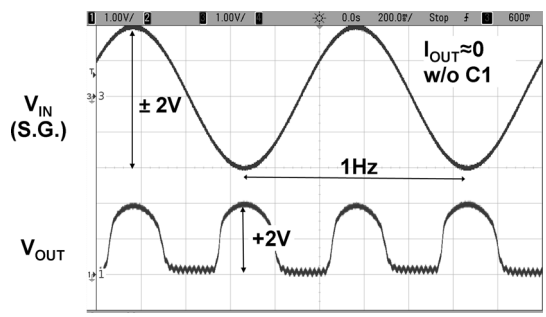

Fig. 11. Measured waveform of the 2 V full-wave rectifier without a smoothing capacitor.

shows the measured waveforms of the $20 \times 28\ \mathrm{cm}^2$ sheet of the PVDF energy harvester and the rectified output. Here, the harvester is pressed by hands and the frequency is approximately 4 Hz, which is intended to be a typical operation speed of the pedometer. The 1 μF smoothing capacitor can be charged by providing a mechanical force to the PVDF energy harvester. The output voltage is approximately 1.3 V with a current of 8 μA.

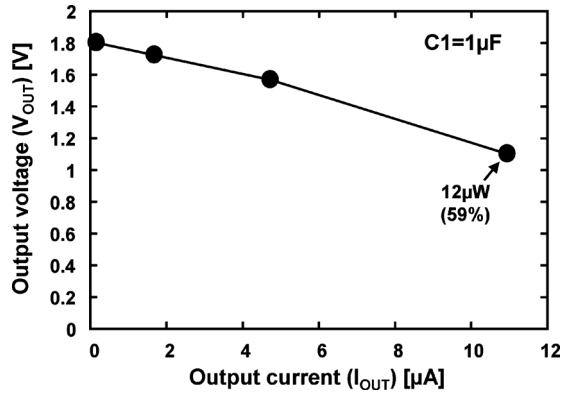

Fig. 12. Measured output voltage versus the output current of the rectifier with a 1 μF smoothing capacitor.

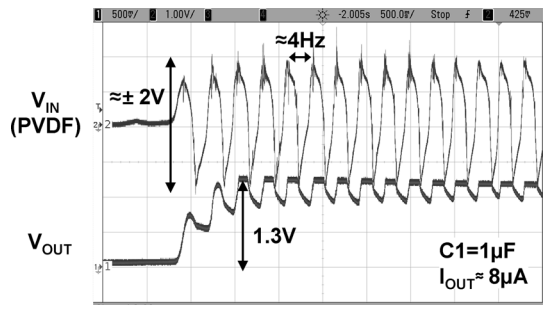

Fig. 13. Measured waveforms of $20 \times 28\ \mathrm{cm}^2$ sheet of the PVDF energy harvester and the rectified output.

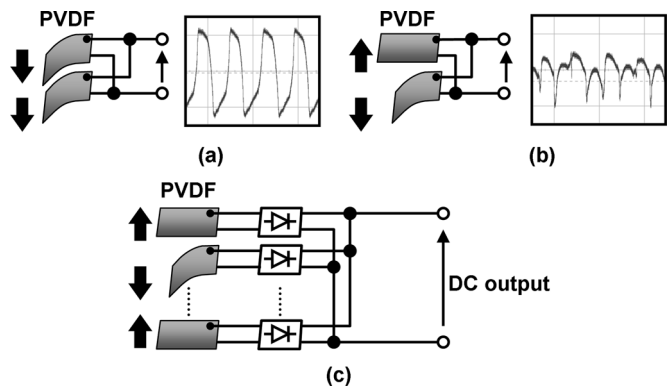

Fig. 14. Optimization of the output voltage of the PVDF sheet. (a) In-phase operation of parallel PVDF harvesters. (b) Ant phase operation. (c) Implementation with distributed rectifiers. (a) In-phase. (b) Anti-phase. (c) Implementation with distributed rectifiers.

The maximum conversion efficiency of the rectifier is 59%, which is an acceptable performance for the insole pedometer. However, if the conversion efficiency of the energy harvester can be improved, its range of applications will be wider. In this implementation, twenty-one PBDF rolls are set in parallel, and only one large rectifier is used for simplicity. When each PVDF sheet is pressed at the same time, the output voltage is maximized as shown in Fig. 14(a). In contrast, in the case of an anti phase, the PVDF outputs mutually conflict and the voltage is canceled out as shown in Fig. 14(b). To avoid such conflict, the rectifiers should be distributed in a certain area as shown in

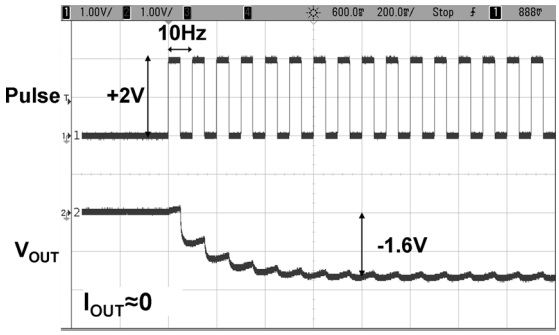

Fig. 15. Measured waveforms of the negative voltage generator.

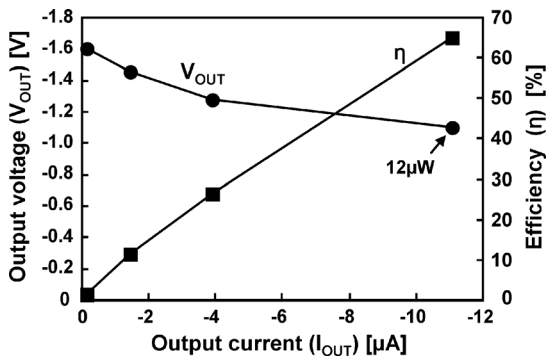

Fig. 16. Measured output voltage versus the output current of the negative voltage generator.

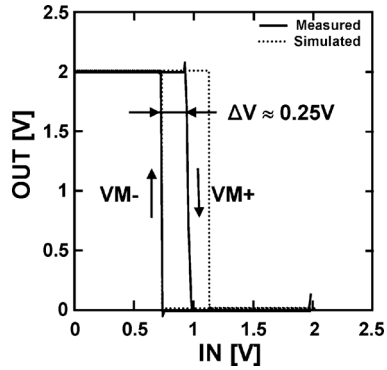

Fig. 17. Measured DC characteristic of the pseudo-CMOS Schmitt trigger inverter.

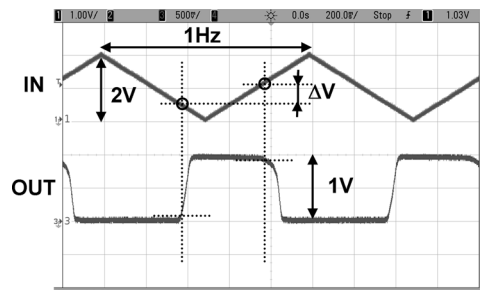

Fig. 18. Measured waveforms of the pseudo-CMOS Schmitt trigger inverter.

Fig. 14(c). In addition, low-cost, large-area organic electronics are suitable for implementing distributed rectifiers.

B. All-pMOS Negative Voltage Generator

Fig. 10(b) shows a chip photograph of the negative voltage generator. The chip area is $21.9 \times 16.0\ \mathrm{mm}^2$. Two 470 nF MIM capacitors (C1 and C2 in Fig. 6) occupy most of the chip area. The measured waveforms and output voltage versus the output current are shown in Figs. 15 and 16, respectively. An input frequency of 10 Hz is chosen to show the maximum output power and the power efficiency at the highest operation speed of the pedometer. The output voltage ($\mathrm{V_{OUT}}$) of the negative voltage generator is -1.6 V in the case of 10 Hz square pulses. Thanks to the pseudo-CMOS-inverter-based switches, the proposed negative voltage generator provides a maximum power of 12 μW with 65% power efficiency.

C. Pulse Shaping (Pseudo-CMOS Schmitt Trigger Inverter)

Fig. 10(c) shows chip a photograph of the pseudo-CMOS Schmitt trigger inverter. The chip area is $6.4 \times 16.7\ \mathrm{mm}^2$. On the basis of the measured DC characteristic in Fig. 17, we find that the switching points for the high-to-low and low-to-high transients have a difference of approximately 0.25 V (ΔV in Fig. 17); this characteristic plays a key role in supplying clean clock signals to the counter. Fig. 18 shows the measured waveform of the pseudo-CMOS Schmitt trigger inverter. The PVDF output is emulated with a 2 V peak-to-peak triangular wave. The frequency is 1 Hz to clearly show the hysteresis characteristics. The measured hysteresis characteristic is clearly observed with the 1 Hz triangular wave input.

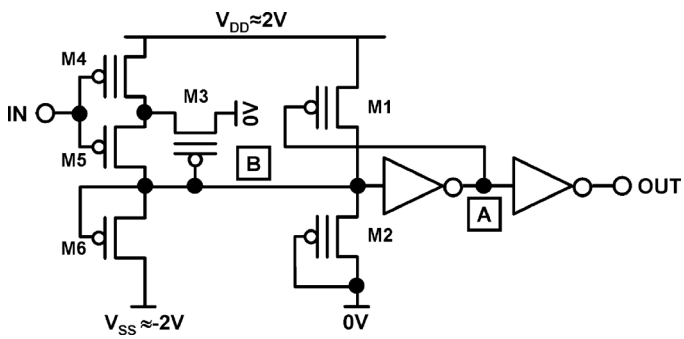

Fig. 19. Schematic of the pseudo-CMOS Schmitt trigger inverter with floating gates.

For the lower-bound transition point in Fig. 17, the measurement result closely agrees with the simulation result (dashed line). On the other hand, the measured upper-bound transition point is lower than the simulated result by approximately 0.15 V. This difference originates from the variation of $\mathrm{V_{TH}}$ in M1 and M2 in Fig. 8. When the variation is critical, a $\mathrm{V_{TH}}$ compensation scheme based on the floating-gate programming [7] is also effective for the Schmitt trigger inverter. In such a case, M1 to M4 should be implemented with a floating-gate layer as shown in Fig. 19. SPICE simulation results for the compensation are shown in Fig. 20. When the $\mathrm{V_{TH}}$ of M1 is increased by floating-gate programming, the upper-bound transition point ($\mathrm{VM+}$) is shifted to the left as shown in Fig. 20(a). On the other hand, the lower-bound transition point is stable. When the $\mathrm{V_{TH}}$ of M2 is increased, $\mathrm{VM+}$ is moved to the right as shown in Fig. 20(b). In M3 and M4, both the upper-bound

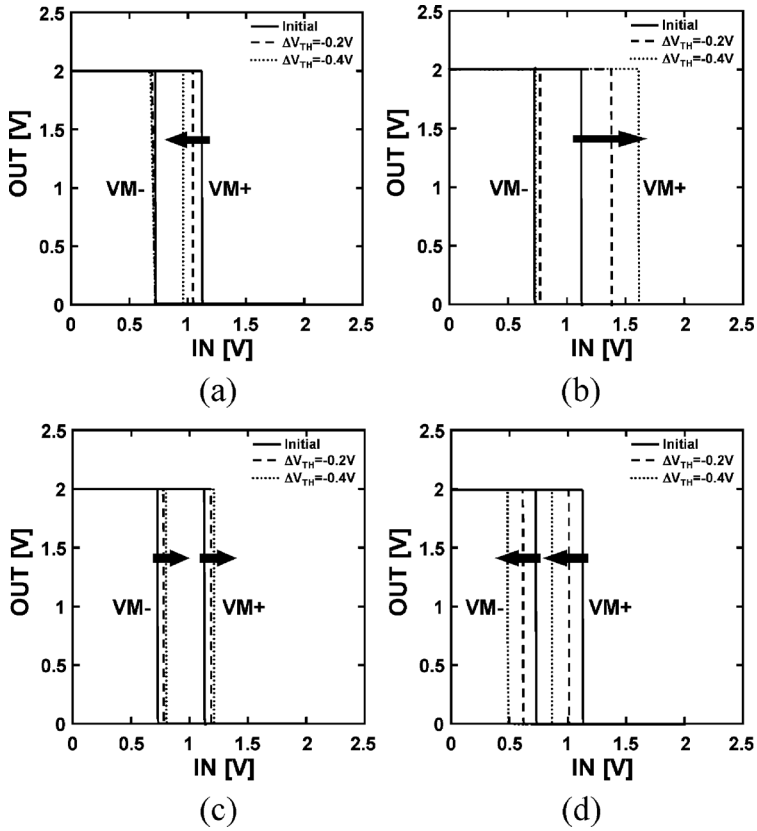

Fig. 20. Simulation results of V_{TH} programming. (a) M1. (b) M2. (c) M3. (d) M4.

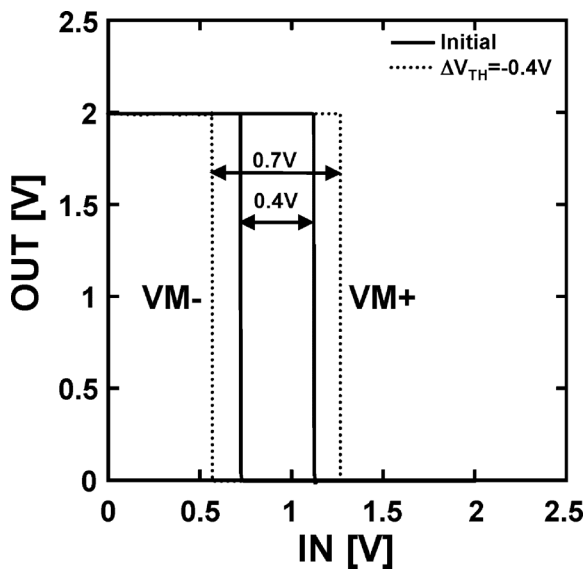

Fig. 21. Simulation results of the enhancement of hysteresis by programming M2 and M4.

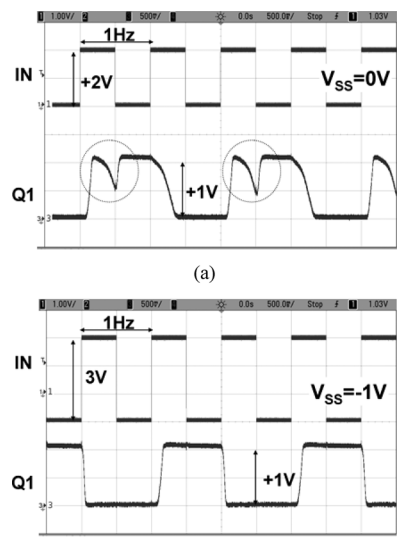

Fig. 22. Measured waveforms of the step counter. (a) Without gate boosting. (b) With gate boosting.

(VM+) and lower-bound (VM−) transitions are modified as shown in Fig. 20(c) and (d), respectively. This floating-gate programming can be used for not only compensation but also the improvement of hysteresis. For instance, by programming both M2 and M4, a wider hysteresis is realized as shown in Fig. 21.

D. 14 bit Pseudo-CMOS Step Counter

Fig. 10(d) shows a chip photograph of the pseudo-CMOS step counter. Note that only two stages are shown in the photograph and the chip area is $25.5 \times 46.8\ \mathrm{mm}^2$.

Fig. 22 shows measured waveforms of the single-stage step counter. The frequency of the input (IN) is 1 Hz to clearly show the signal integrity. The waveform in Fig. 22(a) is for operation

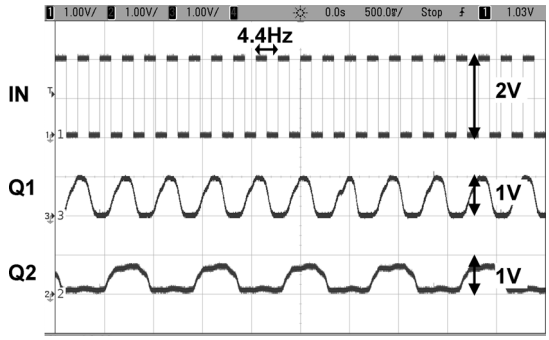

Fig. 23. Measured waveforms of 2 bit step counter.

TABLE I
KEY FEATURES AND PERFORMANCE SUMMARY.

Organic transistors	
Semiconductor material	DNTT(1.0 cm^2/Vs)
Gate oxide material, thickness	SAM 2nm + AlO_X 4nm = 6nm
Minimum gate length	20μm (analog), 50μm (digital)
Energy harvester and pedometer	
Harvester	Piezoelectric energy harvester (PDFV)
Number of transistors	462Tr.
Pedometer size	22x7cm^2

without the gate-boosting technique. Owing to the poor driving capability of the pMOS switches without gate boosting, large dips are observed. Using the gate-boosting technique, the signal integrity of Q1 in Fig. 22(b) is greatly improved and robust operation is achieved. Note that Fig. 22 only shows the signals from output Q1, while QB1 in Fig. 9(a) is used for connecting to the next stage of the binary counter. Fig. 23 shows the measured waveform of the 2 bit step counter. The frequency of the input pulses is 4.4 Hz, which is the maximum measured operation speed of the counter. Although each output swing is slightly degraded, the pseudo-CMOS step counter successfully operates at 4.4 Hz, that is, the counter can handle up to four steps per second.

Table I gives the key features and a performance summary of the proposed insole pedometer. The pedometer consists of 462 transistors and its total area is $22 \times 7\ \mathrm{cm}^2$.

V. CONCLUSIONS

A shoe insole pedometer, which consists of a piezoelectric energy harvester and a 2 V organic pedometer circuit, has been developed as a first step toward the application of flexible large-area energy harvesting. Its feasibility is demonstrated by measurement. A pseudo-CMOS 14 bit step counter records the number of steps up to 16383 steps using the harvested power. A negative voltage generator based on an organic charge pump circuit provides 12 μW power with 65% efficiency. A pseudo-CMOS Schmitt trigger inverter with a 0.25 V hysteresis is also proposed. The integration of organic circuits and flexible energy harvesters will broaden the rnge of applications of flexible, large-area electronics.

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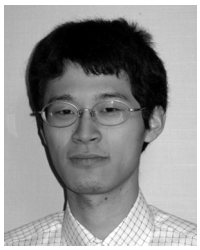

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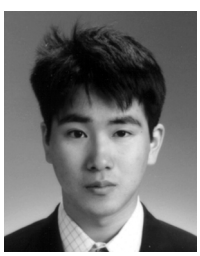

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