# A Low Voltage Buck DC-DC Converter Using On-Chip Gate Boost Technique in 40nm CMOS

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**Abstract - A low voltage buck DC-DC converter (0.45-V input, 0.4-V output) with on-chip gate boosted (OGB) and clock frequency scaled digital PWM controller is designed in 40-nm CMOS process. The highest efficiency to date is achieved at the output power less than 40μW. In order to compensate for the die-to-die delay variations of a delay line in the proposed digital PWM controller, a linear delay trimming by a logarithmic stress voltage (LSV) scheme with good controllability is also proposed and verified in measurement.**

## I Introduction

In modern low-power applications, digital circuits are working with near-threshold supply voltage ($V_{DD}$) to achieve energy efficient operation. Thus an adaptive $V_{DD}$ control with low voltage operation becomes of great importance. In [1], a low dropout regulator (LDO) is used for the adaptive $V_{DD}$ control. However, its efficiency is limited to less than $V_{OUT}$ (output voltage) /$V_{IN}$ (input voltage). To improve the efficiency, a buck DC-DC converter is developed in this paper [2].

Generally speaking, the efficiency of the buck converter with low $V_{IN}$ and $P_{OUT}$ is quite low, because (1) the loss in power transistors increases due to low $V_{IN}$ and (2) the controller power dominates the total power when $P_{OUT}$ is low. From simple calculation, it can be shown that to achieve more than 90% efficiency at $P_{OUT}$ of 2mW, the quiescent power required is less than 222nW. In order to achieve a high efficiency buck converter, this paper proposes (1) an on-chip gate boost (OGB) by fully integrated switched-capacitor (SC) DC-DC converters, (2) a low power clock frequency scaled 0.45-V digital PWM controller, and (3) a linear delay trimming by a novel logarithmic stress voltage (LSV) scheme to compensate for the die-to-die delay variations of a delay line in the PWM controller with good controllability.

## II. Implementation of Buck DC-DC Converter

### *A. On-Chip Gate Boost (OGB)*

Fig. 1 shows a block diagram of the proposed buck converter with OGB. Without OGB, driving voltages of the power transistors are low (=$V_{IN}$), thus the loss of the power transistors increases and the efficiency decreases. In order to reduce the on-resistance of the power transistors, a fully integrated $2V_{IN}$ (=double voltage) SC DC-DC converter for the nMOS power transistor ($M_N$) and a minus $V_{IN}$ SC DC-DC converter for the pMOS power transistor ($M_P$) are developed to boost the supply voltages for the gate drivers. The PWM signal (CK_PWM) is boosted to "$-V_{IN}$ to $V_{IN}$" and "0V to $2V_{IN}$", for $M_P$ and $M_N$, respectively.

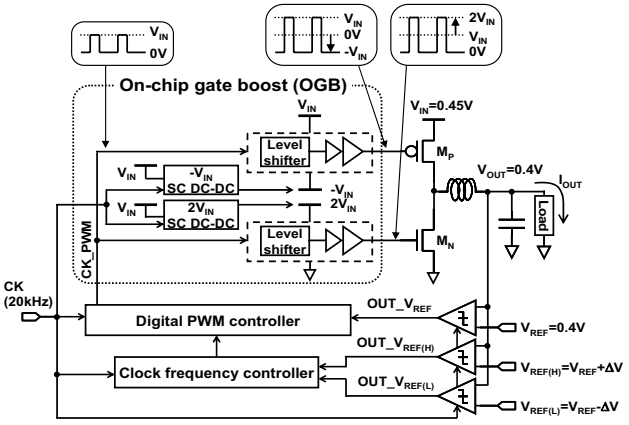


Fig. 1. Block diagram of proposed buck converter.

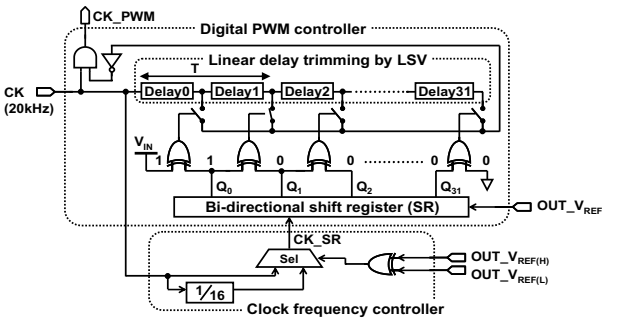


Fig. 2. Digital PWM controller and clock frequency controller.

### *B. Digital PWM Controller*

Fig. 2 shows a circuit schematic of a digital PWM controller and a clock frequency controller. Instead of a conventional analog feedback control, a delay-line based digital PWM controller is newly developed for 0.45-V operation. A clock frequency controller is also employed for power saving. Specifically, when $V_{OUT}$ is higher than the high reference voltage ($V_{REF(H)}$) or lower than the low reference voltage ($V_{REF(L)}$), the clock signal (CK) is given to SR; when $V_{OUT}$ is between $V_{REF(H)}$ and $V_{REF(L)}$, CK divided by 16 is given to SR, thereby reducing the controller power.

### *C. Delay Line Trimming by LSV*

In the digital PWM controller, a delay-line without feedback control is used to minimize the controller power. Therefore, there is a risk that PWM operation may fail due to large variations of the delay line. To compensate for the die-to-die variations, a delay trimming by a charge injection [3] is proposed. Fig. 3 shows a schematic of the trimmed

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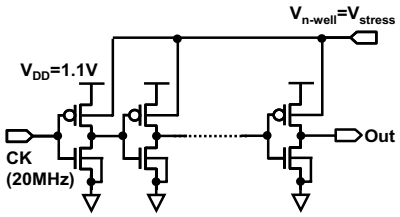



Fig. 3. Trimmed delay line with charge injection.

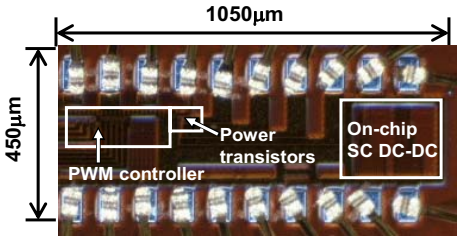



Fig. 4. Chip micrograph.

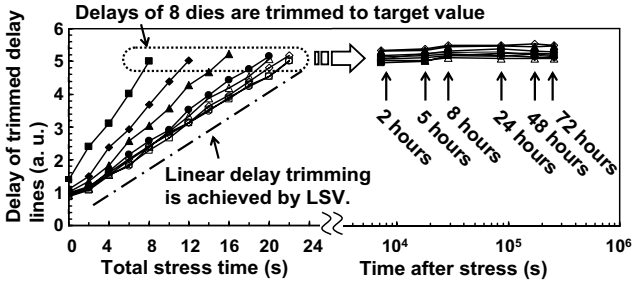



Fig. 5. Measured delay trimming by proposed LSV.

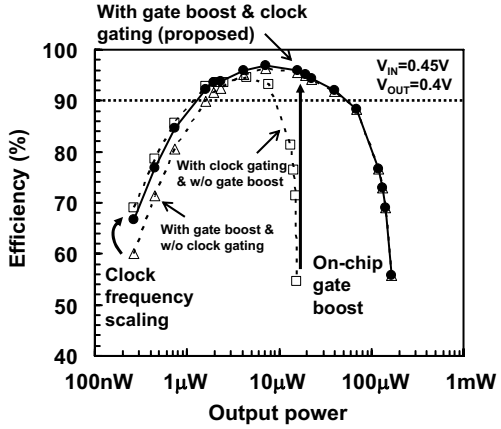
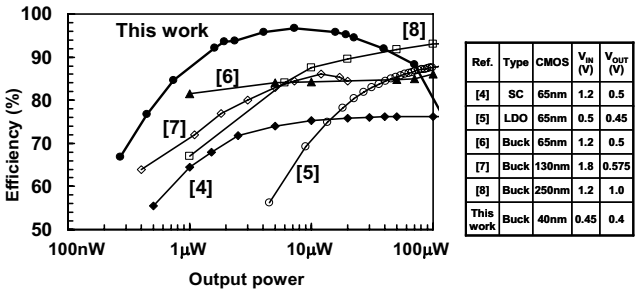



Fig. 6. Measured dependence of efficiency vs. output power.




| Ref. | Type | CMOS | $V_{IN}$ (V) | $V_{OUT}$ (V) |
|---|---|---|---|---|
| [4] | SC | 65nm | 1.2 | 0.5 |
| [5] | LDO | 65nm | 0.5 | 0.45 |
| [6] | Buck | 65nm | 1.2 | 0.5 |
| [7] | Buck | 130nm | 1.8 | 0.575 |
| [8] | Buck | 250nm | 1.2 | 1.0 |
| This work | Buck | 40nm | 0.45 | 0.4 |

Fig. 7. Comparison with published low voltage DC-DC converters.

delay line. During the stress for the charge injection, $V_{DD}$ is set to 1.1V. By applying a high n-well voltage as a stress voltage ($V_{stress}$), the absolute value of the threshold voltage of pMOS is raised to increase the delay.

TABLE I
Performance Summary

| | |
|---|---|
| **Technology** | **40-nm CMOS** |
| **Input voltage** | **0.45V** |
| **Output voltage** | **0.34V~0.44V** |
| **Output power** | **270nW~165μW** |
| **Output ripple** | **<5mV** |
| **Max. efficiency** | **97% at 7μW** |
| **Quiescent power at $I_{OUT}$=0** | **140nW** |
| **Active area** | **0.043 mm²** |

## III. Measurement Results

A die photo of the buck converter fabricated with a 40-nm CMOS is shown in Fig. 4. Fig. 5 shows a measured stress time dependence of the delay of the trimmed delay line and the retention characteristics for 8 dies. The target delay is set to five times of the initial delay to show the controllability of proposed LSV scheme. The linear delay trimming by LSV and the compensation of the die-to-die delay variations are successfully demonstrated. No significant retention degradation is observed.

Fig. 6 shows the measured dependence of the efficiency on $P_{OUT}$. By using the proposed OGB, the efficiency is increased from 55% to 96% at $P_{OUT}$ of 15μW. On the other hand, at $P_{OUT}$ of 270nW, the efficiency is increased from 60% to 67% by the proposed clock gating of SR. At $P_{OUT}$ range from 2μW to 50μW, the proposed buck converter achieves more than 90% efficiency (> ideal LDO efficiency=0.4V/ 0.45V=89%) with a peak value of 97% at 7μW. Fig. 7 shows the comparison with the published low voltage and low power DC-DC converters [4-8]. Table I shows a performance summary.

## V. Summary

A 0.45-V input, 0.4-V output on-chip gate boosted (OGB) buck converter with clock gated digital PWM controller is designed in 40-nm CMOS process. The proposed buck converter achieved the highest efficiency to date with $P_{OUT}$ less than 40μW. Moreover, higher than 90% efficiency is achieved at $P_{OUT}$ range from 2μW to 50μW. A linear delay trimming by a logarithmic stress voltage (LSV) scheme is also proposed to compensate for the die-to-die delay variations of a delay line in the PWM controller with good controllability.

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