6.4 1μm-Thickness 64-Channel Surface Electromyogram Measurement Sheet with 2V Organic Transistors for Prosthetic Hand Control

Hiroshi Fuketa[1,2], Kazuaki Yoshioka[1,2], Yasuhiro Shinozuka[1,2], Koichi Ishida[1,2], Tomoyuki Yokota[1,2], Naoji Matsuhisa[1,2], Yusuke Inoue[1,2], Masaki Sekino[1,2], Tsuyoshi Sekitani[1,2], Makoto Takamiya[1,2], Takao Someya[1,2], Takayasu Sakurai[1,2]

[1]University of Tokyo, Tokyo, Japan, [2]JST/ERATO, Tokyo, Japan

A surface electromyogram (EMG), which measures a voltage waveform produced by skeletal muscles on skin, is an important tool for applications detecting the human will of motion, such as for prosthetic hands and prosthetic legs. In the application to a prosthetic hand, a multipoint EMG measurement is required to precisely control the hand [1, 2]. Conventional multipoint measurements with a passive electrode array [1-3], however, have two problems: 1) Measurement over a long time period is annoying, because the EMG electrodes placed on the skin are rigid, and 2) the signal integrity of EMG is degraded, because the number of wires between the electrodes and the front-end circuits increases with increasing number of measurement points. To address these challenges, a surface EMG measurement sheet (SEMS) on which an EMG electrode array and a front-end amplifier array with 2V organic transistors are integrated on a 1μm-thick ultra-flexible film is developed to control prosthetic hands. The developed SEMS enables a comfortable long-time measurement without signal integrity degradation.

The design challenges of organic circuits for the amplifier array are as follows: 1) the increase in the pitch of the electrode array due to the large area of the amplifier, and 2) the mismatch of amplifiers due to the large mismatch of organic transistors. To solve these problems, we propose: 1) a distributed and shared amplifier (DSA) architecture for the in-situ amplification of the myoelectric signal with a fourfold increase in EMG electrode density, and 2) the post-fabrication select-and-connect (SAC) method that reduces the transistor mismatch and the power consumption of the amplifier by 92% and 56%, respectively, compared with the use of conventional parallel transistors.

Figure 6.4.1 shows a photograph of the developed 45x40mm^2 64-channel SEMS. In SEMS, an 8x8 EMG electrode array sheet and an 8x2 front-end amplifier array sheet with 2V organic transistors on a 1μm-thick ultra-flexible polyethylene naphthalate (PEN) film are stacked. The pitch of the EMG electrode is 0.7mm and the area of the 8x8 EMG electrode array is 3.5mm^2. Figure 6.4.2 shows a circuit schematic of SEMS with the proposed DSA architecture. SEMS has an amplifier array instead of a conventional passive electrode array [1-3] to avoid signal integrity degradation. Because the area of the amplifier is large, as shown in Figs. 6.4.1 and 6.4.7, one amplifier is shared by four EMG electrodes, which increases the electrode density fourfold. In addition, the EMG electrode array and the amplifier array are fabricated on separate sheets and the sheets are stacked [4] to increase the electrode density. As shown in Fig. 6.4.2, in Block00, one of the four EMG electrodes is selected by local word line (LWL) signals LWL0 to LWL3, and the source-followed signal is amplified by the amplifier. Then, the two outputs of the amplifiers are selected by global word line (GWL) signals GWL0 to GWL1. We use 2V organic pMOS transistors with the organic semiconductor of DNTT [5] and the gate dielectric of a self-aligned monolayer (SAM) technology [6], which requires a pMOS-only circuit design.

Figure 6.4.3 shows conventional and proposed transistor mismatch reduction techniques for the amplifier array. Figures 6.4.3(a) and (b) show conventional transistor mismatches in a single transistor and N parallel transistors, respectively. Figure 6.4.3(c) shows the proposed post-fabrication SAC method. In the SAC method, first, the I-V characteristics (e.g., threshold voltage and ON-current (I_{ON})) of each transistor are measured. 2N measurements are required. Then, M_1 and M_2 transistors are selected from the left and right groups in Fig. 6.4.3(c), respectively, on the basis of the results of calculation to minimize the target mismatch. M_1 and M_2 are not always equal. Finally, the selected M_1 (M_2) transistors are connected by inkjet-printed interconnects, as shown in Fig. 6.4.3(c). Although the proposed SAC is too costly and impractical in silicon VLSI technology, SAC is advantageous in printed electronics. In Fig. 6.4.3(d), the area, power, and mismatch are compared among (a) single transistor, (b) parallel transistors, and (c) SAC. Detailed analysis is shown in Fig. 6.4.4.

Figure 6.4.4(a) shows the measured I_{DS}-V_{DS} characteristics of 11 organic pMOS transistors. In this work, the target mismatch is I_{ON}. On the basis of the measured $\mu(I_{ON})$ and $\sigma(I_{ON})$, I_{ON} mismatch is simulated assuming that I_{ON} is normally distributed, and the conventional parallel transistors (Fig. 6.4.3(b)) and the proposed SAC (Fig. 6.4.3(c)) are compared. Figure 6.4.4(b) shows the simulated N dependence of I_{ON} mismatch. The I_{ON} mismatch of the parallel transistors is proportional to $1/\sqrt{N}$ according to Pelgrom's law. In contrast, the I_{ON} mismatch of the proposed SAC is much smaller than that of the conventional parallel transistors. Figure 6.4.4(c) shows the simulated N dependence of I_{ON} mismatch reduction derived from Fig. 6.4.4(b). I_{ON} mismatch reduction is -92% at N=4, which corresponds to the photograph in Fig. 6.4.3(c). Figure 6.4.4(d) shows the simulated N dependence of $\mu(I_{ON})$ (=average power). $\mu(I_{ON})$ is reduced by 56% at N=4 compared with that of the parallel transistors. In this way, the proposed SAC achieves a much smaller mismatch than the conventional parallel transistors with less power overhead.

In pMOS-only circuit design, it is difficult to increase the gain of an amplifier. A pseudo-CMOS inverter [4, 7] achieves a high gain, although it requires a negative voltage. Therefore, in this work, a pMOS-only amplifier with an AC-coupled load based on [8] is used, which does not require a negative voltage. Figure 6.4.5(a) shows a circuit schematic of the pMOS-only amplifier used in SEMS. For comparison, a conventional diode load is also shown. In the AC-coupled load, the V_{GS} of M_1 is constant owing to C_2 and the impedance of the load is high, thereby achieving a high gain. C_1 and C_2 are implemented by MIM capacitors, and R_1 and R_2 are implemented by pMOS transistors. Figure 6.4.5(b) shows the measured frequency dependence of the gain of the amplifier at 2V. The gain of the amplifier with the AC-coupled load is much higher than that with the diode load. The power consumption of the amplifier with the AC-coupled load is 30μW. The target specifications of the amplifier are "gain at 100Hz > 20dB" and "gain at 500Hz > 10dB", because the typical amplitude and frequency band of the surface EMG are 1-to-2mV and 10-to-500Hz, respectively. In Fig. 6.4.5(b), the measured gains at 100Hz and 500Hz are 21dB and 10dB, respectively, which satisfy the target specification.

Figure 6.4.6 shows the measurement setup and measured waveforms of the surface EMG with the organic amplifier. The difference between the waveforms with open and closed hands is clearly observed. Figure 6.4.7 shows the photograph of the organic amplifier and a summary of key features.

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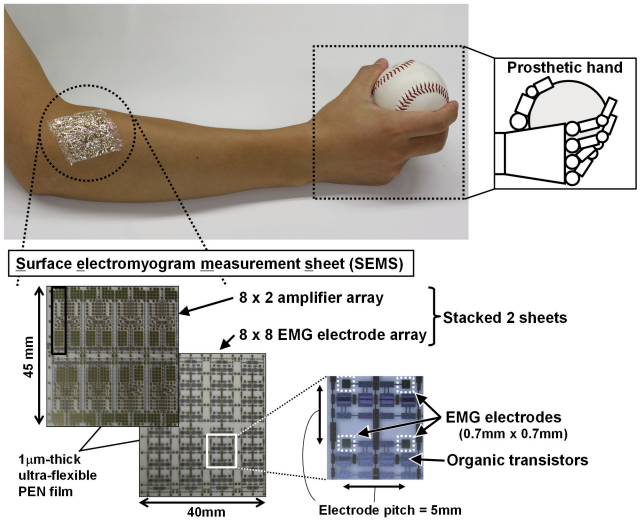


Figure 6.4.1: Developed 64-channel surface electromyogram measurement sheet (SEMS).

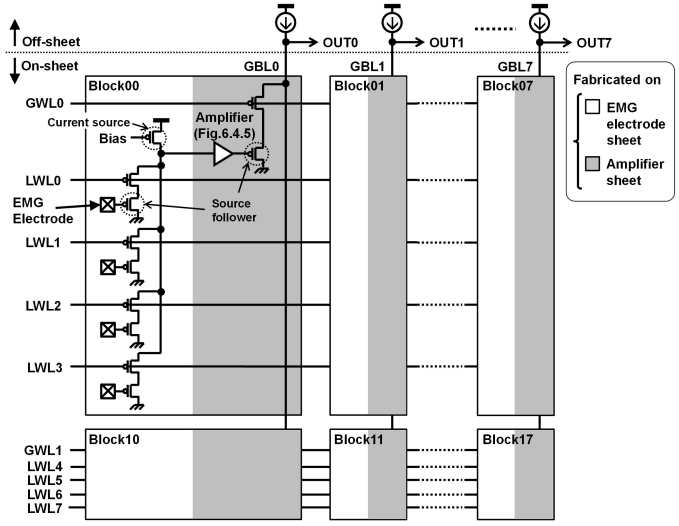


Figure 6.4.2: Circuit schematic of SEMS with proposed distributed and shared amplifier (DSA) architecture.

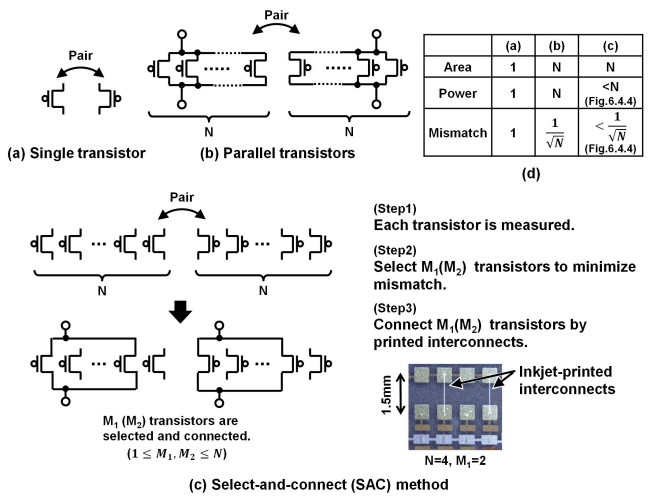


Figure 6.4.3: Conventional and proposed transistor mismatch reduction techniques. The post-fabrication select-and-connect (SAC) method is proposed.

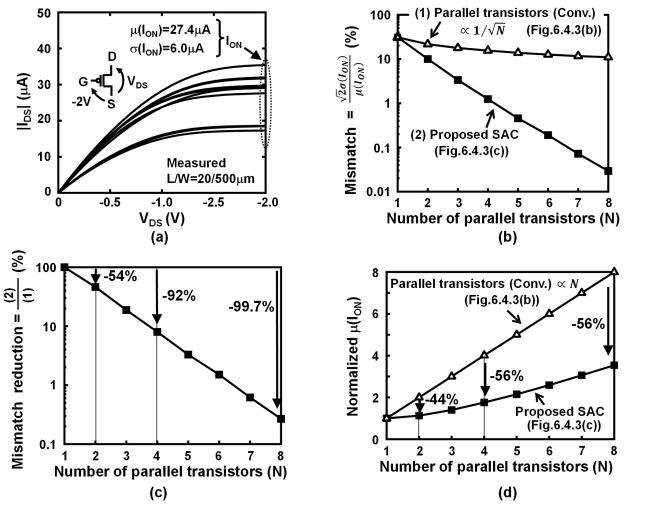


Figure 6.4.4: (a) Measured mismatch in 11 organic pMOS transistors. Simulated N dependence of (b) I_{ON} mismatch, (c) I_{ON} mismatch reduction, and (d) average I_{ON}.

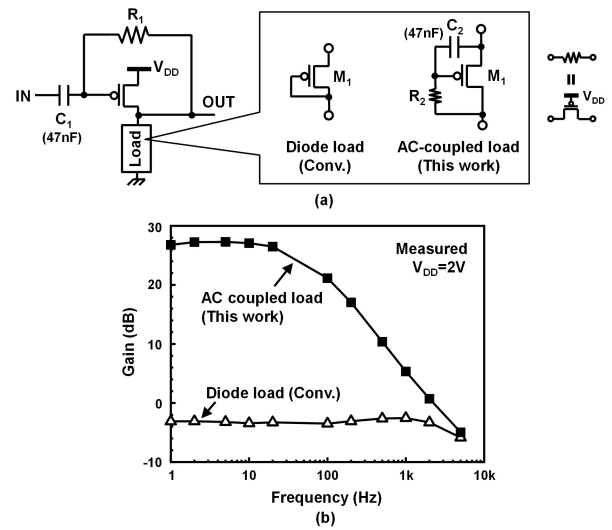


Figure 6.4.5: (a) Schematic of pMOS-only amplifier. (b) Measured frequency dependence of gain of amplifiers with different loads.

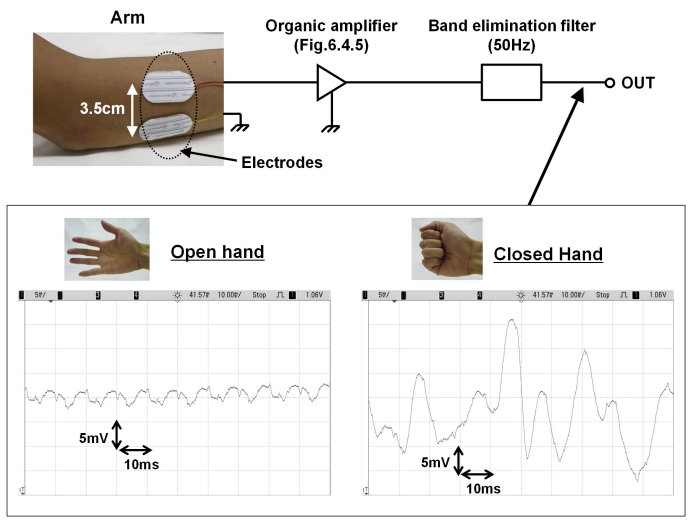
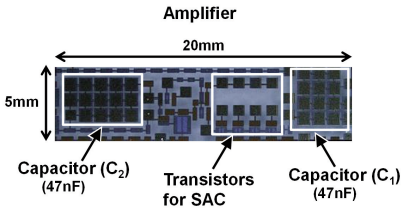


Figure 6.4.6: Measurement setup and measured waveforms of surface EMG with organic amplifier.



Performance summary of amp.

Unity-gain frequency		2kHz
Gain	@ 10Hz	27dB
	@ 100Hz	21dB
	@ 200Hz	17dB
	@ 500Hz	10dB

Organic transistors	
Semiconductor material	DNTT (Mobility=1.0 cm^2/Vs)
Gate oxide material, thickness	SAM* 2nm + AlOx 4nm = 6nm
Minimum gate length	20μm
Surface electromyogram measurement sheet	
Sheet size	45mm x 40mm
Number of amplifiers	16
Number of EMG electrodes	8 x 8 (5mm pitch)

*SAM: Self assembled monolayer

Figure 6.4.7: Photograph and key features.

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