24.9 Intermittent Resonant Clocking Enabling Power Reduction at any Clock Frequency for 0.37V 980kHz Near-Threshold Logic Circuits

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In order to improve the energy efficiency of logic circuits, reductions in capacitance (C) and power supply voltage (V_{DD}) are required, as energy consumption is proportional to CV_{DD}^2. Near-threshold (V_t) operation achieves an energy minimum [1]. Resonant clocking [2-5] can reduce the effective capacitance of the clock distribution network [3]. In this work, a new resonant clocking scheme enabling power reduction at any clock frequency is proposed and applied to a 0.37V 980kHz near-V_t logic circuit in 40nm CMOS.

Figs. 24.9.1(a), (b), and (c) show conventional non-resonant clocking with a buffered H-tree, conventional resonant clocking with an unbuffered H-tree [4-5], and the proposed intermittent resonant clocking (IRC) with an unbuffered H-tree, respectively. The conventional resonant clocking in Fig. 24.9.1(b) has three problems: 1) The clock frequency (f_{CLK}) range is narrow, typically ±20% [3-5]. At f_{CLK} lower than the resonant frequency (f_{RES}), power higher than that of non-resonant clocking and functional errors due to ringing are observed [2], which prohibit dynamic frequency scaling (DFS) and low-speed testing. 2) f_{CLK} values in previous papers [2-5] range from 100MHz to 5GHz and less-than-1MHz operation is difficult to achieve, because a large inductance for the resonance is required, which prevents the application of resonant clocking to near-V_t logic circuits. 3) A sinusoidal clock waveform increases the clock skew due to the low slew rate. To solve these problems, the IRC in Fig. 24.9.1(c) is proposed. In conventional resonant clocking, the clock period (T_{CLK}) is equal to the resonant period (T_{RES}). In contrast, in IRC, T_{CLK} is larger than T_{RES}. Therefore, IRC has three advantages: 1) The selection of f_{CLK} is flexible, and power reduction is achieved at any clock frequency. Thus, IRC can be applied to near-V_t logic circuits, and DFS and low-speed testing are possible. 2) The required inductance for the resonance is reduced to $(T_{RES}/T_{CLK})^2$ of conventional resonant clocking. 3) A small clock skew owing to a high slew rate is obtained. The slew rate is increased to T_{CLK}/T_{RES} of conventional resonant clocking.

Details of IRC are shown in Fig. 24.9.2. Fig. 24.9.2(a) shows a schematic of the circuit of an IRC buffer that drives the clock node (CKB). C_{CLK} denotes the capacitance of CKB. A voltage doubler [6] is added to overdrive the gate of nMOS (M1). Figs. 24.9.2 (b) and (c) show timing waveforms for the IRC circuit. To illustrate the operating principles of IRC, Fig. 24.9.2(b) shows timing waveforms with a step input applied. Fig. 24.9.2(c) shows actual IRC operation with a pulse input. When Pulse is high, IRC is in a resonant mode. In contrast, when Pulse is low, IRC is in a non-resonant mode. In IRC, both the resonant mode and the non-resonant mode are mixed within a clock period and T_{CLK} is larger than T_{RES}, thereby enabling the flexible selection of f_{CLK}. The pulse width (T_{PW}) of Pulse shown Fig. 24.9.2(c) is an important parameter for IRC to minimize the clocking power. In Fig. 24.9.2(b), after the step input, CKB shows ringing at around 0V. To minimize the clocking power, the highest voltage in the ringing shown as "Point A" in Fig. 24.9.2(b) indicates the best timing for T_{PW}, because the power required to pull up CKB to V_{DD} is minimized at Point A. The timing of Point A corresponds to T_{RES}, as shown in Fig. 24.9.2(b). In contrast, the lowest voltage in the ringing at T_1 indicates the worst timing at which the clocking power is maximized. Similarly, T_2 indicates the second worst timing.

To minimize the clocking power, the large ringing observed in Fig. 24.9.2(b) is required. Such ringing is determined by the resistance of the LC resonator, which is dominated by the ON resistance of M1 in Fig. 24.9.2(a). In the 0.37V near-V_t logic circuit, however, the ON resistance at V_{DD} = 0.37V is very high. To decrease the ON resistance with small area and power overhead, the gate of M1 is boosted by the voltage doubler. Fig. 24.9.3(a) shows a simulated comparison of the gate widths and powers of M1 with and without gate boosting at the same ON resistance. At the same ON resistance, the proposed gate boosting with the voltage doubler reduces the gate width of M1 and the power dissipation to drive M1 by 97% and 91%, respectively.

The proposed IRC is applied to a 0.37V near-V_t adder array. Fig. 24.9.3(b) shows a block diagram of a test chip. 32 arrays of 32b adders are implemented with input/output latches. The critical path of each adder is 110 FO4 inverter delays. In IRC, static CMOS latches, instead of flip-flops, are used, since CKB is not a signal with a 50% duty cycle but a pulse signal, as shown in Fig. 24.9.2(c). In this paper, V_{DD} = 0.37V is used, because the measured minimum energy of the adder array is achieved at V_{DD} = 0.37V.

In the test chip, conventional non-resonant clocking with an unbuffered clock tree is also implemented for comparison, since clocking with an unbuffered tree is more energy-efficient than that with a buffered tree in near/sub-V_t circuits [7]. Figures 24.9.4 (a) and (b) show conventional non-resonant clocking and the proposed IRC, respectively. For a fair power comparison, the unbuffered clock tree is the same and the gate widths of the clock drivers are designed to have the same slew rate. Compared with conventional non-resonant clocking, the total gate width of the proposed IRC is reduced by 84%. Fig. 24.9.4 also shows the measured waveforms of CKB at V_{DD} = 0.37V and f_{CLK} = 980kHz. The measured waveform in Fig. 24.9.4(b) validates the qualitative waveform in Fig. 24.9.2(c). The measured slew rates in Figs. 24.9.4(a) and (b) are similar. In IRC, the measured f_{RES} is 19MHz with an off-chip inductor of 7µH, which corresponds to C_{CLK} of 10pF. In this implementation, T_{CLK}/T_{RES} = 19. Therefore, the required inductance of IRC for the resonance is reduced to $1/19^2$ = $1/361×$ that of conventional resonant clocking, and the slew rate is increased to 19× that of conventional resonant clocking.

To validate the discussion on the optimum T_{PW} in Figs. 24.9.2 (b) and (c), Fig. 24.9.5 shows the measured T_{PW} dependence of the clock power of IRC. The clock power of the conventional non-resonant clocking (Fig. 24.9.4(a)) is also shown for comparison. As expected, the minimum clock power is achieved at T_{PW} = T_{RES} with the power reduction of -36%.

To demonstrate power reduction at any clock frequency in the proposed IRC, Fig. 24.9.6 shows the measured f_{CLK} dependence of the clock powers of conventional non-resonant clocking and the proposed IRC. In IRC, the clock power is proportional to f_{CLK}, which is different from that observed in conventional resonant clocking [2-5]. Compared with that of conventional non-resonant clocking, the clock power of IRC is reduced at all f_{CLK} values, which is the most important advantage of the proposed IRC. At f_{CLK} = 980kHz, the clock power is reduced by 36% and the total power including the adder array is reduced by 10%. When the clock is stopped, the clock leakage power is reduced by 81%, owing to the 84% gate width reduction in Fig. 24.9.4.

Fig. 24.9.7(a) shows a die micrograph of the test chip in 40nm CMOS. The area overhead due to the voltage doubler is 0.6%. Fig. 24.9.7(b) shows a comparison with prior work.

References:
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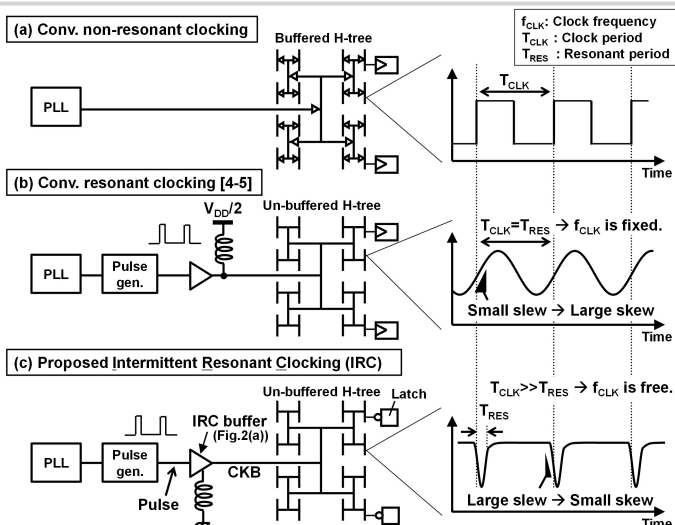
Figure 24.9.1: (a) Conventional non-resonant clocking; (b) conventional resonant clocking [4-5]; (c) proposed intermittent resonant clocking (IRC).
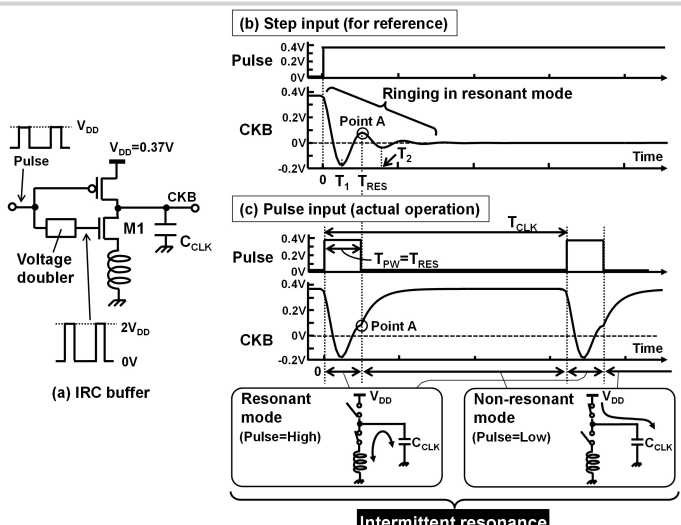

Figure 24.9.2: (a) IRC buffer; (b) timing waveforms of IRC with a step input; (c) timing waveforms of IRC operation with a pulse input.
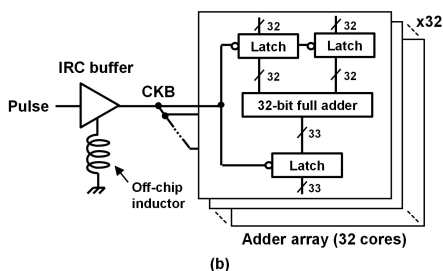

Figure 24.9.3: (a) Simulated comparison of gate widths and powers of M1; (b) block diagram of test chip including adder array and IRC.
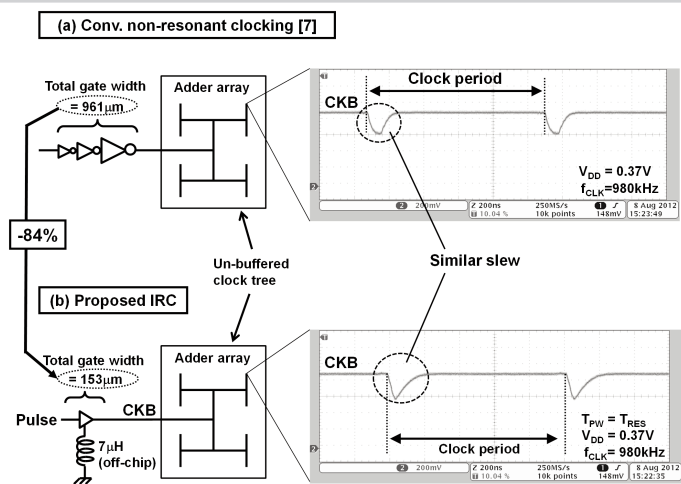

Figure 24.9.4: Two clocking circuits in test chip for comparison. (a) Conventional non-resonant clocking [7]; (b) proposed IRC.
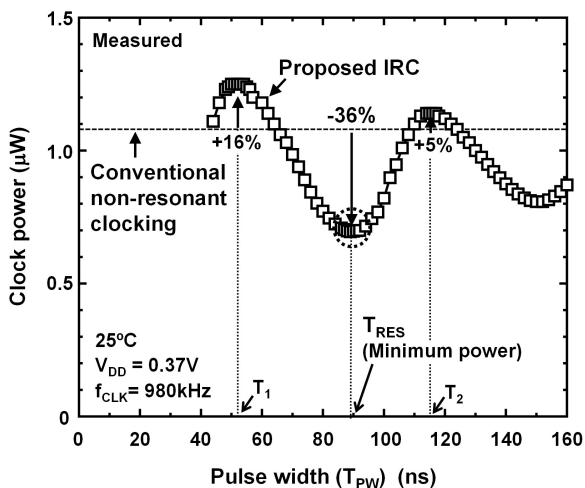

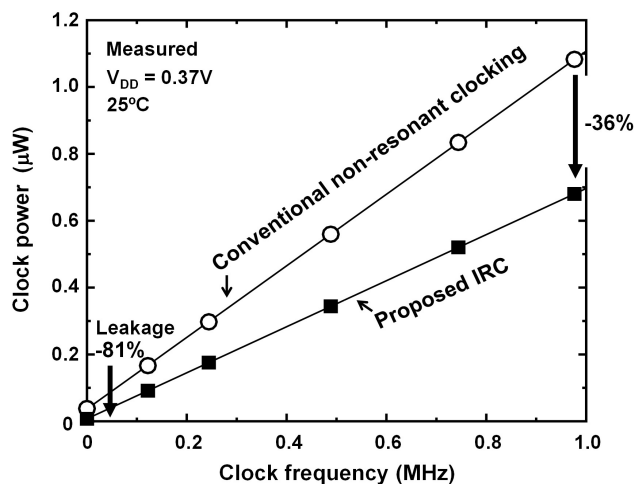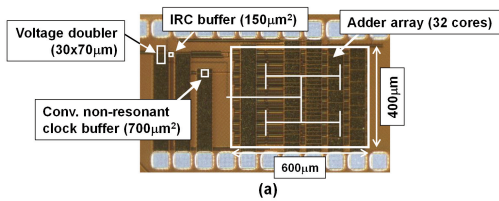Figure 24.9.5: Measured dependence of clock power on pulse width of Pulse signal (T_{PW}).

Figure 24.9.6: Measured f_{CLK} dependence of clock powers of conventional non-resonant clocking and proposed IRC.

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(a)

	ISSCC08 [2]	ISSCC12 [3]	CICC07[4]	ESSCIRC09 [5]	This work
Supply voltage	1.2V	1.2V	1.03-1.21V	1.2V	0.37V
Clock frequency (f_{CLK})	1.6 ~ 5GHz	< 4.25GHz*	800MHz ~ 1.2GHz	100 ~ 200MHz	DC ~ 980kHz
Resonant frequency	3.2GHz	3.3GHz	1.03GHz	125MHz	19MHz
Freedom of f_{CLK}	Poor ($P \not\propto f$)	Fair ($P \not\propto f$)*	Poor ($P \not\propto f$)	Poor ($P \not\propto f$)	Good ($P \propto f$)
Clock slew rate	Fair	Fair	Low	Low	High
Local clock buffer	Yes	Yes	No	No	No
Inductor	On-chip	On-chip	On-chip	Off-chip	Off-chip
Latch/FF	FF	FF	Latch	FF	Latch
Power reduction	25%	24%	76%	85%	36 ~ 81%

(*) Inductors can be disconnected when the clock frequency is low (<2.9GHz). In this case, conventional clocking is used, and hence the clock power is proportional to the clock frequency.

(b)

Figure 24.9.7: Die micrograph and compairison with previous works.