Reducing IR Drop in 3D Integration to Less Than 1/4 Using Buck Converter on Top Die (BCT) Scheme

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Abstract

This paper proposes a method to reduce the supply voltage IR drop of 3D stacked-die systems by implementing an on-chip Buck Converter on Top die (BCT) scheme. The IR drop is caused by the parasitic resistance of Through Silicon Vias (TSV's) used in the 3D integration. The IR drop reduction and the overhead associated with the BCT scheme are modeled and analyzed. A 3D stacked-die system is manufactured using 90nm CMOS technology with TSV's and a silicon interposer. A chip inductor and chip capacitors for the buck converter are mounted directly on the top die. The reduction of the IR drop to less than 1/4 is verified through experiments.

Keywords

3D integration, TSV, Stacked die, Buck converter, IR drop, Power integrity, Power supply, DC-DC converter

1. Introduction

Recently, 3-dimensional integration based on TSV's have been explored extensively for achieving low power and high performance to break the limit of single-chip 2D integration. The TSV and associated bump connection structure (TSV link) inherently have parasitic resistance and thus the supply voltage is exposed to IR drop due to the TSV link resistance [1-4]. This is considered to be a stringent issue in 3D integration since the IR drop quadratically increases as the number of stacked dies increases, whose detailed analysis is presented in Section 3 of this paper.

The increase of IR drop is shown in Fig.1. The IR drop is calculated as a function of the number of stacked dies (N) and the total number of TSV's per die (n_L) used for power delivery including both V_{DDL} and V_{SS}. If allowable IR drop is assumed to be 3% of the nominal power supply voltage (V_{DDL}), it is seen from the figure that hundreds of TSV's are needed to make the IR drop within the tolerance. Part of the reason why the problem gets severe is that the IR drop in V_{SS} lines is additive to the V_{DD} IR drop and the number of total TSV's required for the power delivery includes both V_{DD} TSV's and V_{SS} TSV's. In this paper, the IR drop is defined as the DC voltage drop across V_{DD} lines and V_{SS} lines.

In order to reduce the IR drop due to TSV, a Buck Converter on Top die (BCT) scheme is proposed in Section 2. In Section 3, The IR drop reduction and the overhead associated with the BCT scheme are modeled and analyzed. A fabricated 3D stacked-die system is described in Section 4 and the measurement results are presented in Section 5 followed by conclusions in Section 6.

2. Buck Converter on Top die (BCT) scheme

A typical 3D integration with the conventional power supply scheme is illustrated in Fig.2. All the current is supplied from a buck converter which is either implemented on the bottom die or is implemented as a separate die residing external to the 3D stacked dies. Since the top die can be far from the power supply circuit, the IR drop gets large as the current must go through many serially-connected TSV's.

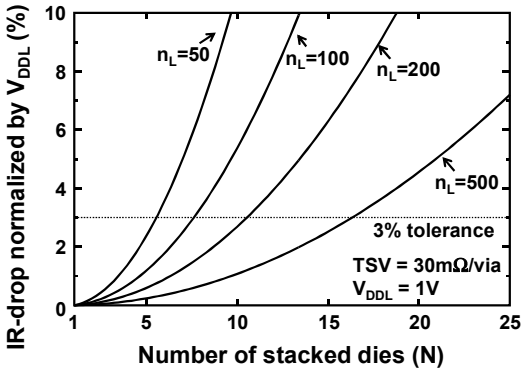


Fig. 1 Caluculated IR drop in 3D integration. n_L is the total number of TSV's per die used for power delivery including both V_{DDL} and V_{SS} TSV's. Each die is assumed to consume 1A.

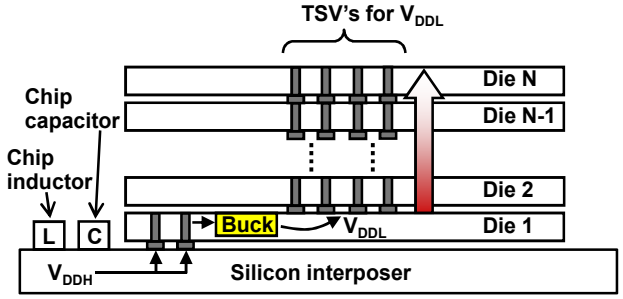


Fig. 2 Conventional power supply scheme. The buck converter on the bottom chip could be on a separate die. The TSV's for V_{SS} are omitted for simplicity.

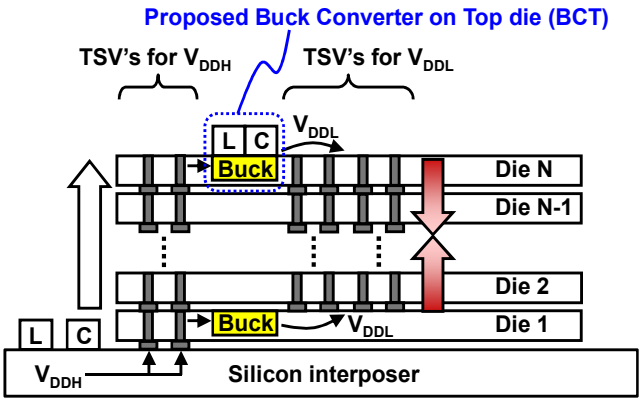


Fig. 3 Proposed Buck Converter on Top die (BCT) scheme. The TSV's for V_{SS} are omitted for simplicity.

The proposed BCT scheme is depicted in Fig.3. By adding a buck converter on the topmost die (Die N), the current to an upper half of the 3D integration (Die (N/2)+1 ~ Die N) is delivered from the added BCT, while the current for a lower half (Die 1 ~ Die N/2) is supplied from the buck converter on the bottom. Each buck converter on the top die and the bottom die stably supply the specified voltage and the current to the furthest die (Die N/2, Die (N/2)+1) from a buck converter through less number of TSV's compared with the conventional case. Thus, the maximum IR drop gets smaller and improved. Compared with the direct V_{DDL} power delivery to the topmost die, the TSV current for V_{DDH} in BCT is reduced to (V_{DDL}/V_{DDH}) times by the voltage down conversion from V_{DDH} to V_{DDL}. thereby reducing the required number of TSV's for V_{DDH}.

For a general case where each chip consumes different amount of current, the IR drop improvement and the overhead by the BCT scheme needs to be calculated case by case. For example, if the topmost die consumes most of the total current, the BCT reduces the IR drop caused by TSV's to almost zero. The difficult case for both the conventional and the BCT arises when all dies consume the same amount of current. This uniformly distributed current consumption case can be treated theoretically and gives insight to the design trade-off of the BCT scheme. Thus, the detailed discussion for the uniform case is given in Section 3 and it is shown that the maximum IR drop is reduced to less than 1/4 of the one observed in the conventional approach.

The overhead of the BCT is the area overhead and the power loss caused by the added TSV's to bring the external high voltage (V_{DDH}) to the top die. In Section 3, this overhead is shown to be reasonably small. It should be noted that if the IR drop has to be reduced to 1/4 in the conventional approach, the number of TSV's should be increased by a factor four.

A buck converter is used as a DC-DC voltage down converter, since the buck converter provides high conversion efficiency at rather high current output among different types of DC-DC voltage down converters. Unfortunately though, the buck converter requires a low-resistance inductor and a large capacitor as a low-pass filter, which cannot be realized by an on-chip coil and MOS capacitors.

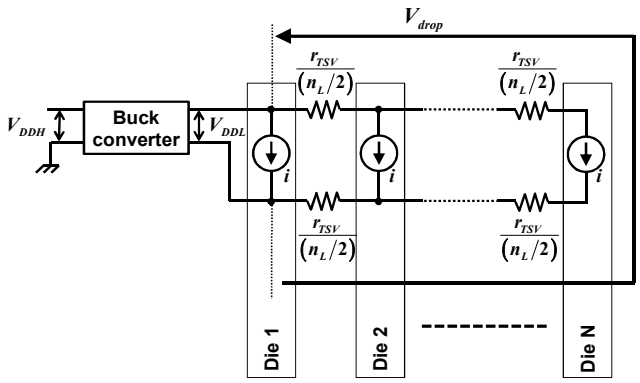


Fig. 4 Equivalent circuit for conventional scheme. V_{drop} is maximum IR drop and is defined in (1). r_{TSV} is a resistance of a single TSV, n_L is the total number of TSV's per die for both V_{DDL} and V_{SS}.

Off-chip components, such as a chip inductor and a chip capacitor, are needed as shown in Figs. 2 and 3. Only on the top die, it is possible to directly mount the off-chip components and thus in the BCT scheme, a buck converter is added only on the topmost die.

Since the chip capacitor on the top die can provide μF order of capacitance, which is difficult to realize by on-chip MOS capacitors, the BCT scheme has an added benefit of improving dynamic power integrity although this benefit is not the main target of this paper.

3. Design considerations

The theoretical background for the BCT scheme is established in this section. The IR drop reduction and the overhead associated with the BCT scheme are modeled and analyzed.

3.1. IR drop reduction by conventional power supply scheme

The equivalent circuit for the conventional scheme (Fig. 2) is depicted in Fig. 4. The maximum IR drop due to TSV's (V_{drop} in Fig. 4) is given by

$$\begin{aligned} V_{drop}(N,n_L) &= (N-1)i\frac{r_{TSV}}{n_L/2}+(N-2)i\frac{r_{TSV}}{n_L/2}+\cdots+i\frac{r_{TSV}}{n_L/2} \\ &\quad +(N-1)i\frac{r_{TSV}}{n_L/2}+(N-2)i\frac{r_{TSV}}{n_L/2}+\cdots+i\frac{r_{TSV}}{n_L/2} \\ &= \frac{2ir_{TSV}}{n_L}N(N-1), \end{aligned} \tag{1}$$

where N is the number of the stacked dies, r_{TSV} is a resistance of a single TSV, n_L is the total number of TSV's per die for both V_{DDL} and V_{SS}, and i is the load current of each die.

Equation (1) indicates that the IR drop is inversely proportional to n_L, and hence increasing n_L can reduce the IR drop. On the other hand, the power dissipation of TSV's decreases by the TSV resistance reduction obtained by the increase in n_L. Therefore, the power of TSV's is discussed from here.

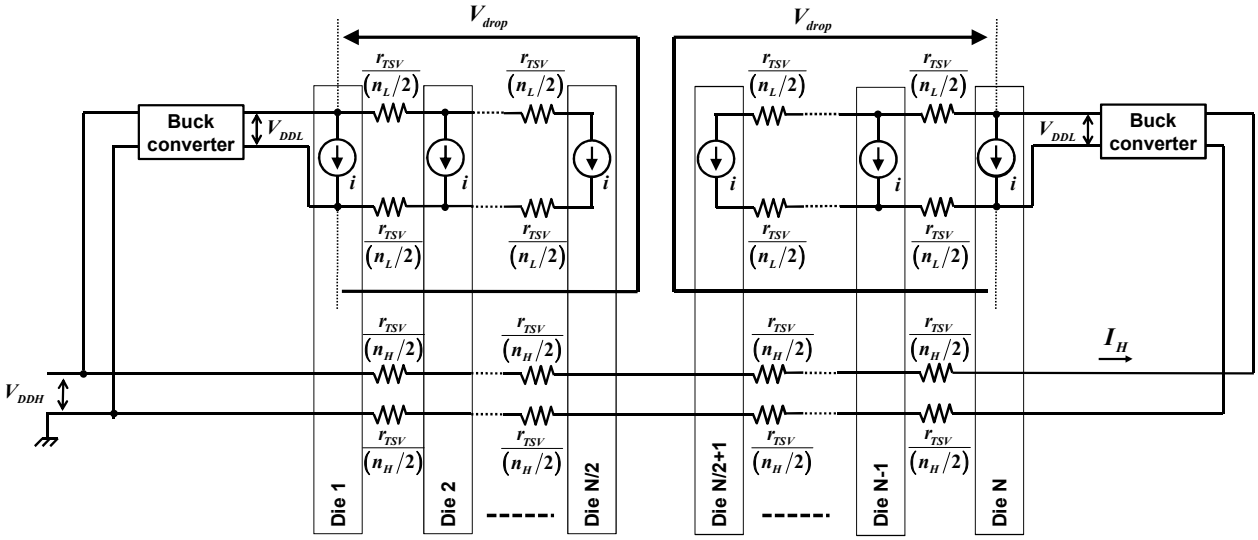


Fig. 5 Equivalent circuit for proposed BCT scheme. V_{drop} is maximum IR drop. n_H is the total number of TSV's per die for both V_{DDH} and V_{SS}.

Let $P_{TSV,L}$ be the power dissipation of the TSV's for V_{DDL} and V_{SS}. $P_{TSV,L}$ is written as

$$P_{TSV,L}(N,n_L)=\{(N-1)i\}^2\frac{r_{TSV}}{n_L/2}+\{(N-2)i\}^2\frac{r_{TSV}}{n_L/2}+\cdots+i^2\frac{r_{TSV}}{n_L/2}$$
$$+\{(N-1)i\}^2\frac{r_{TSV}}{n_L/2}+\{(N-2)i\}^2\frac{r_{TSV}}{n_L/2}+\cdots+i^2\frac{r_{TSV}}{n_L/2}$$
$$=\frac{2i^2r_{TSV}}{3n_L}N(N-1)(2N-1). \quad (2)$$

The total power dissipation of the N-stacked dies is expressed as

$$P_{LOAD}=V_{DDL}\cdot Ni. \quad (3)$$

From (1), (2), and (3), the ratio of the TSV power to the total power of the stacked dies is derived as

$$\frac{P_{TSV,L}}{P_{LOAD}}=\frac{1}{3}\cdot\frac{V_{drop}(N,n_L)}{V_{DDL}}\cdot\frac{2N-1}{N}. \quad (4)$$

When N is sufficiently large, this equation can be approximated to

$$\frac{P_{TSV,L}}{P_{LOAD}}\simeq\frac{2}{3}\cdot\frac{V_{drop}(N,n_L)}{V_{DDL}}. \quad (5)$$

When n_L increases by A times, the IR drop is reduced by 1/A times according to (1). In this case, the power loss due to the TSV increase (P_{LOSS}) is given by

$$\frac{P_{LOSS}}{P_{LOAD}}=\frac{P_{TSV,L}(N,An_L)-P_{TSV,L}(N,n_L)}{P_{LOAD}}=\left(\frac{1}{A}-1\right)\frac{P_{TSV,L}}{P_{LOAD}}$$
$$\simeq\left(\frac{1}{A}-1\right)\cdot\frac{2}{3}\cdot\frac{V_{drop}(N,n_L)}{V_{DDL}} \quad (6)$$

For example, in order to reduce the IR drop (V_{drop}/V_{DDL}) from 10% to 2.5% (A=4), P_{LOSS} decreases by 5%, whereas n_L increases by 4 times (300%). This means that a huge area overhead to reduce the IR drop is required in the conventional power supply scheme.

3.2. IR drop reduction by proposed BCT scheme

In the conventional power supply scheme, the TSV area overhead is huge as described in the previous section. On the other hand, the proposed BCT scheme can reduce the IR drop with moderate overheads. The overheads in the BCT scheme are discussed in this section.

In this paper, TSV's for V_{DDH} are added to the TSV's for V_{DDL}, that is, the number of TSV's for V_{DDL} (n_L) does not change. Fig. 5 shows the equivalent circuit for the proposed BCT scheme. Let $V_{drop(conv)}$ and $V_{drop(prop)}$ be the IR drops in the conventional and the proposed scheme, respectively. $V_{drop(conv)}$ and $V_{drop(prop)}$ are expressed using (1) as

$$V_{drop\ (conv)}=V_{drop}(N,n_L) \quad (7)$$

$$V_{drop\ (prop)}=V_{drop}(N/2,n_L)=\frac{2ir_{TSV}}{n_L}\frac{N(N-2)}{4}. \quad (8)$$

Therefore, from (7) and (8), the IR drop reduction is given by

$$\frac{V_{drop\ (prop)}}{V_{drop\ (conv)}}=\frac{N-2}{N-1}\cdot\frac{1}{4}<\frac{1}{4}. \quad (9)$$

This equation indicates that the BCT scheme can reduce the IR drop to less than 1/4.

In order to achieve such IR drop reduction, the following overheads are required; 1) area overhead due to additional TSV's for V_{DDH} and V_{SS}, and 2) power loss caused by the additional TSV's. From here, these overheads are analytically investigated.

Let $P_{TSV,H}$ be the power dissipation of the additional TSV's for V_{DDH} and V_{SS}. $P_{TSV,H}$ is given by

$$P_{TSV,H}=2\times\frac{r_{TSV}}{n_H/2}(N-1)\cdot{I_H}^2=\frac{4r_{TSV}}{n_H}(N-1)\cdot{I_H}^2, \quad (10)$$

where n_H is the number of TSV's per die for both V_{DDH} and V_{SS}, and I_H is the input current of the buck converter.

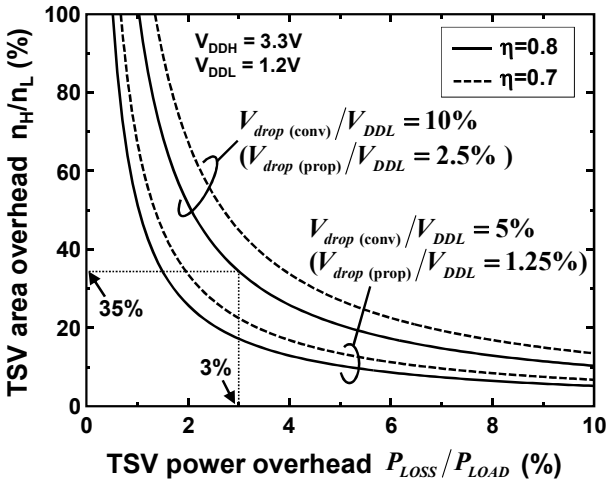


Fig. 6 TSV area and power overheads in IR drop reduction by BCT scheme. It is assumed that N is sufficiently large.

The input power (P_{in}) and the output power (P_{out}) of the buck converter are written as

$$P_{in} = V_{DDH} \cdot I_H , \tag{11}$$

$$P_{out} = \frac{P_{LOAD}}{2} = \frac{V_{DDL} \cdot Ni}{2} , \tag{12}$$

$$P_{out} = \eta P_{in} , \tag{13}$$

where η is the efficiency of the buck converter. Strictly speaking, the input voltage of the buck converter on the top die is slightly lower than V_{DDH} due to the resistance of TSV's for V_{DDH}. For simplicity, the voltage drop is ignored in this paper. From (11), (12), and (13), I_H is expressed as

$$I_H = \frac{P_{LOAD}}{2\eta V_{DDH}} . \tag{14}$$

Here, the power loss of TSV's for V_{DDH} is only considered for simplicity. From (10) and (14), the ratio of the power loss (P_{LOSS}) to the total power is derived as

$$\frac{P_{LOSS}}{P_{LOAD}} = \frac{P_{TSV,H}}{P_{LOAD}} = \frac{r_{TSV} P_{LOAD} (N-1)}{\eta^2 {V_{DDH}}^2} \left(\frac{n_L}{n_H}\right) \frac{1}{n_L} . \tag{15}$$

The following equation is obtained from (3) and (12).

$$\frac{1}{n_L} = \frac{2{V_{DD}}^2}{r_{TSV} P_{LOAD} (N-2)} \left(\frac{V_{drop\ (prop)}}{V_{DDL}}\right) . \tag{16}$$

Therefore, the following equation is derived from (15) and (16).

$$\frac{n_H}{n_L} \cdot \frac{P_{LOSS}}{P_{LOAD}} = \frac{2}{\eta^2} \cdot \frac{N-1}{N-2} \cdot \left(\frac{V_{drop\ (prop)}}{V_{DDL}}\right) \left(\frac{V_{DDL}}{V_{DDH}}\right)^2 \tag{17}$$

$$= \frac{1}{2\eta^2} \cdot \frac{N-2}{N-1} \cdot \left(\frac{V_{drop\ (conv)}}{V_{DDL}}\right) \left(\frac{V_{DDL}}{V_{DDH}}\right)^2 . \tag{18}$$

In this equation, n_H/n_L and P_{LOSS}/P_{LOAD} denote the area and power overheads due to the additional TSV's, and this equation shows a trade-off relation between them. With sufficiently large N, (17) and (18) can be approximated to

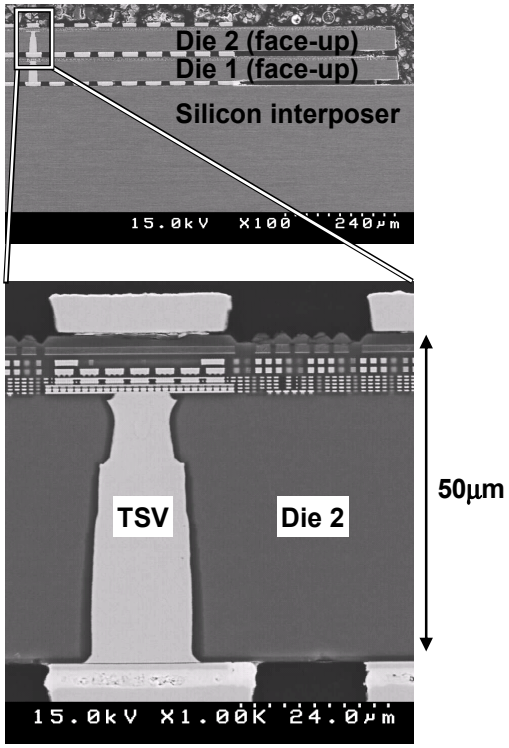


Fig. 7 Cross sectional view of 3D integrated system. The upper photo is a global view and the lower photo is a magnified view around a TSV.

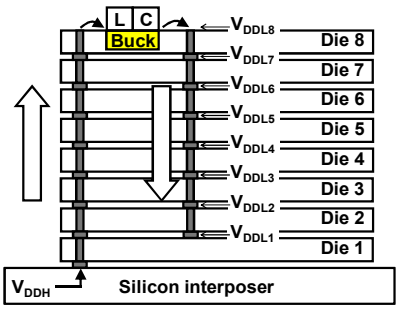
$$\frac{n_H}{n_L} \cdot \frac{P_{LOSS}}{P_{LOAD}} \simeq \frac{2}{\eta^2} \left(\frac{V_{drop\ (prop)}}{V_{DDL}}\right) \left(\frac{V_{DDL}}{V_{DDH}}\right)^2 \tag{19}$$

$$= \frac{1}{2\eta^2} \left(\frac{V_{drop\ (conv)}}{V_{DDL}}\right) \left(\frac{V_{DDL}}{V_{DDH}}\right)^2 . \tag{20}$$

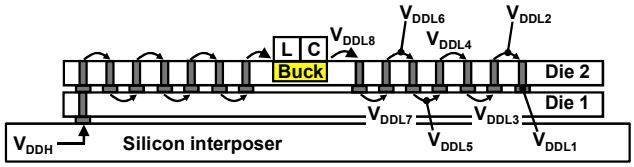
Fig. 6 illustrates the trade-off relation between the area and power overheads with sufficiently large N when V_{DDH} and V_{DDL} are 3.3 and 1.2V, respectively. For example, when η is 0.8, the area of TSV's increases by 35% with 3% TSV power overhead to reduce the IR drop from 10% to 2.5%. This indicates that the IR drop improvement by a factor of four is possible with a reasonable overhead by the BCT scheme.

4. Fabricated 3D stacked-die system

The details of a fabricated 3D stacked-die system are described in this section. First, the technology aspect is summarized. The cross sectional view of the fabricated stacked dies and silicon interposer is shown in Fig. 7. Two face-up dies are stacked on top of a silicon interposer with a via-last process. The diameter of the TSV is 20μm and the minimum pitch of the TSV's is 50μm. The resistance of a TSV link is 29mΩ (typical). In this 3D integration technology, all dies are face-up and the off-chip components are mounted on the surface of the top die. When the top die is face-down, the off-chip components will be mounted at the back of the top die through TSV's.



(a) Actual stacked-die setup



(b) Emulated setup

Fig. 8 8-die stack is emulated by making current go through TSV's repeatedly. In the figures, many parallel vias are expressed as one via for simplicity.

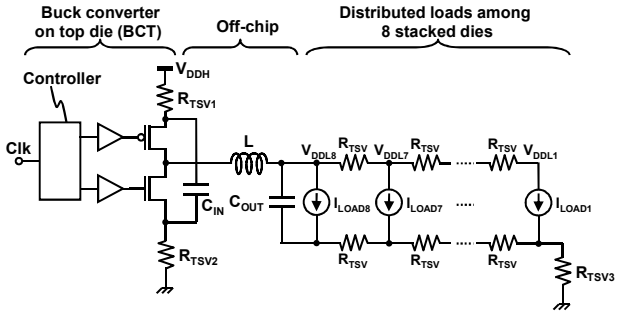


Fig. 9 Circuit diagram of 3D stacked-die system.

The technology used to implement circuits is 8-metal, 90nm CMOS. The typical operation voltage for logic transistors is 1.2V while I/O transistors accept typically 3.3V. Thus, 3.3V is used for V_{DDH} and 1.2V for V_{DDL} in the 3D stacked-die system design.

Although only two dies are stacked physically, 8-die stack case (Fig. 8 (a)) is emulated by the daisy chain of TSV's in two stacked dies (Fig. 8 (b)), where the current go through dies repeatedly. The circuit diagram of the 3D stacked-die system is shown in Fig. 9. V_{DDH} is 3.3V and V_{DDL8} is 1.2V. A constant current load is emulated by a transistor in the saturation region. Each V_{DDL} (V_{DDL1} ~ V_{DDL8}) has a current load to emulate the current consumed by the load circuits in each die. The typical current of the current load is 200mA and the corresponding output current of the buck converted is 1.6A (= 200mA x 8).

A microphotograph of the fabricated two stacked dies mounted on top of a silicon interposer is shown in Fig. 10. The silicon interposer is needed to accept 50μm pitch TSV's, which cannot be realized by a PCB board whose design rule is loose. The die size is 5.0mm x 5.0mm. Two identical buck converters are implemented on a die to expect yield improvement in this 3D stacked-die system.

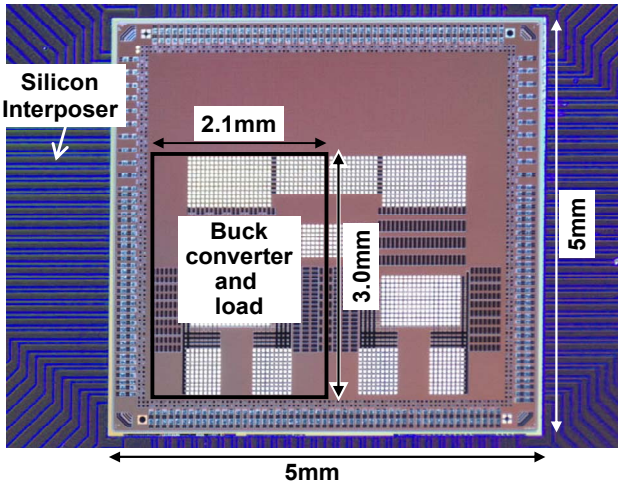


Fig. 10 Two stacked dies using TSV's are mounted on top of a silicon interposer.

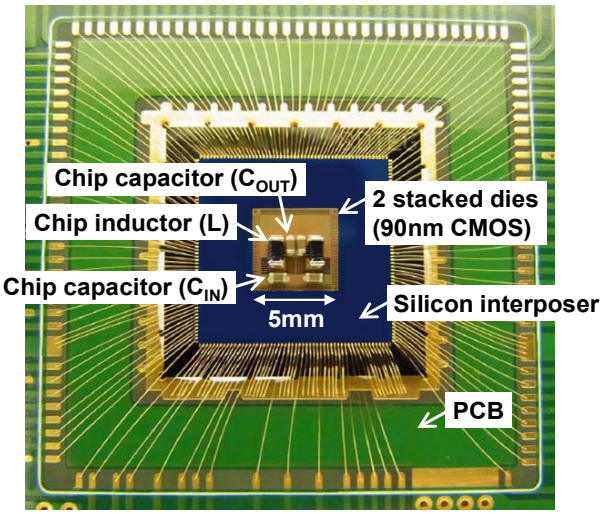


Fig. 11 Photograph of assembled system on a PCB board. Chip inductor and chip capacitor are mounted directly on top of stacked dies at the center of the photo.

The photo in Fig. 11 shows an assembled 3D stacked-die device. A chip inductor and two chip capacitors are directly mounted on the top die. The blue part in the picture is a silicon interposer.

The chip inductor for a buck converter is 3.9nH in inductance with 40mΩ parasitic resistance, whose size is 1.6 x 0.8 x 0.8mm^3 and the chip capacitor is 1μF in capacitance with the size of 1.0 x 0.5 x 0.5mm^3. The same chip capacitor is also placed at the input terminal of the buck converter signified as C_{IN} in Fig. 9. These values are chosen to optimize the buck converter design following the design theory described in [5].

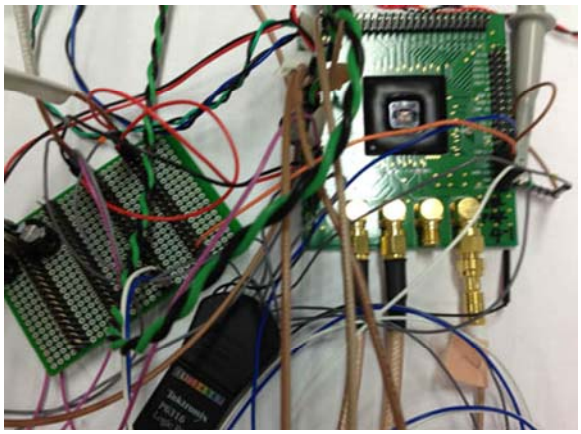


Fig. 12 Measurement setup.

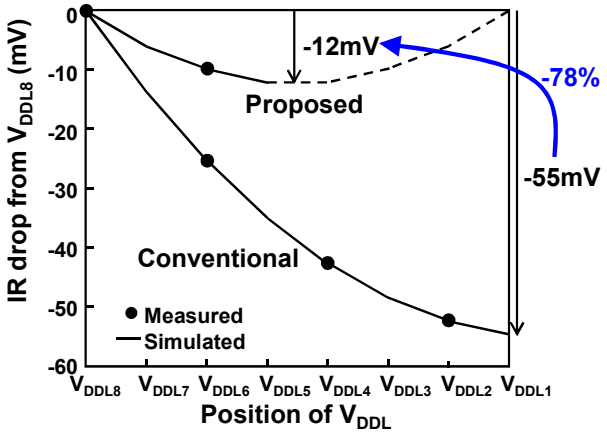


Fig. 13 Measured IR drop and simulated results.

5. Measurement results

The whole measurement setup is shown in Fig. 12. The estimated efficiency of the buck converter is 72% from the measured data. The efficiency of the buck converter could be further improved with more advanced design practice. The chopping frequency of the buck converter is 62MHz. The adopted control scheme for the fabricated buck converter is simple without any feedback control.

Fig. 13 shows the measured and simulated data. The simulation results are obtained using SPICE. Although the voltage of only selected locations can be monitored in the manufactured 3D stacked-die system due to TSV constraints, the simulation results can be used to extrapolate the measured points since the simulation results agree very well with the measured results as is seen in Fig. 13. It is shown that the proposed scheme achieves 78% decrease in IR voltage drop compared with the conventional approach. That is, the IR drop is reduced to less than 1/4 by introducing the BCT scheme. The 78% reduction is consistent with (9) with N = 8.

6. Conclusions

In this paper, the Buck Converter on Top die (BCT) scheme is proposed and the theory for the IR drop improvement and the overhead associated with the BCT scheme is elaborated. It is revealed that the IR drop improvement by a factor of more than four is possible with a reasonable overhead by the BCT scheme. It is worth mentioning that the number of TSV's is to be quadrupled for reducing the IR drop to 1/4 in the conventional approach.

A 3D stacked-die system is fabricated and the effectiveness of the proposed BCT scheme is demonstrated through measurements. For the future when the number of stacked dies is increased, the importance of the proposed scheme will become of much more importance.

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