Increase of Crosstalk Noise Due to Imbalanced Threshold Voltage Between nMOS and pMOS in Subthreshold Logic Circuits

Hiroshi Fuketa, *Member, IEEE*, Ryo Takahashi, *Student Member, IEEE*, Makoto Takamiya, *Member, IEEE*, Masahiro Nomura, *Member, IEEE*, Hirofumi Shinohara, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—An abnormal increase in crosstalk noise in subthreshold logic circuits is observed for the first time. When the threshold voltages (V_{TH}) of nMOS and pMOS are imbalanced and the on-resistance of the aggressor driver is much lower than that of the victim driver, large crosstalk noise is observed, because the on-resistance has an exponential dependence on V_{TH} in the subthreshold region being different from normal voltage operations. A simple crosstalk noise model is also proposed and verified with SPICE simulations. In a crosstalk noise test chip with a 1.5-mm interconnect in 40-nm CMOS at a power supply voltage (V_{DD}) of 0.3 V, the measured noise amplitude increases from 32% of V_{DD} to 71% of V_{DD}, when V_{TH} imbalance is realized by tuning body bias in pMOS. This body bias tuning can be used to mitigate the crosstalk problem in chip designs. For noise induced by a rising edge, the noise becomes largest under the slow-nMOS/fast-pMOS corner condition, while for noise induced by a falling edge, the noise becomes largest under the fast-nMOS/slow-pMOS corner condition, which is explained by the proposed model.**

***Index Terms*—Crosstalk, manufacturing variability, noise measurement, signal integrity, subthreshold circuit.**

I. Introduction

SUBTHRESHOLD circuits, which operate at a supply voltage (V_{DD}) lower than threshold voltage (V_{TH}), are one of the promising solutions to achieve ultra-low power operation [1]. The delay of subthreshold circuits, however, shows large variations due to V_{TH} variation, since transistor current in the subthreshold region shows an exponential dependence on V_{TH}. Therefore, many researchers have focused on investigating circuit techniques to cope with such a large delay variation [2], [3]. In contrast, there are few reports on crosstalk noise in subthreshold circuits [4], although many papers have been published on crosstalk noise in above-threshold circuits [5]–[7]. In these works, the dependence of crosstalk noise on V_{DD} has not been clarified. If the crosstalk noise in subthreshold circuits is larger than the crosstalk noise in above-threshold circuits, a new sign-off condition for crosstalk check should be developed.

Therefore, in this paper, interline-coupled crosstalk noise in subthreshold circuits is measured in a 40-nm CMOS test chip. In addition, a new crosstalk noise model is proposed and verified with SPICE simulations. An abnormal increase in crosstalk noise in the subthreshold operation is observed for the first time. This abnormal noise is caused by the pMOS/nMOS strength imbalance. The major cause of such imbalance in the subthreshold region is the difference between pMOS V_{TH} and nMOS V_{TH}. This V_{TH} imbalance mainly comes from within-die V_{TH} variation and/or die-to-die V_{TH} variation. The within-die variation can be reduced by employing wider MOSFET's but die-to-die variation is difficult to reduce by a designers' practice other than making use of adaptive body biasing. It should be noted that although the V_{TH} balance is perfect in the above-threshold voltage region, the V_{TH} imbalance may develop in the subthreshold region by the imbalance of the drain induced barrier lowering (DIBL) effect between pMOS and nMOS. As such, cares must be taken for the abnormal crosstalk noise increase in the subthreshold region.

The preliminary work of this paper is presented in [8]. The contributions of this paper beyond the preliminary work are as follows: 1) rising crosstalk noise is investigated with measurements and simulations in addition to falling noise, 2) the detailed derivation of the crosstalk noise model proposed in this paper is explained and the accuracy of the model is discussed, 3) the accuracy of the noise peak detector, which is a circuit block for measuring the peak voltage of crosstalk noise in the test chip, is explained, and 4) an impact of crosstalk noise on signal delays is investigated.

This paper is organized as follows. Section II describes the silicon measurements of crosstalk noise and shows its dependence on the V_{TH} difference. To investigate the dependence, a new crosstalk noise model for subthreshold circuits is proposed in Section III. An impact of crosstalk noise on signal delays is evaluated in Section IV. Finally, Section V concludes this paper.

II. Measurement of Crosstalk Noise

A. Test Chip Design

To measure the dependence of crosstalk noise on V_{DD} and V_{TH}s of nMOS and pMOS, a crosstalk noise test chip is designed and fabricated in a 40-nm CMOS. Fig. 1 shows a circuit diagram for measuring the peak noise voltage induced by

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H. Fuketa and R. Takahashi are with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan (e-mail: fuketa@iis.u-tokyo.ac.jp).

M. Takamiya is with the VLSI Design and Education Center, Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan.

M. Nomura and H. Shinohara are with the Semiconductor Technology Academic Research Center (STARC), Kanagawa 222-0033, Japan.

T. Sakurai is with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan.

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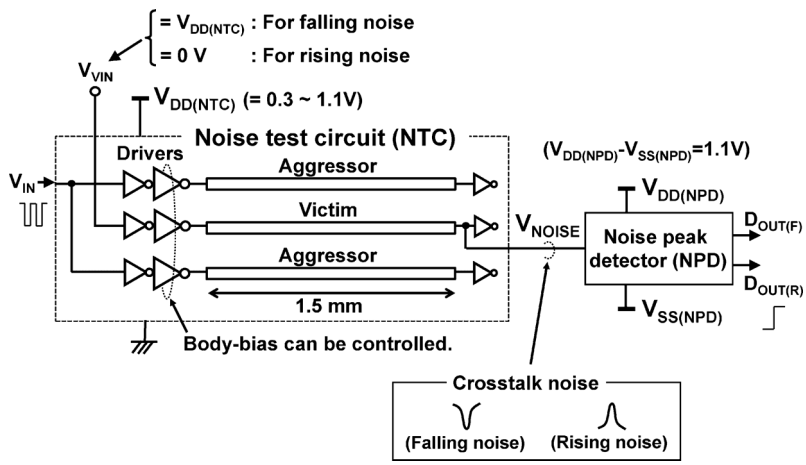

Fig. 1. Circuit diagram of crosstalk noise measurement circuit.

crosstalk. In this paper, rising and falling crosstalk noises are defined as the noises induced by a rising edge and a falling edge, respectively, as shown in Fig. 1. The measurement circuit consists of a noise test circuit (NTC), which includes 1.5-mm coupled wire lines, and a noise peak detector (NPD). A long (1.5 mm) wire is used in the measurement, because the resistance of the wire is much smaller than that of the driver in the subthreshold region, and hence many repeaters are not required. Crosstalk noise is measured over a wide range of supply voltages of the NTC ($V_{DD(NTC)}$). In this measurement circuit, rising and falling crosstalk noises can be measured. The rising crosstalk noise is induced by asserting the inputs of the aggressor line drivers (V_{IN}) while the input of the victim line driver (V_{VIN}) is kept to be the ground. In contrast, the falling crosstalk noise is caused by negating the inputs of the aggressor line drivers (V_{IN}) while the input of the victim line driver (V_{VIN}) is kept to be $V_{DD(NTC)}$. In addition, the body-bias voltage of the wire line drivers can be controlled to investigate the dependence of the V_{TH} difference between nMOS and pMOS on crosstalk noise.

Fig. 2 shows a schematic of the NPD, which detects the peak voltage of crosstalk noise. The Schmitt trigger buffer converts a noise that exceeds the logical threshold voltage of the buffer ($V_{DETECT(R)}$ or $V_{DETECT(F)}$) to a pulse. $V_{DETECT(R)}$ and $V_{DETECT(F)}$ are used for detecting the peak voltages of rising and falling noises, respectively. A rising crosstalk noise that exceeds $V_{DETECT(R)}$ is converted to a rising pulse and the pulse is captured by the NOR RS latch. Consequently, the output of the latch ($D_{OUT(R)}$) becomes high. On the other hand, a falling crosstalk noise that dips below $V_{DETECT(F)}$ is converted to a falling pulse and the pulse is captured by the NAND RS latch. Then, the output of the latch ($D_{OUT(F)}$) becomes high. The Schmitt trigger buffer is used to widen the pulse. Reset_R and Reset_F signals in Fig. 2 reset the latches. The voltage difference between the supply voltage ($V_{DD(NPD)}$) and the ground ($V_{SS(NPD)}$) of the NPD is fixed to 1.1 V regardless of $V_{DD(NTC)}$. $V_{DETECT(R)}$ and $V_{DETECT(F)}$ are varied by changing both $V_{DD(NPD)}$ and $V_{SS(NPD)}$. As shown in Fig. 3, falling noise peak voltage (V_{PEAK}) is measured by the following procedure:

1) $V_{DD(NPD)}$ and $V_{SS(NPD)}$ are set to low voltages;

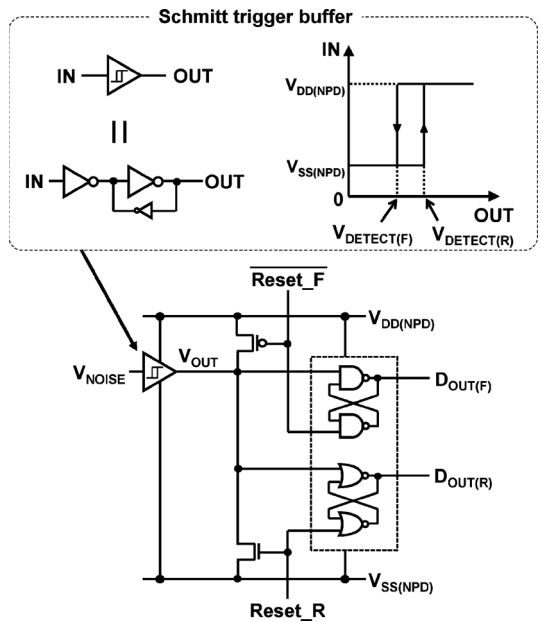

Fig. 2. Schematic of noise peak detector (NPD) in measurement circuit shown in Fig. 1.

2) a falling transition signal is given to aggressor lines, while the victim line is kept high;
3) if the output of the latch ($D_{OUT(F)}$) becomes high, $V_{DD(NTC)}$–$V_{DETECT(F)}$ is the peak noise voltage (V_{PEAK}). On the other hand, if D_{OUT} remains low, we increase $V_{DD(NPD)}$ and $V_{SS(NPD)}$ to raise $V_{DETECT(F)}$.

Then, steps 2 and 3 are repeated until the noise is detected. The peak voltage of the rising noise can be measured in a similar manner.

$V_{DETECT(F)}$ and $V_{DETECT(R)}$ must be calibrated to measure V_{PEAK}, because they are fluctuated due to die-to-die variations. Fig. 4 shows the calibration flow of $V_{DETECT(F)}$. During the calibration, no crosstalk noise is generated. Therefore, the exact $V_{DETECT(F)}$ is measured by sweeping both $V_{DD(NPD)}$ and $V_{SS(NPD)}$, because $V_{DETECT(F)}$ is equal to $V_{DD(NTC)}$ at the rising edge of $D_{OUT(F)}$. $V_{DETECT(R)}$ is calibrated in a similar manner.

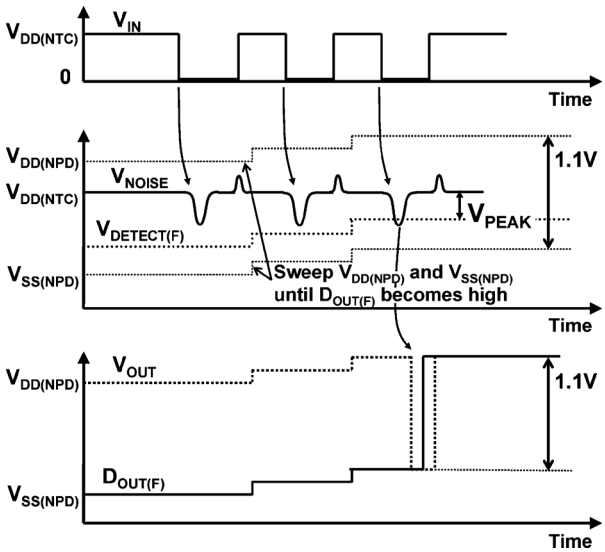

Fig. 3. Timing chart for detecting peak voltage of falling crosstalk noise. Rising noise can also be measured by a similar mechanism.

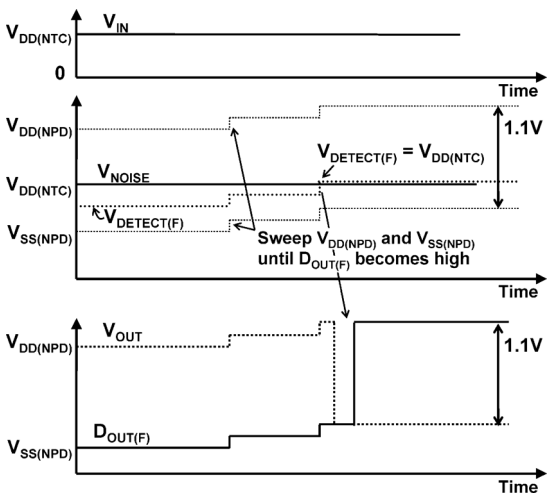

Fig. 4. Calibration flow for $\mathrm{V_{DETECT(F)}}$. $\mathrm{V_{DETECT(R)}}$ can be calibrated in a similar manner.

The noises occurring in the subthreshold region are slow, and hence they can be easily measured with the NPD. However, it is difficult to accurately measure the peak voltages of fast and sharp noises that often occur in the nominal supply voltage region. Fig. 5 shows the simulated relative error between the actual crosstalk noise voltage and the noise voltage detected by the NPD. The relative error is less than 4% below 0.5 V, whereas it is around 10% above 0.7 V. Such error in the nominal supply voltage region is not critical, since the dependence of crosstalk noise on the supply voltage is investigated and especially crosstalk noise in the subthreshold region is focused on in this work.

Fig. 6 shows the cross section of the coupled wire lines in NTC. The orthogonal lines (M2-5 and M7) are inserted as dummy metals. The output resistances of the drivers are around 160 Ω at $\mathrm{V_{DD}} = 1.1$ V. The chip micrograph is shown in Fig. 7. The measurement circuit was fabricated in a 40-nm CMOS process with seven metal layers.

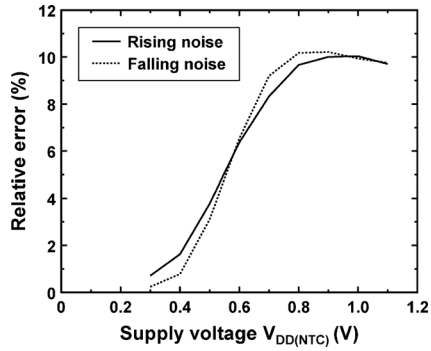

Fig. 5. Simulated relative errors between actual crosstalk noise voltage and noise voltage detected by NPD (Fig. 2).

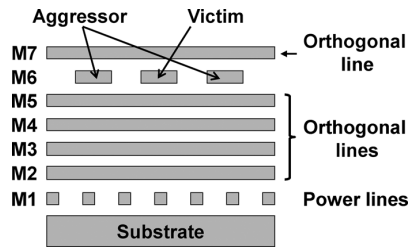

Fig. 6. Cross section of coupled wire lines in NTC.

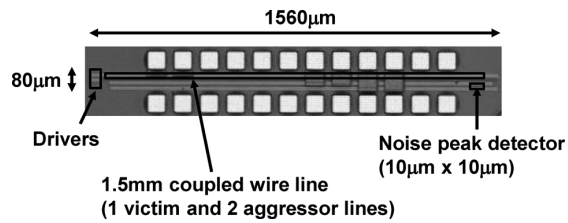

Fig. 7. Chip micrograph in 40-nm CMOS.

B. Measurement Results

Fig. 8(a) and (b) show the measured and simulated peak voltages of the rising and falling crosstalk noises as functions of the supply voltage, respectively. The SPICE simulations are conducted with the parasitic wire resistance and capacitance extracted from the layout data. $\mathrm{V_{TH}}$ used in the simulations is based on the measured single transistors provided by the foundry. The simulation results agree with the measurement results. Fig. 8 indicates that $\mathrm{V_{PEAK}/V_{DD(NTC)}}$ sharply decreases as $\mathrm{V_{DD(NTC)}}$ is reduced for the rising crosstalk noise, while $\mathrm{V_{PEAK}/V_{DD(NTC)}}$ slightly decreases for the falling crosstalk noise. Details of these dependences will be discussed in Section III.

In order to examine how the $\mathrm{V_{TH}}$ difference between nMOS and pMOS affects peak noise voltage, the dependence of peak noise voltage on the body-bias voltage of the victim driver is measured. The measurement results are illustrated in Fig. 9. The body-bias voltages of the aggressor line drivers do not change. As body-bias voltage of n-well of the victim line driver ($\mathrm{V_{NW}}$–$\mathrm{V_{DD(NTC)}}$) increases, $\mathrm{V_{TH}}$ of pMOS of the victim line driver decreases, which enlarges the $\mathrm{V_{TH}}$ difference between pMOS and nMOS. Fig. 9 shows that the peak noise voltage at

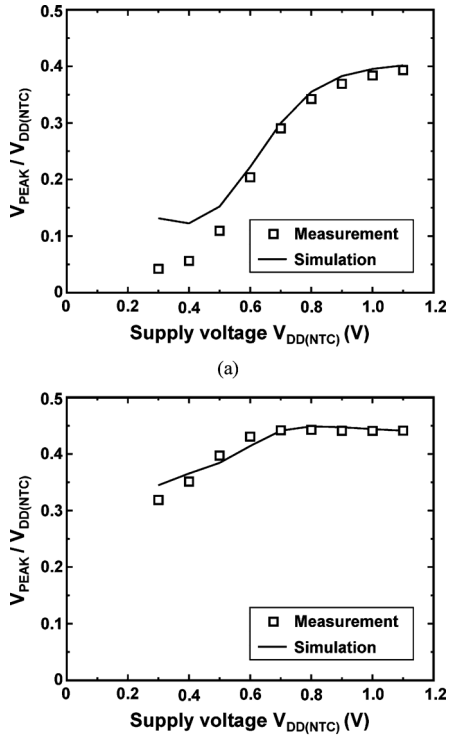

Fig. 8. Measured and simulated peak voltages ($\mathrm{V_{PEAK}}$) as functions of supply voltage of NTC ($\mathrm{V_{DD(NTC)}}$). (a) Rising noise. (b) Falling noise.

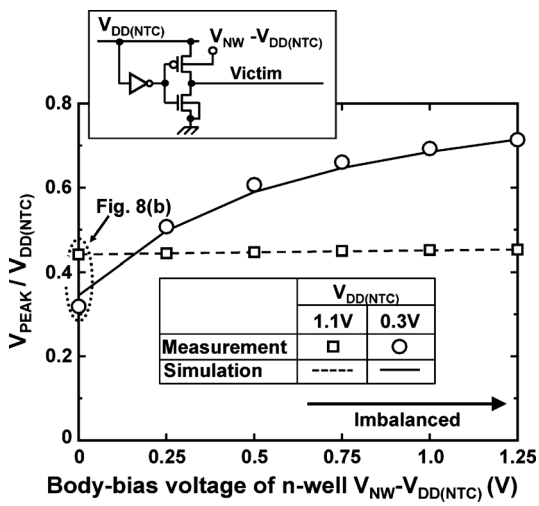

Fig. 9. Measured and simulated dependences of peak noise voltage ($\mathrm{V_{PEAK}}$) on the n-well body-bias voltage of victim driver. Noise peak voltage is significantly sensitive to the $\mathrm{V_{TH}}$ balance in subthreshold circuits.

a nominal supply voltage of 1.1 V hardly depend on the n-well body-bias voltage of the victim driver, whereas the peak noise voltage at $\mathrm{V_{DD(NTC)}}$ of 0.3 V significantly increases as reverse body-bias becomes large. Noise amplitude increases from 32% of $\mathrm{V_{DD}}$ to 71% of $\mathrm{V_{DD}}$, when the $\mathrm{V_{TH}}$ imbalance is realized by tuning the body bias in pMOS. This indicates that peak noise voltage is extremely sensitive to the balance of $\mathrm{V_{TH}}$ between nMOS and pMOS in subthreshold circuits. The reason why the balance of $\mathrm{V_{TH}}$ significantly affects peak noise voltage is discussed in the next section.

III. Modeling of Crosstalk Noise in Subthreshold Region

A. Crosstalk Noise in Coupled Wire Lines With One Aggressor

First, crosstalk noise by one aggressor line is investigated for simplicity. Fig. 10 illustrates the equivalent circuit of the coupled wire lines with one aggressor and one victim, where $\mathrm{C_W}$ denotes the wire capacitance and $\mathrm{C_C}$ represents the coupling capacitance between the aggressor and the victim.

In this paper, $\mathrm{R_{5N}}$ ($\mathrm{R_{5P}}$) and $\mathrm{R_{3N}}$ ($\mathrm{R_{3P}}$) are the equivalent resistances of nMOS (pMOS), and the definition for nMOS is explained in Fig. 11. $\mathrm{R_{5N}}$ and $\mathrm{R_{5P}}$ are pentode resistances (on-resistances) given by

$$R_{5\mathrm{N(P)}} = \frac{V_{DS}}{I_{DS,\mathrm{N(P)}}@\left(V_{DS} = V_{GS} = V_{\mathrm{DD}}\right)} \tag{1}$$

where $\mathrm{I}_{DS,\mathrm{N(P)}}$ is the drain-source current of nMOS (pMOS), which is a function of drain voltage (V_{DS}) and gate voltage (V_{GS}). $\mathrm{R_{3N}}$ and $\mathrm{R_{3P}}$ are triode resistances defined as

$$R_{3\mathrm{N(P)}} = \frac{V_{DS}}{I_{DS,\mathrm{N(P)}}@\left(V_{GS} = V_{\mathrm{DD}}, V_{DS} = \frac{V_{\mathrm{DD}}}{4}\right)}. \tag{2}$$

For the rising noise, the drain-source voltage of pMOS of the aggressor line driver is $\mathrm{V_{DD}}$ at first, and hence $\mathrm{R_{5P}}$ defined in (1) is used as the equivalent resistance of pMOS. In contrast, the victim line is pulled down by nMOS of the victim line driver and the drain-source voltage of the nMOS is less than $\mathrm{V_{PEAK}}$. In this paper, the critical peak noise voltage is assumed to be half $\mathrm{V_{DD}}$. Therefore, $\mathrm{R_{3N}}$ defined in (2) that is the resistance at $\mathrm{V}_{DS} = \mathrm{V_{DD}}/4$, which is an intermediate voltage between half $\mathrm{V_{DD}}$ and the ground, is used as the equivalent resistance of nMOS of the victim line driver for the rising noise. For the falling noise, $\mathrm{R_{5N}}$ is used as the equivalent resistance of nMOS of the aggressor line driver and $\mathrm{R_{3P}}$ is used as the equivalent resistance of pMOS of the victim line driver.

In the nominal supply voltage region, the equivalent resistances of the wire line drivers ($\mathrm{R_{5N}}$, $\mathrm{R_{5P}}$, $\mathrm{R_{3N}}$, and $\mathrm{R_{3P}}$) are so small that the wire resistance ($\mathrm{R_W}$) must be taken into consideration, as shown in Fig. 10(a). On the other hand, $\mathrm{R_W}$ can be ignored in the subthreshold region, since $\mathrm{R_{5N}}$, $\mathrm{R_{5P}}$, $\mathrm{R_{3N}}$, and $\mathrm{R_{3P}}$ are much larger than $\mathrm{R_W}$. Therefore, the equivalent circuit in the subthreshold region can be easily analyzed as illustrated in Fig. 10(b).

Let $\mathrm{V}_{VIC}(\mathrm{t})$ be the voltage of the victim wire line. When the input of the aggressor line driver is asserted at $\mathrm{t} = 0$, as shown in the upper panel of Fig. 10(b), the rising noise is induced on the victim line, and in this case, $\mathrm{V_{VIC}(t)}$ is expressed as

$$V_{\mathrm{VIC}}(t) = V_{\mathrm{DD}}\frac{c}{2c+1}\frac{1}{\alpha_{r1}-\beta_{r1}} \cdot \left(e^{(\alpha_{r1}/R_{5\mathrm{P}}C_{\mathrm{W}})t} - e^{(\beta_{r1}/R_{5\mathrm{P}}C_{\mathrm{W}})t}\right) \tag{3}$$

where $\mathrm{c} = \mathrm{C_C}/\mathrm{C_W}$. α_{r1} and β_{r1} ($0 > \alpha_{r1} > \beta_{r1}$) are the solutions to the following quadratic equation

$$r_r\left(2c+1\right)x^2 + \left(r_r+1\right)\left(c+1\right)x + 1 = 0 \tag{4}$$

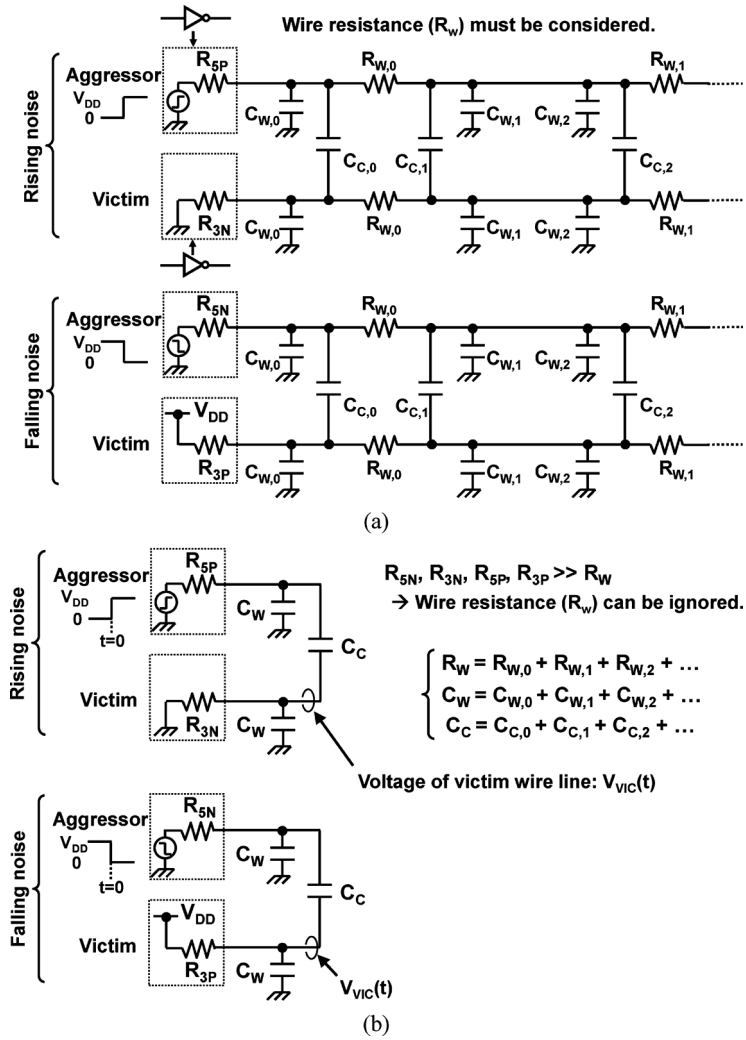

Fig. 10. Equivalent circuit of coupled wire lines with one aggressor and one victim. (a) Nominal supply voltage region (conventional). (b) Subthreshold voltage region (this work).

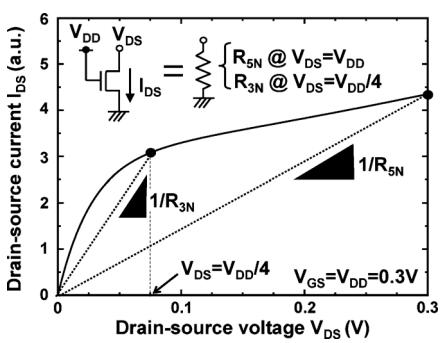

Fig. 11. Definition of equivalent resistance of nMOS.

where $r_r = R_{3N}/R_{5P}$. T_{PEAK} is defined as the time when the noise voltage becomes maximum peak and is given by

$$\left.\frac{dV_{VIC}}{dt}\right|_{t=T_{PEAK}} = 0. \tag{5}$$

Therefore, T_{PEAK} is derived as

$$T_{PEAK} = -\frac{R_{5P}C_W}{\alpha_{r1}-\beta_{r1}} \ln\left(\frac{\alpha_{r1}}{\beta_{r1}}\right). \tag{6}$$

Consequently, peak noise voltage (V_{PEAK}) for the rising noise is expressed as

$$\begin{aligned} V_{PEAK} &= V_{VIC}(T_{PEAK}) \\ &= V_{DD}\frac{c}{(2c+1)}\frac{1}{\alpha_{r1}-\beta_{r1}} \\ &\quad \cdot \left(\left(\frac{\alpha_{r1}}{\beta_{r1}}\right)^{-\alpha_{r1}/(\alpha_{r1}-\beta_{r1})} - \left(\frac{\alpha_{r1}}{\beta_{r1}}\right)^{-\beta_{r1}/(\alpha_{r1}-\beta_{r1})}\right). \end{aligned} \tag{7}$$

V_{PEAK} for the falling noise can be derived in the same manner. When the input of the aggressor line driver is negated at $t = 0$, as shown in the lower panel of Fig. 10(b), $V_{VIC}(t)$ is expressed as

$$\begin{aligned} V_{VIC}(t) = V_{DD}\Bigg(1 - \frac{c}{2c+1}\frac{1}{\alpha_{f1}-\beta_{f1}} \\ \cdot \left(e^{(\alpha_{f1}/R_{5N}C_W)t} - e^{(\beta_{f1}/R_{5N}C_W)t}\right)\Bigg) \end{aligned} \tag{8}$$

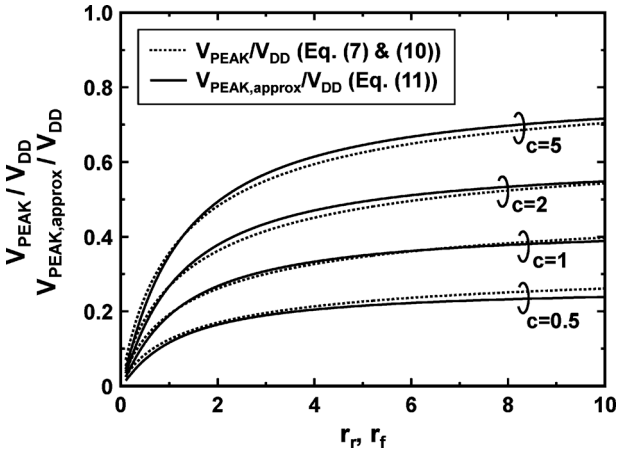

Fig. 12. Peak noise voltage ($\mathrm{V_{PEAK}}$) obtained using (7) and (10) and its approximated value ($\mathrm{V_{PEAK,approx}}$) calculated using (11) for coupled wire line with one aggressor. $\mathrm{V_{PEAK,approx}}$ is a good approximation of $\mathrm{V_{PEAK}}$.

where α_{f1} and β_{f1} ($0 > \alpha_{\mathrm{f1}} > \beta_{\mathrm{f1}}$) are the solutions to the following quadratic equation

$$r_{\mathrm{f}}\left(2c+1\right)x^2+\left(r_{\mathrm{f}}+1\right)\left(c+1\right)x+1=0 \tag{9}$$

where $\mathrm{r_f} = \mathrm{R_{3P}/R_{5N}}$. Thus, $\mathrm{V_{PEAK}}$ for the falling noise is derived as

$$V_{\mathrm{PEAK}}=V_{\mathrm{DD}}\frac{c}{(2c+1)}\frac{1}{\alpha_{\mathrm{f1}}-\beta_{\mathrm{f1}}} \cdot\left(\left(\frac{\alpha}{\beta}\right)^{-\alpha_{\mathrm{f1}}/(\alpha_{\mathrm{f1}}-\beta_{\mathrm{f1}})}-\left(\frac{\alpha}{\beta}\right)^{-\beta_{\mathrm{f1}}/(\alpha_{\mathrm{f1}}-\beta_{\mathrm{f1}})}\right). \tag{10}$$

Equations (7) and (10) are too complicated to discuss the $\mathrm{V_{PEAK}}$ dependence on $\mathrm{V_{TH}}$. A simple expression of a bound of $\mathrm{V_{PEAK}}$ has been derived in [9]. In this paper, a modification to the expression is introduced for more accurate approximation of $\mathrm{V_{PEAK}}$. $\mathrm{V_{PEAK}}$ for the rising noise given by (7) is approximated as

$$V_{\mathrm{PEAK,approx}}=V_{\mathrm{DD}}\left(\frac{r_r}{r_r+1}\cdot\frac{c}{c+1}\right)^{1.2}. \tag{11}$$

For the falling noise, $\mathrm{r_f}$ is used instead of r_r.

Fig. 12 shows $\mathrm{V_{PEAK}}$ and $\mathrm{V_{PEAK,approx}}$ to discuss the accuracy of the approximation model. This figure indicates that the proposed model is a good approximation of $\mathrm{V_{PEAK}}$. The relative error ($|\mathrm{V_{PEAK}} - \mathrm{V_{PEAK,approx}}|/\mathrm{V_{DD}}$) is less than 3.2% under the conditions of $0.1 < \mathrm{r}_r, \mathrm{r_f} < 10$ and $0.5 < \mathrm{c} < 5$. Using the expression described in [9], the relative error is less than 8.5%, and hence the proposed expression in (11) is a better approximation of $\mathrm{V_{PEAK}}$. When the lines are partially coupled, for example, the coupling capacitance ($\mathrm{C_C}$) decreases. In this case, $\mathrm{V_{PEAK}}$ is reduced, because $\mathrm{c}(= \mathrm{C_C/C_W})$ decreases, as indicated by (11).

B. Crosstalk Noise in Coupled Wire Lines With Two Aggressors

Crosstalk noise in coupled wire lines with two aggressors can be derived in the same manner. The equivalent circuit in the subthreshold region is depicted in Fig. 13. The equivalent circuit with two aggressors is converted to that with one aggressor, as shown. When the wire capacitances of the victim and aggressors are identical ($\mathrm{C_W} = \mathrm{C_{WV}} = \mathrm{C_{WA}}$), the voltage of the victim line (V_{VIC}) is given by

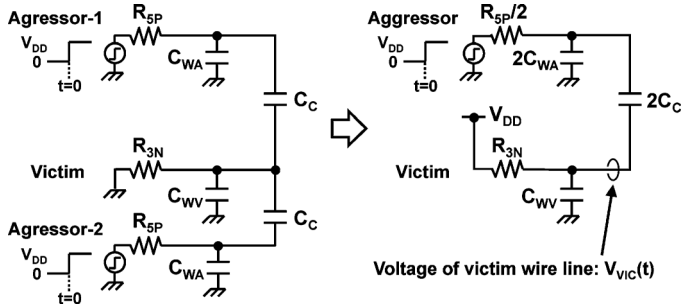

Fig. 13. Equivalent circuit of coupled wire lines with two aggressors and one victim. This circuit can be converted to a circuit with one aggressor.

$$V_{VIC}\left(t\right)=V_{\mathrm{DD}}\frac{2c}{3c+1}\frac{1}{\alpha_{r2}-\beta_{r2}} \cdot\left(e^{(\alpha_{r2}/R_{5\mathrm{P}}C_{\mathrm{W}})t}-e^{(\beta_{r2}/R_{5\mathrm{P}}C_{\mathrm{W}})t}\right) \tag{12}$$

where $\mathrm{c} = \mathrm{C_C/C_W}$. α_{r2} and β_{r2} ($0 > \alpha_{r2} > \beta_{r2}$) are the solutions to the following quadratic equation

$$r_r\left(3c+1\right)x^2+\left(2r_rc+r_r+c+1\right)x+1=0 \tag{13}$$

where $\mathrm{r}_r = \mathrm{R_{3N}/R_{5P}}$. Thus, peak noise voltage ($\mathrm{V_{PEAK}}$) in coupled wire lines with two aggressors for the rising noise is derived as

$$V_{\mathrm{PEAK}}=V_{\mathrm{DD}}\frac{2c}{(3c+1)}\frac{1}{\alpha_{r2}-\beta_{r2}} \cdot\left(\left(\frac{\alpha_{r2}}{\beta_{r2}}\right)^{-\alpha_{r2}/(\alpha_{r2}-\beta_{r2})}-\left(\frac{\alpha_{r2}}{\beta_{r2}}\right)^{-\beta_{r2}/(\alpha_{r2}-\beta_{r2})}\right). \tag{14}$$

For the falling noise, α_{f2} and β_{f2} are used instead of α_{r2} and β_{r2} in (14), respectively, where α_{f2} and β_{f2} are the solutions to the following quadratic equation

$$r_{\mathrm{f}}\left(3c+1\right)x^2+\left(2r_{\mathrm{f}}c+r_{\mathrm{f}}+c+1\right)x+1=0 \tag{15}$$

where $\mathrm{r_f} = \mathrm{R_{3P}/R_{5N}}$.

Also for the crosstalk noise with two aggressors, $\mathrm{V_{PEAK}}$ given by (14) can be approximated as

$$V_{\mathrm{PEAK,approx}}=V_{\mathrm{DD}}\left(\frac{r_r}{r_r+0.5}\cdot\frac{c}{c+0.5}\right)^{1.3}. \tag{16}$$

For the falling noise, $\mathrm{r_f}$ is used instead of r_r.

Fig. 14 shows $\mathrm{V_{PEAK}}$ and $\mathrm{V_{PEAK,approx}}$. The relative error ($|\mathrm{V_{PEAK}} - \mathrm{V_{PEAK,approx}}|/\mathrm{V_{DD}}$) is less than 4.5% under the conditions of $0.1 < \mathrm{r}_r, \mathrm{r_f} < 10$ and $0.5 < \mathrm{c} < 5$.

If the wire capacitances of the victim and aggressors are different, a slight modification of (16) is required. For example, when the wire capacitance of the aggressor is two times larger than that of the victim ($\mathrm{C_{WA}} = 2\mathrm{C_{WV}}$), $\mathrm{V_{PEAK}}$ can be approximated using a power of 1.5 instead of 1.3 in (16). In this case, the relative error is less than 5.8% under the conditions of $0.1 < \mathrm{r}_r, \mathrm{r_f} < 10$ and $0.5 < \mathrm{c} < 5$.

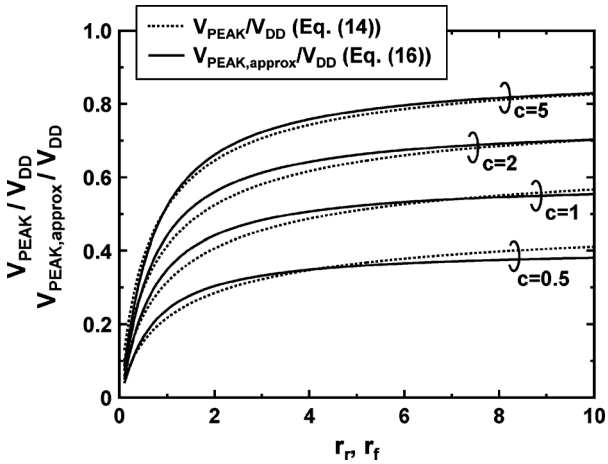

Fig. 14. Peak noise voltage ($\mathrm{V_{PEAK}}$) obtained using (14) and its approximated value ($\mathrm{V_{PEAK,approx}}$) calculated using (16) for coupled wire line with two aggressors.

C. Dependence of Peak Noise Voltage on $\mathrm{V_{TH}}$ Imbalance

According to [10], in the subthreshold region, $\mathrm{I}_{DS,\mathrm{N}}$ in (1) and (2) is given by

$$I_{DS,\mathrm{N}} = I_{0,\mathrm{N}} e^{(V_{GS}-V_{\mathrm{TH,N}}+\eta V_{DS})/nU_T}\left(1-e^{-V_{DS}/U_T}\right) \tag{17}$$

where n is the subthreshold slope parameter, η is the DIBL coefficient, U_T is the thermal voltage, $\mathrm{V_{TH,N}}$ is $\mathrm{V_{TH}}$ of nMOS, and $\mathrm{I_{0,N}}$ is the technology-dependent parameter.

From (1), (2), and (17), r_r and $\mathrm{r_f}$ can be expressed as

$$r_r = \frac{R_{3\mathrm{N}}}{R_{5\mathrm{P}}} \propto e^{(V_{\mathrm{TH,N}}-|V_{\mathrm{TH,P}}|)/nU_T} \tag{18}$$

$$r_\mathrm{f} = \frac{R_{3\mathrm{P}}}{R_{5\mathrm{N}}} \propto e^{(|V_{\mathrm{TH,P}}|-V_{\mathrm{TH,N}})/nU_T} \tag{19}$$

where $\mathrm{V_{TH,P}}$ is $\mathrm{V_{TH}}$ of pMOS. These equations indicate that r_r and $\mathrm{r_f}$ have exponential dependences on the $\mathrm{V_{TH}}$ difference between nMOS and pMOS. According to (11) and (16), peak noise voltage ($\mathrm{V_{PEAK}}$) depends on r_r and $\mathrm{r_f}$, and is enlarged by increases in r_r and $\mathrm{r_f}$. Thus, peak noise voltage is strongly affected by the $\mathrm{V_{TH}}$ difference between nMOS and pMOS. r_r is maximized at the SF (slow-nMOS/fast-pMOS) process corner, while $\mathrm{r_f}$ is maximized at the FS (fast-nMOS/slow-pMOS) process corner. Therefore, crosstalk noise is especially crucial at process corners, such as the SF corner for the rising noise and the FS corner for the falling noise.

Fig. 15(a) and (b) show the simulated peak noise voltage on the 1.5-mm coupled wire line with one victim and two aggressors under a typical process condition (TT) and the corner conditions (SF and FS) for the rising noise and falling noise, respectively. $\mathrm{V_{PEAK}/V_{DD}}$ at 0.3 V is 1.1 times larger than $\mathrm{V_{PEAK}/V_{DD}}$ at 1.1 V for the rising noise under the SF corner condition and 1.4 times larger for the falling noise under the FS corner condition. The approximated peak noise ($\mathrm{V_{PEAK,approx}}$) calculated using (16) is also shown, and it agrees with the simulation results. The measured $\mathrm{V_{PEAK}}$ dependences shown in Fig. 8 are different from the $\mathrm{V_{PEAK}}$ dependences obtained by simulations shown in Fig. 15 because the $\mathrm{V_{TH}}$ balance of the measured chip is between TT and SF.

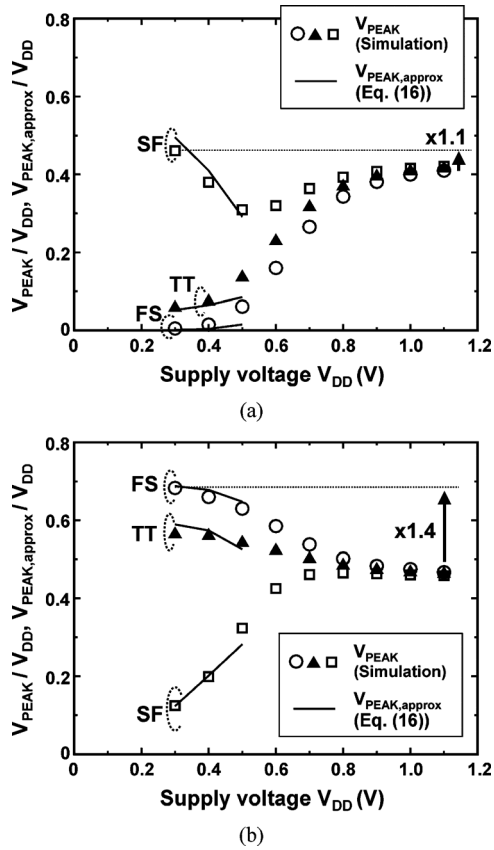

Fig. 15. Peak voltage of crosstalk noise on 1.5-mm coupled wire line with two aggressors and one victim at TT, FS, and SF process corners. $\mathrm{V_{PEAK}}$ is obtained by SPICE simulations and $\mathrm{V_{PEAK,approx}}$ is calculated using the proposed approximation model equation. (a) Rising noise. (b) Falling noise.

As shown in Fig. 15, crosstalk noise in the nominal supply voltage region hardly depends on the $\mathrm{V_{TH}}$ balance. This is because 1) the dependence of the equivalent resistances of the drivers on $\mathrm{V_{TH}}$ is much smaller than that in the subthreshold region, and 2) the influence of wire resistances is not ignored. In contrast, peak noise voltage in the subthreshold region is much more sensitive to the $\mathrm{V_{TH}}$ balance. This is because peak noise voltage depends on equivalent resistance ratios (r_r and $\mathrm{r_f}$), which have an exponential dependence on the $\mathrm{V_{TH}}$ difference between nMOS and pMOS, as indicated in (18) and (19). Therefore, designers must consider the process corners, such as the SF and FS corner conditions, as the worst-case conditions for signal integrity in subthreshold circuits.

IV. Delay Degradation due to Crosstalk Noise in Subthreshold Region

In this section, an impact of crosstalk noise on signal delays is investigated. For analyzing the peak voltage of crosstalk noise ($\mathrm{V_{PEAK}}$), the input signal of the victim line driver is fixed to the ground or $\mathrm{V_{DD}}$ as shown in Fig. 10. In contrast, the victim line is also driven for analyzing the influence of crosstalk noise on delays as shown in Fig. 16(a), and the signal delay on the victim line is evaluated. Fig. 16(b) illustrates a timing chart when the falling transition signal is input to the aggressor line driver ($\mathrm{V_{IN(A)}}$) (crosstalk noise is induced) or $\mathrm{V_{IN(A)}}$ is kept

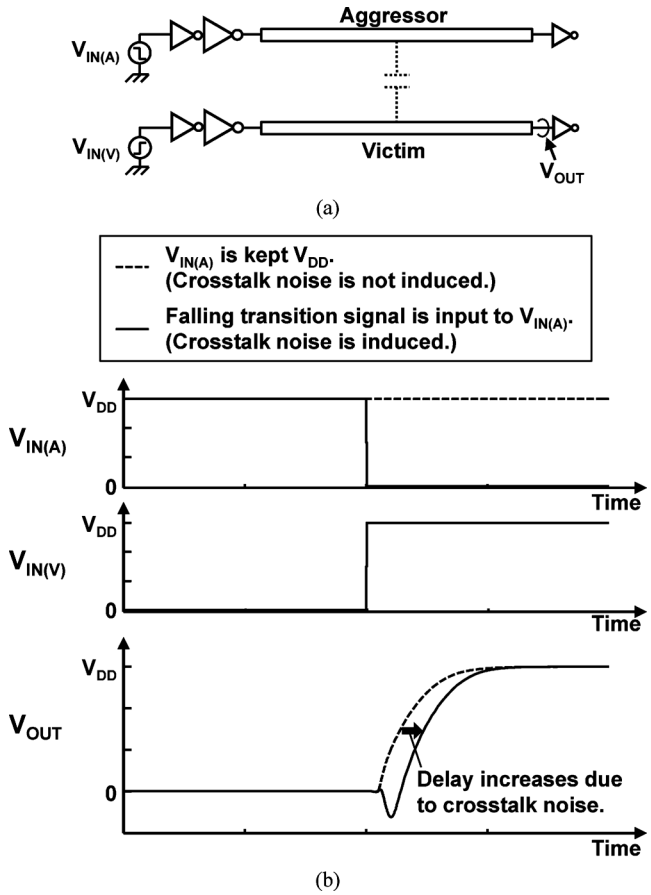

Fig. 16. (a) Circuit diagram for evaluating signal delays and (b) timing chart.

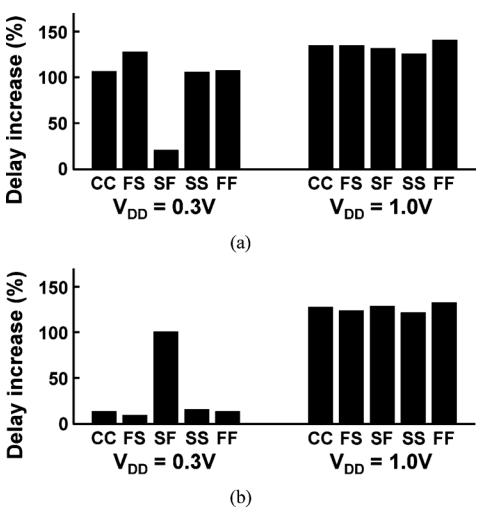

Fig. 17. Simulated maximum delay increase due to crosstalk noise 1.5-mm coupled wire line with two aggressors and one victim under TT and process corners. (a) Delay increase of rising transition. (b) Delay increase of falling transition.

V_{DD} (crosstalk noise is not induced). The rising transition delay on the victim line increases due to the crosstalk noise. For evaluating the falling transition delay, the rising transition signal is input to $V_{IN(A)}$. The falling transition delay also increases due to the crosstalk noise.

Fig. 17 shows the simulated maximum delay increase on the 1.5-mm coupled wire line with one victim and two aggressors under TT and process corners (FS, SF, SS, FF) when V_{DD} is 1.0 and 0.3 V. The delay increase is derived by dividing the maximum delay increase, which is induced by crosstalk noise, by the delay without crosstalk noise. The delay increase at $V_{DD} = 0.3$ V is much more sensitive to process variations than that at $V_{DD} = 1.0$ V. The delay increase of the rising transition is largest under the FS corner condition and smallest under the SF corner condition, since the falling crosstalk noise is largest under the FS corner condition and smallest under the SF corner condition as shown in Fig. 15(b). On the other hand, the delay increase of the falling transition is largest under the SF corner condition and smallest under the FS corner condition. This means V_{TH} imbalance causes the large delay increase in the subthreshold region.

V. Conclusions

In this paper, the dependence of the peak noise voltage induced by crosstalk on the V_{TH} difference between nMOS and pMOS in subthreshold circuits was presented. The large crosstalk noise due to the V_{TH} imbalance was measured in the test chip with 1.5-mm coupled wires fabricated by a 40-nm CMOS process. A new crosstalk noise model was proposed and verified with SPICE simulations. The proposed model indicates that peak noise voltage is significantly sensitive to the V_{TH} difference. Simulation results show that the rising crosstalk noise is largest under the SF corner condition, while the falling noise is largest under the FS corner condition. In the worst-case FS corner simulation, noise amplitude increased by 1.4 times when V_{DD} was reduced from 1.1 to 0.3 V. These results were explained by the proposed model. In addition, the impact of crosstalk noise on signal delays was investigated. Simulation results show that the delay increase due to crosstalk noise at $V_{DD} = 0.3$ V is much more sensitive to process variations than that at $V_{DD} = 1.0$ V and V_{TH} imbalance causes the large delay increase in the subthreshold region.

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Hiroshi Fuketa (S'07–M'10) received the B.E. degree from Kyoto University, Kyoto, Japan, in 2002 and the M.E. and Ph.D. degrees in information systems engineering from Osaka University, Osaka, Japan, in 2008 and 2010, respectively.

He is currently a Research Associate with Institute of Industrial Science, the University of Tokyo, Tokyo, Japan. His research interests include ultra-low-power circuit design and variation modeling.

Dr. Fuketa is a member of IEICE and IPSJ.

Ryo Takahashi (S'12) received the B.Eng. degree in electrical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 2009, and the M.S.E.E. degree from the University of Tokyo, Tokyo, Japan, in 2011. He is currently working toward the Ph.D. in electrical engineering at the University of Tokyo.

His research is focused on the design of low-voltage low-power circuits.

Makoto Takamiya (S'98–M'00) received the B.S., M.S., and Ph.D. degrees in electronic engineering from the University of Tokyo, Japan, in 1995, 1997, and 2000, respectively.

In 2000, he joined NEC Corporation, Japan, where he was engaged in the circuit design of high speed digital LSI's. In 2005, he joined University of Tokyo, Japan, where he is an Associate Professor of VLSI Design and Education Center. His research interests include the circuit design of the low-power RF circuits, the ultra low-voltage logic circuits, the low-voltage DC-DC converters, and the large area electronics with organic transistors.

Dr. Takamiya is a member of the technical program committee for the *IEEE Symposium on VLSI Circuits*. He received the 2009 and 2010 IEEE Paul Rappaport Awards.

Masahiro Nomura (M'96) received the B.E. and M.E. degrees in electrical engineering and the Ph.D. degree in information sciences from Tohoku University, Sendai, Japan, in 1989, 1991, and 2007, respectively.

He joined NEC Corporation, Sagamihara, Japan, in 1991. He was initially engaged in the research and development of high-speed video signal processors, high-speed microprocessors, and low-power multiprocessors. He transferred to NEC Electronics Corporation and Renesas Electronics Corporation in 2008 and 2010, respectively, and has been a Senior Researcher at the LSI Research Laboratory, Renesas Electronics Corporation, Kawasaki, Japan. Since 2009, he has been concurrently serving as a Manager of logic design at the Semiconductor Technology Academic Research Center. His current research interests include low-power, high-speed circuit techniques and reconfigurable circuit techniques.

Dr. Nomura is a member of the Institute of Electronics, Information, and Communication Engineers (IEICE) of Japan and the IEEE Solid-State Circuits Society. He served as a technical program committee member of the A-SSCC in 2005, 2006, 2007, 2008, and 2009, and the Symposium on VLSI Circuits in 2009 and 2010.

Hirofumi Shinohara received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree in informatics from Kyoto University, in 1976, 1978, and 2008, respectively.

In 1978, he joined the LSI Laboratory of Mitsubishi. Electric Corporation, where he was involved in research and development of MOS SRAMs, embedded memory compilers and logic blocks. From 2003 to 2009 he was a Manager of basic logic and memory circuits development department in Renesas Technology Corporation. In 2009 he moved to STARC, where he has been managing a joint research project on extremely low power circuits and systems with universities in Japan. His research interests include advanced SRAM, low-power circuits, and variation-aware design.

Dr. Shinohara is a member of IEICE.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1981.

In 1981 he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC Solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 through 1990, he was a visiting Researcher at the University of California Berkeley, where he conducted research in the field of VLSI CAD. From 1996, he has been a Professor at the University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic IC's and large-area electronics. He has published more than 400 technical publications including 100 invited presentations and several books and filed more than 200 patents.

He is a Fellow of STARC and IEICE. He gave keynote speech at more than 50 conferences including *ISSCC*, *ESSCIRC*, and *ISLPED*. He was an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS Distinguished Lecturer. He is an executive committee Chair for the *VLSI Symposia* and a steering committee Chair for the *IEEE A-SSCC* since 2010. He served as a conference Chair for the *Symposium on VLSI Circuits*, and *ICICDT*, a Vice Chair for *ASPDAC*, a TPC Chair for the *A-SSCC*, and *VLSI Symposium*, an executive committee member for ISLPED, and a program committee member for *ISSCC*, *CICC*, *A-SSCC*, *DAC*, *ESSCIRC*, *ICCAD*, *ISLPED*, and other international conferences. He is a recipient of the 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, the 2009 and 2010 IEEE Paul Rappaport Awards, the 2010 IEICE Electronics Society Award, the 2009 Achievement Award of IEICE, the 2005 IEEE ICICDT Award, the 2004 IEEE Takuo Sugano Award, the 2005 P&I patent of the year award, and four product awards.