

Variation-aware Subthreshold Logic Circuit Design

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Abstract

Subthreshold logic circuits are one of promising solutions to achieve ultra-low power operation. However, subthreshold circuits are significantly sensitive to manufacturing and environmental variability. In this paper, we will discuss design challenges in subthreshold logic circuits, such as rise in a minimum operating voltage, signal integrity degradation, and large delay variations.

1. Introduction

Subthreshold logic circuits, which operate at lower supply voltage than threshold voltage (V_{TH}), are one of promising solutions to achieve ultra-low power operation [1]. Fig. 1 shows simulated delay, power, and energy (power delay product) of a CMOS logic circuit [2]. As the supply voltage (V_{DD}) is reduced, the delay increases, whereas the power significantly decreases. Therefore, subthreshold logic circuits are suitable for low-power applications in which circuit speed is not a primary concern or can be compensated by parallelization. For such applications, energy is a key metric. As shown in Fig. 1, the energy has its optimum value (E_{opt}) at $V_{DD}=V_{opt}$. Thus, V_{opt} is the target supply voltage for ultra-low-power applications. V_{opt} is around 0.3V for typical logic circuits [2].

Subthreshold circuits are, however, extremely sensitive to manufacturing and environmental (e.g. temperature) variability, because I-V characteristics of MOSFET's in the subthreshold region have an exponential dependence on V_{TH} . In this paper, the following three challenges in subthreshold circuit design induced by such variability are discussed; 1) rise in a minimum operating voltage (V_{DDmin}), 2) signal integrity degradation due to crosstalk noise, and 3) large delay variations.

2. Minimum operating voltage (V_{DDmin})

Reducing V_{DD} could cause functional errors. The supply voltage at which the first functional error occurs is defined as a minimum operating voltage (V_{DDmin}). The

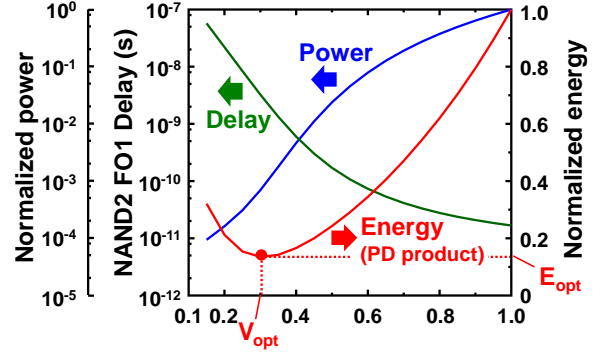


Fig. 1. Simulated dependence of power, delay, and energy of CMOS logic circuit.

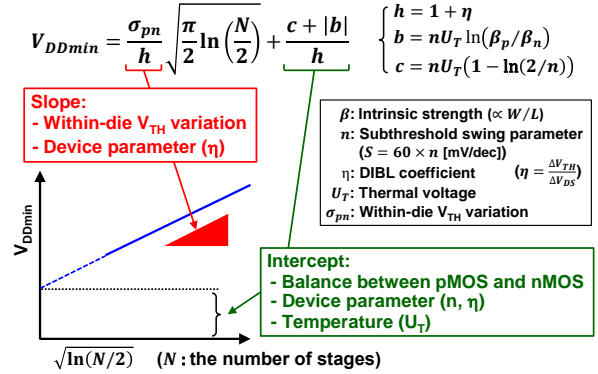


Fig. 2. Closed-form expression of V_{DDmin} of logic gates when pMOS and nMOS are not perfectly balanced.

minimum operating voltage (V_{DDmin}) is defined as the supply voltage where the first functional error occurs. If V_{DDmin} is higher than V_{opt} , the minimum-energy operation cannot be attained. Therefore, investigations on V_{DDmin} are essential for subthreshold circuits.

Fig. 2 shows a closed-form expression for estimating V_{DDmin} of logic gates [3]. V_{DDmin} can be expressed as a linear function of square-root of logarithm of the number of logic gates. This means that V_{DDmin} rises as the number of logic gates increases. Fig. 3 illustrates V_{DDmin} 's of an inverter chain with various configurations of the within-die V_{TH} variation obtained by Monte Carlo SPICE simulations and the closed-form expression in a

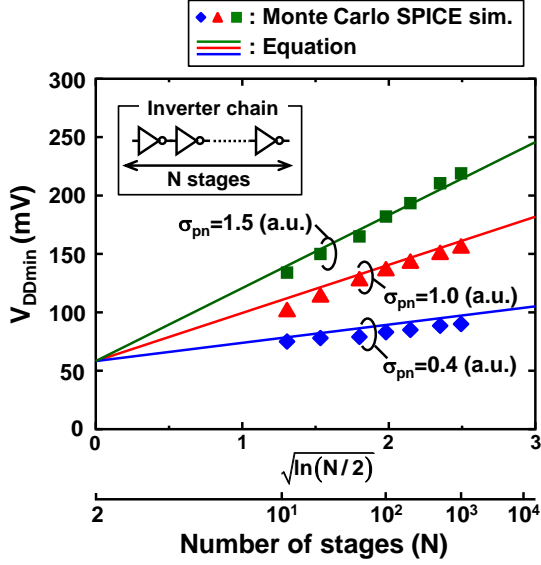


Fig. 3. Simulated V_{DDmin} 's of inverter chain in 65nm process. σ_{pn} 's are normalized by nominal value of this process.

65nm CMOS process. V_{DDmin} 's obtained by the expression agree with the simulated results.

The slope of the expression of V_{DDmin} (Fig. 2) is proportional to the standard deviation of the within-die variation in the V_{TH} difference between pMOS and nMOS transistors (σ_{pn}). In contrast, the intercept of the expression depends on the balance between intrinsic strengths of pMOS and nMOS transistors (β). This indicates that the slope depends on the within-die V_{TH} variation, while the intercept depends on the die-to-die V_{TH} variation. Although body-biasing can compensate the die-to-die variation, that is, can reduce the intercept, it has no effects on reducing the slope. Therefore, the V_{DDmin} increase due to the within-die V_{TH} variation could be a critical problem in large-scale circuits.

Fig. 4 shows simulated V_{DDmin} 's of the inverter and NAND chains. V_{DDmin} 's of logic gates, which contain the larger number of stacked/paralleled transistors, are much higher. This is because stacking and paralleling transistors contained in the NAND gate worsen the balance of the strength of pMOS and nMOS, which corresponds to the increase in parameter $|\beta|$ in the closed-form expression (Fig. 2). Although V_{DDmin} can be reduced by adjusting the balance between the strength of pMOS and nMOS, it is usually impractical, since the gate sizes of either pMOS or nMOS transistors must be significantly enlarged for the adjustment, and hence it is not acceptable due to the area constraint [4]. Therefore, the logic gates with a lot of inputs should not be used in the design of subthreshold logic circuits.

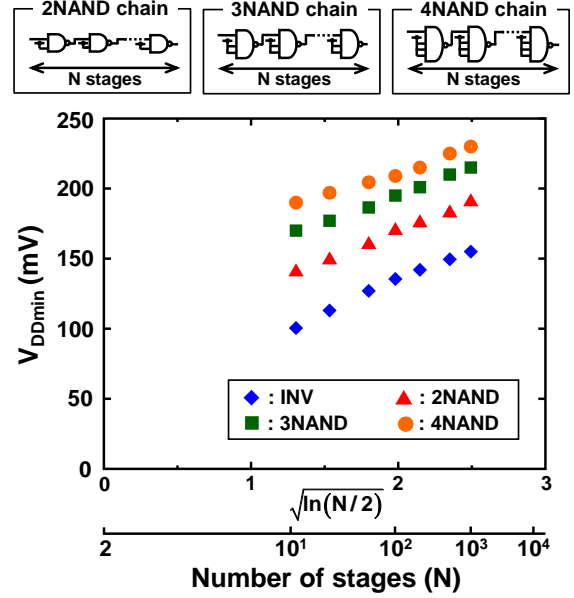


Fig. 4. Simulated V_{DDmin} 's of inverter and 2-, 3-, 4-input NAND chains in 65nm process.

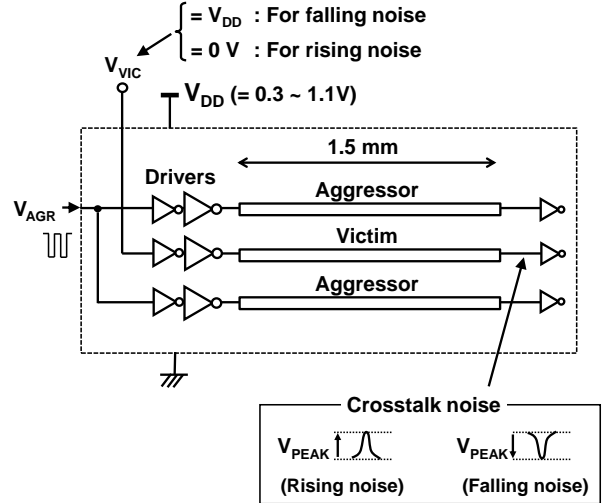


Fig. 5. Crosstalk-noise on 1.5-mm coupled wire lines discussed in this paper.

3. Increase of crosstalk noise due to V_{TH} imbalance

In subthreshold circuits, the dependence of crosstalk noise on manufacturing variability should be also taken into account. In this paper, crosstalk noise on a 1.5-mm coupled wire line shown in Fig. 5 is investigated. The approximation model of crosstalk noise in the subthreshold region has been proposed in [5, 6]. The peak voltage of crosstalk noise (V_{PEAK}) in Fig. 5 in the

subthreshold region is approximated as

$$V_{PEAK,approx} = V_{DD} \left(\frac{r}{r+0.5} \cdot \frac{c}{c+0.5} \right)^{1.3}, \quad (1)$$

where $c=C_C/C_W$ (C_W and C_C are the wire capacitance and the coupling capacitance, respectively.) and r is the equivalent resistance ratio. r is expressed as

$$r \propto e^{\frac{V_{TH,N}-|V_{TH,P}|}{nU_T}}, \quad (2)$$

for rising noise, and

$$r \propto e^{\frac{|V_{TH,P}|-V_{TH,N}}{nU_T}}, \quad (3)$$

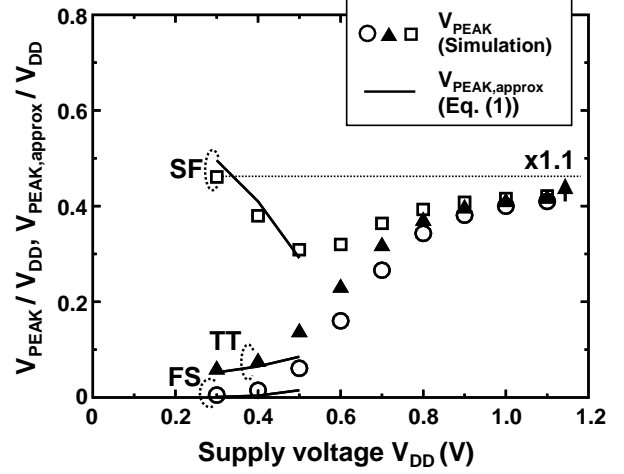
for falling noise, where $V_{TH,P}$ and $V_{TH,N}$ are V_{TH} 's of pMOS and nMOS, respectively. These equations indicate that the peak noise voltage is sensitive to the V_{TH} balance between pMOS and nMOS. Here, we focus on the V_{TH} imbalance induced by the die-to-die V_{TH} variation, since within-die V_{TH} variation can be reduced by employing wider MOSFET's.

Fig. 6 shows the simulated peak noise voltage under a typical process condition (TT) and the corner conditions (slow-nMOS/fast-pMOS (SF) and fast-nMOS/slow-pMOS (FS)) for the rising noise and falling noise, respectively. V_{PEAK}/V_{DD} at 0.3V is 1.1 times larger than V_{PEAK}/V_{DD} at 1.1V for the rising noise under the SF corner condition and 1.4 times larger for the falling noise under the FS corner condition. The approximated peak noise ($V_{PEAK,approx}$) calculated using (1) is also shown, and it agrees with the simulation results. Fig. 6 indicates that peak noise voltage in the subthreshold region is significantly sensitive to the V_{TH} balance, since peak noise voltage depends on the equivalent resistance ratio (r), which has an exponential dependence on the V_{TH} difference between nMOS and pMOS, as indicated in (2) and (3). Therefore, designers must consider the process corners, such as the SF and FS corner conditions, as the worst-case conditions for signal integrity in subthreshold circuits.

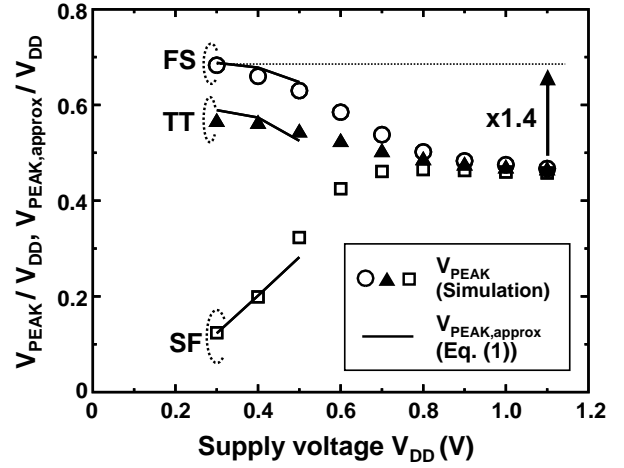
In [5, 6], the peak voltage of crosstalk noise is measured in a 40nm CMOS process, and the measurement results agrees with the simulation results.

4. Gate delay variation in subthreshold region

In the subthreshold region, the gate delay is significantly



(a) Rising noise



(b) Falling noise

Fig. 6. Peak voltage of crosstalk noise on 1.5- μ m coupled wire line with two aggressors and one victim at TT, FS, and SF process corners in 40nm CMOS process.

sensitive to V_{TH} , because the subthreshold current has an exponential dependence on V_{TH} . Therefore, the gate delay is fluctuated by environmental variability such as temperature. Fig. 7 shows the measured dependence of the average gate delay ($=\mu$) on temperature of NAND and NOR gates with different V_{DD} [7]. As temperature is reduced from 80°C to -40°C, the average gate delay slightly decreases at $V_{DD}=1.1V$, whereas it increases at $V_{DD}=0.3V$ by a factor of more than 10. The worst-case ($=$ largest) μ is observed at -40°C.

In addition, the gate delay variation ($=\sigma/\mu$) also depends on temperature. Fig. 8 shows the measured dependence of σ/μ on temperature [7]. The worst-case ($=$ largest) σ/μ is also observed at -40°C. In the NAND gate at

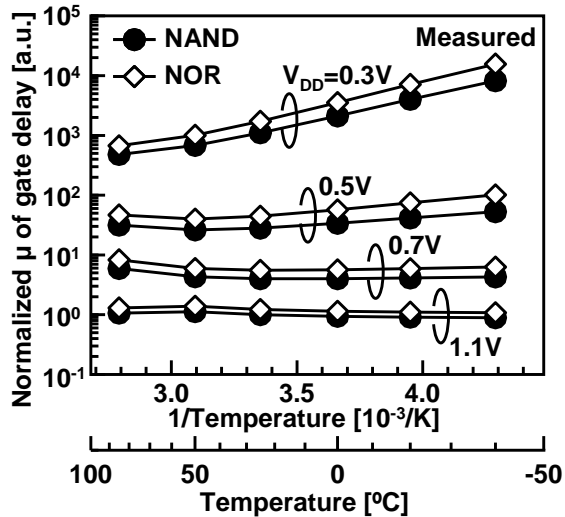


Fig. 7. Measured dependence of average gated delay (μ) on temperature in 40nm CMOS process.

$V_{DD}=0.3V$, σ/μ at $-40^{\circ}C$ is 1.8 times larger than that at $85^{\circ}C$. This indicates that the temperature dependence of σ/μ as well as μ must be taken into account for subthreshold logic circuits.

As shown in Figs 7 and 8, the gate delay variation in the subthreshold region is much larger than that in the nominal supply voltage region. This indicates that large timing margins are required in the worst case design. Since such large timing margins spoil energy-efficient operation achieved by the reduction of V_{DD} , an adaptive performance control, such as dynamic V_{DD} control and/or body-bias control, is indispensable for subthreshold circuits.

In order to attain the adaptive performance control, a performance monitor is required, and conventionally, replica circuits have been used for monitoring [8]. However, the critical path replica is inadequate for subthreshold circuits, because the delay mismatch between the replica and the actual critical path is remarkably large due to the within-die variation. In order to overcome this mismatch, in-situ techniques, such as Canary FF [9] and PEPD [10], which can predict the occurrence of timing errors, have been proposed. These techniques reduce the large timing margins, and consequently the energy-efficient operation can be achieved.

5. Conclusion

In this paper, design challenges in subthreshold logic circuits were discussed. Subthreshold circuits are

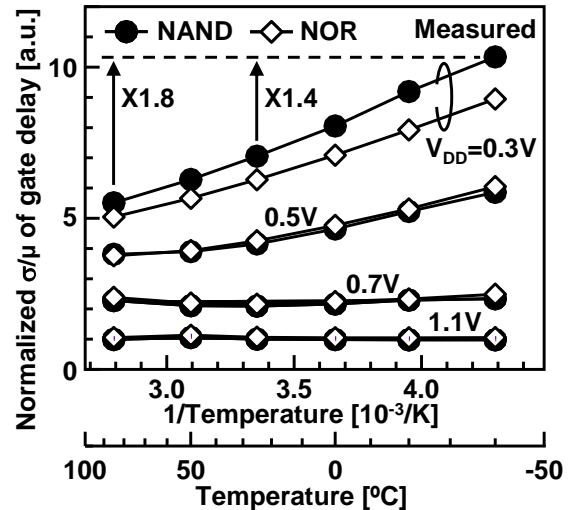


Fig. 8. Measured dependence of gated delay variation (σ/μ) on temperature in 40nm CMOS process.

sensitive to manufacturing and environmental variability. Due to V_{TH} variation, V_{DDmin} increases and signal integrity is degraded in subthreshold region. In addition, the gate delay is fluctuated by environmental variability such as temperature, which requires the large timing margins. Therefore, the adaptive performance control, which can reduce the timing margins, is effective for subthreshold logic circuits.

Acknowledgments

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