93% Power Reduction by Automatic Self Power Gating (ASPG) and Multistage Inverter for Negative Resistance (MINR) in 0.7V, 9.2μW, 39MHz Crystal Oscillator

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Abstract

In order to reduce the power consumption of a crystal oscillator (XO), an automatic self power gating (ASPG) and a multistage inverter for a negative resistance (MINR) are proposed. By combining ASPG and MINR, the measured power of a 39-MHz XO in 40-nm CMOS decreases by 93% from 139μW to 9.2μW, which is the lowest power in the published XO's at 0.7V.

Introduction

Fig. 1 shows a target application of a proposed crystal oscillator (XO). XO must be always powered ON not only in an active mode but also in a stand-by mode. The power reduction of XO is important, because XO dominates the power in the stand-by mode. In the active mode, a low phase noise of XO is required for RF blocks, while the low phase noise is not required in the stand-by mode, because the RF blocks are powered OFF. Therefore, in this paper, a new low power mode of XO with an automatic self power gating (ASPG) is proposed. A multistage inverter for a negative resistance (MINR) is also proposed to reduce the power.

Multistage Inverter for Negative Resistance (MINR)

Figs. 2 (a) and (b) show schematics of a conventional Pierce XO and a proposed XO with MINR. Comparing Figs. 2 (a) and (b), a one-stage CMOS inverter for the negative resistance necessary for the oscillation of XO is replaced with three-stage CMOS inverters in Fig. 2 (b). In the conventional Pierce XO, short-circuit current in a CMOS inverter is large, because the input signal is a sinusoidal wave as shown in Fig. 2 (a), thereby increasing the power consumption of XO. In order to reduce the short-circuit current, MINR is proposed. Fig. 3 shows simulated waveforms of XO with MINR. The waveforms at X2 and X3 are rectangular waves, thereby reducing the short-circuit current of Inv2 and Inv3. The power consumption of Inv1 is much lower than that in Fig. 2 (a), because the gate width of Inv1 is one-tenth of that in Fig. 2 (a).

Automatic Self Power Gating (ASPG)

XO can keep the oscillation for a while without the negative resistance, because the quartz crystal has a very high Q (> 10000). In order to investigate the duration of the oscillation without the negative resistance, Fig. 4 shows measured waveforms of Gating and X1 shown in Fig. 2 (c). Gating is controlled from an off-chip pulse generator to switch SW1, SW2, and SW3. The damping time is 2.5ms, which corresponds to 100k cycles of 39-MHz clock. By use of the long damping time of XO, ASPG is proposed to reduce the power of XO. Fig. 2 (c) shows a schematic of a proposed XO with MINR and ASPG. Comparing Figs. 2 (b) and (c), three switches (SW1, SW2, and SW3) and a switch controller are added in Fig. 2 (c). In ASPG, the negative resistance is intermittently powered OFF to save the power. After XO is powered OFF, the amplitude of X1 attenuates as shown in Fig. 4. When the amplitude is less than a preset level, the switch controller turns on the three switches. Fig. 5 shows a schematic of the switch controller. In order to detect the amplitude, in stead of a conventional continuous time comparator which consumes a lot of power, two inverter chains with different threshold voltages are used to save the power. The simulated power consumption of the switch controller is 1.3μW. Fig. 6 shows a timing chart of the switch controller. When the amplitude of Out is less than a preset level (V_{REF}), X_{HVT} goes to low and Gating goes to high. As a result, XO is powered ON. Thus, the amplitude of Out is kept higher than V_{REF}.

Experimental Results

The proposed XO with MINR and ASPG is fabricated in 40-nm CMOS process. Fig. 7 shows a die photo and layout. Table I shows a performance summary. Fig. 8 shows a measured power supply voltage (V_{DD}) dependence of the power consumption. The conventional Pierce XO [1], XO with MINR, and XO with MINR and ASPG are compared. The minimum power of XO with MINR and ASPG is 9.2μW at V_{DD} = 0.7V, because the negative resistance is maximum at 0.7V. At V_{DD} = 0.7V, MINR reduces the power by 50%. ASPG reduces the power by 87%, because the power ON duty is 6.7%. Thus, MINR and ASPG reduce the power by 92% from 139μW to 9.2μW.

Fig. 9 shows measured waveforms of Gating and Out in XO with MINR and ASPG at 0.7V. The amplitude of Out is kept to 0.2V by ASPG. The waveform of Out looks similar between power OFF and power ON. The startup times with and without ASPG are compared. Figs. 10 (a) and (b) show measured startup waveforms of Gating and X1 in XO with and without ASPG, respectively. ASPG reduce the startup time by 20% from 259μs to 208μs. Fig. 11 shows a measured amplitude dependence of the power consumption and the startup time in XO with MINR and ASPG at 0.7V. With decreasing the amplitude, the power consumption is decreased and the startup time is increased. Therefore, the power consumption and the startup time are the trade-off in ASPG. Fig. 12 shows a measured V_{DD} dependence of the frequency accuracy with and without ASPG. The frequency accuracy across V_{DD} from 0.6V to 0.9V is -4 to +4 ppm without ASPG and -29 to +7 ppm with ASPG. The degradation of the frequency accuracy due to ASPG is acceptable.

Fig. 13 shows measured phase noise of XO with and without ASPG at 0.7V. By introducing ASPG, the phase noise at 1-MHz frequency offset degrades by 38dB. The phase noise with ASPG at 1-MHz frequency offset is -112dBc/Hz. The phase noise is not acceptable for RF circuits, while it is acceptable for logic circuits.

Table II shows a comparison with previously reported crystal oscillators [1-4]. 9.2μW in this work is the lowest power at 0.7V in the published XO's. Though 4.1μW is reported in [1], the startup time dramatically increases as V_{DD} is reduced as modeled in [2]. In order to reduce the power, an analog-based amplitude control is shown in [4], which fails to work below 1V. Therefore, the digital-based amplitude control shown in this paper is important to reduce the power of sub-1V XO's.

Conclusions

A new low power mode of XO enabled by ASPG is proposed and demonstrated for the first time. ASPG reduce the power and the startup time by 87% and 20%, respectively, at the cost of 38-dB phase noise degradation.

Acknowledgment

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References

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[3] D. Aebischer et al., ISSCC, pp. 999-1005, 1997.
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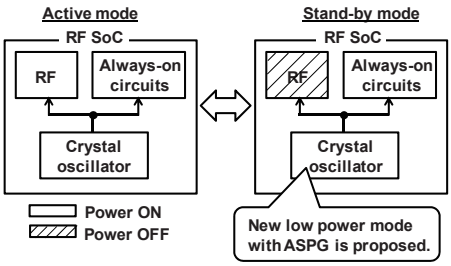

Fig. 1. Target application of proposed crystal oscillator (XO).

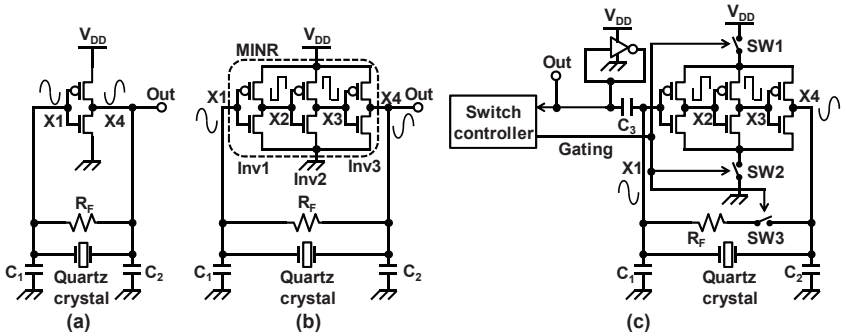

Fig. 2. (a) Conventional Pierce XO. (b) Proposed XO with MINR. (c) Proposed XO with MINR and ASPG.

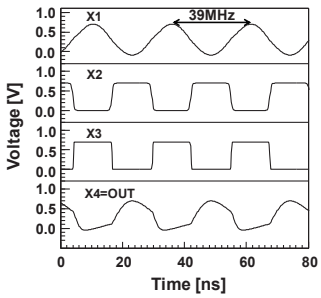

Fig. 3. Simulated waveforms of XO with MINR.

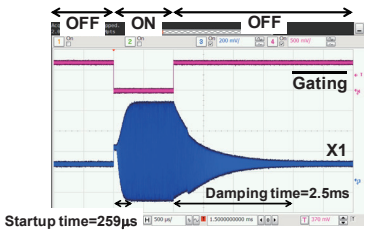

Fig. 4. Measured waveforms of Gating and X1 in Fig. 2 (c).

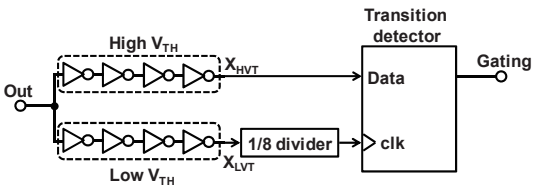

Fig. 5. Schematic of switch controller.

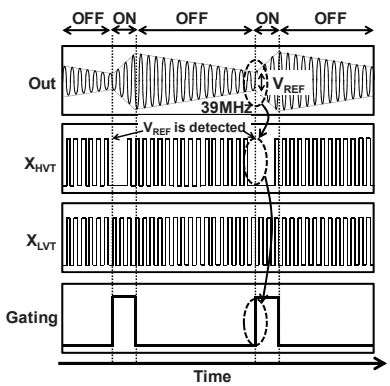

Fig. 6. Timing chart of switch controller.

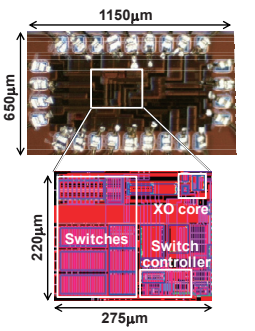

Fig. 7. Die photo and layout.

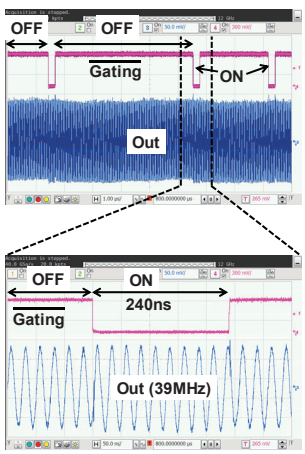

Fig. 9. Measured waveforms of Gating and Out in XO with MINR and ASPG.

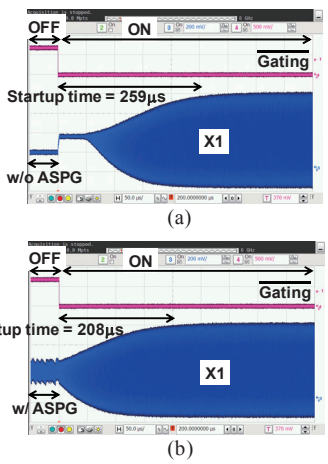

Fig. 10. Measured startup waveforms of Gating and X1. (a) Without ASPG. (b) With ASPG.

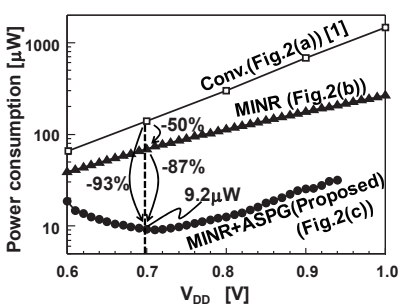

Fig. 8. Measured V_{DD} dependence of power consumption in three XO's.

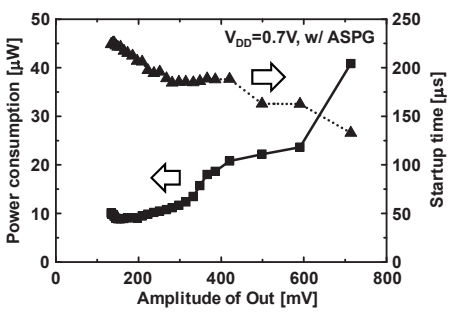

Fig. 11. Measured amplitude dependence of power consumption and startup time.

Table I Performance summary.

	MINR	MINR+ASPG
CMOS technology	40nm	←
Frequency (f)	39MHz	←
Supply voltage (V_{DD})	0.7V	←
Power	69µW	9.2µW
Startup time	259µs	208µs
Phase noise at 1MHz offset	-150dBc/Hz	-112dBc/Hz
Core area	60,500µm^2	←
f accuracy at V_{DD}=0.6-0.9V	-4 / +4ppm	-29 / +7ppm

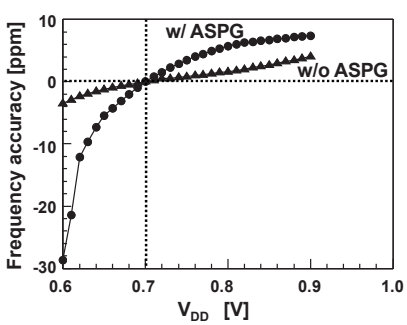

Fig. 12. Measured V_{DD} dependence of frequency accuracy with and without ASPG.

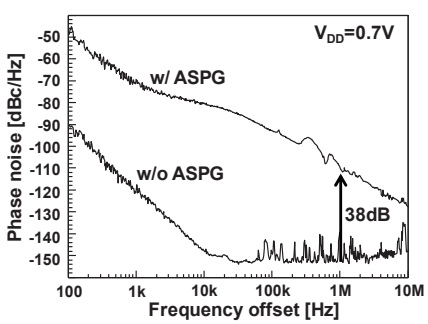

Fig. 13. Measured phase noise of XO with and without ASPG at 0.7V.

Table II Comparison with published crystal oscillators.

Ref.		[2]	[3]	[4]	[1]		This work
Frequency	MHz	2.1	2.1	19	39	←	←
CMOS process	µm	3.0	2.0	0.1	0.04	←	←
V_{DD}	V	1.5	1.8	1.2	0.35	0.7	←
Power	µW	1.4	0.7	21.6	4.1	139	9.2