0.5V Image Processor with 563 GOPS/W SIMD and 32bit CPU Using High Voltage Clock Distribution (HVCD) and Adaptive Frequency Scaling (AFS) with 40nm CMOS

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Abstract

A 0.5V, 10MHz, 9mW image processor with 320 processing element (PE) SIMD and a 32bit CPU has been developed using 40-nm CMOS. High voltage clock distribution (HVCD) reduces the number of excessive hold buffers required in a 0.5-V logic circuit design, thereby reducing the area, delay, and energy of the SIMD by 14 %, 13%, and 6%, respectively. The 0.5-V SIMD with HVCD achieves an energy efficiency of 563 GOPS/W (= 4.26mW at 7.5MHz), the highest yet reported for near-threshold SIMD. In addition, adaptive frequency scaling (AFS), used to mitigate the impact of the ripple of a buck converters, increases average clock frequency by 33%.

Introduction

We have developed an energy efficient programmable 0.5-V image processor for front-end signal processing of imagers. In order to increase energy efficiency, heterogeneous multi-cores with SIMD, 320 parallel processing in SIMD, and near-threshold operations are used. In the design of near-threshold logic circuits, large delay variations due to PVT variations are a critical problem. We propose two techniques for dealing with this: high voltage clock distribution (HVCD) at design stage and adaptive frequency scaling (AFS) for a post-fabrication tuning.

Image Processor with SIMD and CPU

Fig. 1 shows a block diagram of a developed image processor that includes a 32bit CPU, a 320 PE SIMD, buck converters, an all digital PLL (ADPLL) [1], and an A/D converter (ADC) [2]. The clock frequency (f_{CLK}) is 10MHz. The image processor has four power supply voltages (V_{DD}), including V_{DD} for logic circuits other than those for clock distributions (V_{LOGIC}), V_{DD} for clock distributions in the logic circuits (V_{CLK}), V_{DD} for a 1-port SRAM [3] (V_{SRAM1}), and V_{DD} for a 2-port SRAM (V_{SRAM2}). The four V_{DD}'s are supplied by on-chip buck converters.

High Voltage Clock Distribution (HVCD)

Fig. 2 (a) shows a hold timing design in a logic circuit. In order to achieve correct hold timing with regard to early and late on-chip variation (OCV) conditions, hold buffers, buffers added to prevent hold time violations, are required. Fig. 2 (b) shows simulated V_{LOGIC} dependence of the normalized minimum number (N) of stages of the logic gates that include hold buffers. V_{CLK} is varied. N increases with decreasing V_{LOGIC} because OCV increases and within-die gate delay variations increase. N also increases with decreasing V_{CLK} because OCV increases and clock skew increases. For example, at V_{LOGIC} = 0.5V, N at $V_{CLK} = V_{LOGIC}$ - 0.1V is seven times as large as N at $V_{CLK} = V_{LOGIC}$. Increasing N increases area and power overhead, and the setup timing design will also be affected by an increased N. In contrast, N at $V_{CLK} = V_{LOGIC}$ + 0.1V is one-fifth of N at $V_{CLK} = V_{LOGIC}$. For this reason, we propose HVCD in which V_{CLK} and V_{LOGIC} are separated and $V_{CLK} > V_{LOGIC}$, in order to reduce excessive N due to large within-die process variations at 0.5V. Fig. 3 shows a layout for 320 PE SIMD with HVCD. In each 16 PE, the V_{CLK} domain and V_{LOGIC} domains are separated, and all clock buffers are placed and routed in the V_{CLK} domain. Figs. 4 (a) and (b) show simulated area, delay, power, and energy for HVCD with respect to conventional $V_{CLK} = V_{LOGIC}$ for CPU and the SIMD, respectively,. In CPU, area, delay, and energy are reduced by 11%, 13%, and 6%, respectively, at the cost of an 8% increase in power. Similarly, in the SIMD, area, delay, and energy are reduced by 14%, 13%, and 6%, respectively.

Adaptive Frequency Scaling (AFS)

In conventional AFS [4] for a high performance 2.5 GHz processor, f_{CLK} is varied with ns-resolution, using voltage detectors and digital frequency dividers. The area and the power overheads of the conventional AFS are not acceptable in the mW-class processor in the this work. Therefore, we propose AFS with a small area and power overheads (see Fig. 5). Adaptive voltage scaling (AVS) [5] is also implemented. AFS is performed by a μs-order and ns-order feedback loops, while AVS is performed by a ms-order feedback loop. Ring oscillators (ROSC's) monitor V_{LOGIC} and also function as integrators for V_{LOGIC}, which solves the area and power overhead problem in [4]. ROSC frequency is compared with a reference frequency (f_{REF}), and an up/down signal is given to the AVS controller every several 10ms to adapt to die-to-die process variations and temperature variations. An up/down signal is also given to the AFS controller every about 10μs to adapt to several 100 μs-order V_{LOGIC} noise, and f_{CLK} is changed by changing a multiplication number in the ADPLL. Critical path replicas also monitor V_{LOGIC} every 100ns (cycle-by-cycle at 10MHz) by checking the setup margin. When a setup warning is found, the critical-path-replica interrupts the up/down signal to avoid a setup error.

Experimental Results

The proposed image processor has been fabricated in a 40-nm CMOS process. Fig. 6 shows a die photo. Table I shows a performance summary. Fig. 7 shows measured shmoo results for two CPUs, (CPU0 and CPU1), which were designed and fabricated to show the advantage of HVCD. CPU0 is designed with HVCD ($V_{CLK} = V_{LOGIC}$ + 0.1V), while CPU1 is designed with a conventional single V_{DD} ($V_{LOGIC} = V_{CLK}$). In Fig. 7, the target 10MHz operation is achieved at 0.5V only with CPU0, which is faster than CPU1 at a fixed V_{LOGIC}. Fig. 8 shows a measured shmoo for SIMD with HVCD. The target 10MHz operation is achieved at 0.5V. Fig. 9 shows measured V_{LOGIC} dependence of maximum f_{CLK}, total power, and leakage power for SIMD. Fig. 10 shows measured V_{LOGIC} dependence of energy efficiency for SIMD. The maximum 563GOPS/W is obtained at V_{LOGIC} = 0.45V, 4.26mW, and 7.5MHz. Table II shows a comparison with a previously reported SIMD [6]. Our design achieves the highest energy efficiency in the reported near-threshold SIMD. Fig. 11 shows measured waveforms of V_{LOGIC} and f_{CLK} with AFS. A 4kHz sinusoidal wave is applied to V_{LOGIC} to emulate the ripple of buck converters. The proposed AFS makes it possible to track f_{CLK} to V_{LOGIC}, thereby increasing average clock frequency by 33%.

Acknowledgment

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References

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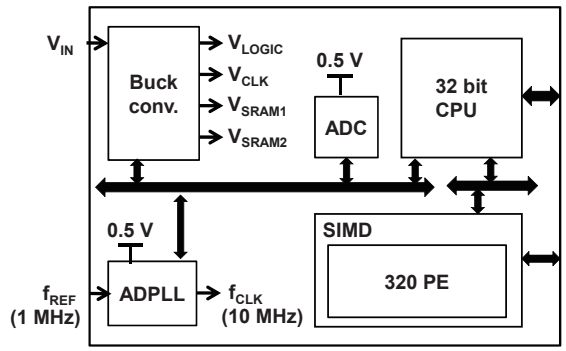

Fig. 1. Block diagram of image processor.

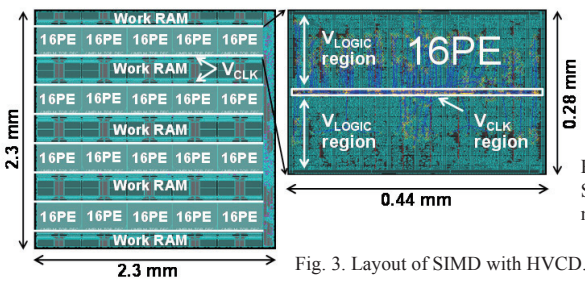

Fig. 3. Layout of SIMD with HVCD.

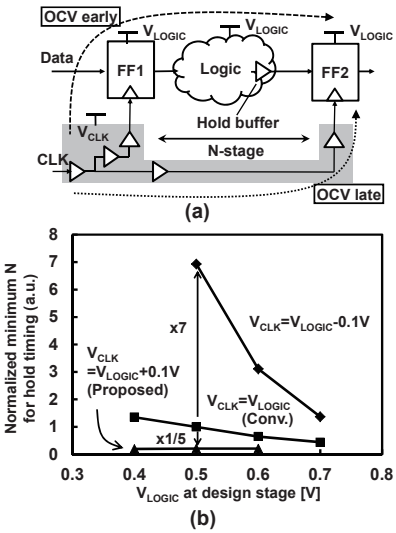

Fig. 2. (a) hold timing design in logic circuit. (b) Simulated V_{LOGIC} dependence of normalized minimum number (N) of stages of the logic gates.

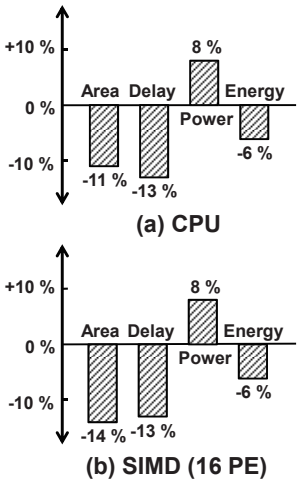

Fig. 4. Effect of HVCD.

Table I Performance summary

Technology	40 nm CMOS		
Die size	5 mm x 5 mm		
Number of Transistors	31 M (Logic: 16 M, SRAM: 15 M)		
Logic cores	CPU	32 bit	
	SIMD	4 bit, 320 PE	
SRAM	CPU	Inst.	1 Mbit
		Data	256 kbit
	SIMD	Inst.	512 kbit
		Image	128 kbit x 4
		Work	64 Byte x 320 (2port)
Frequency	10 MHz		
Supply voltages	V_{LOGIC}	0.5 V	
	V_{CLK}	0.6 V	
	V_{SRAM1}	0.8 V (1 port)	
	V_{SRAM2}	0.6 V (2 port)	
Power	9 mW		
SIMD performance	559 GOPS/W (5.73 mW@10 MHz) Max. 563 GOPS/W (4.26 mW@7.5 MHz)		

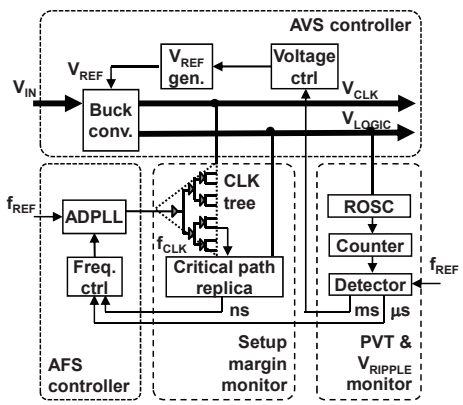

Fig. 5. Block diagram of proposed adaptive voltage and frequency scaling.

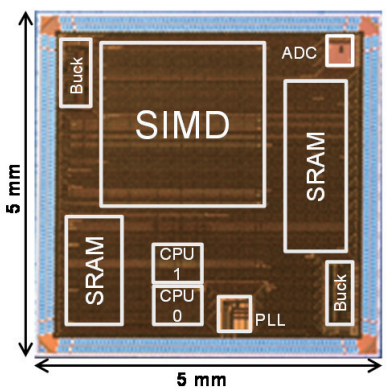

Fig. 6. Die photo.

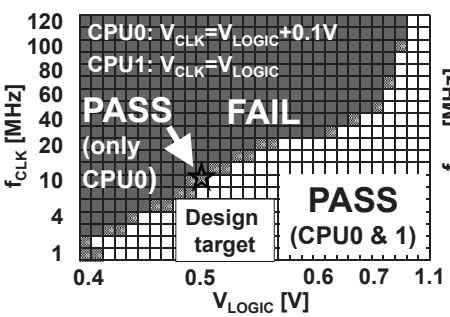

Fig. 7. Measured shmoo for CPU.

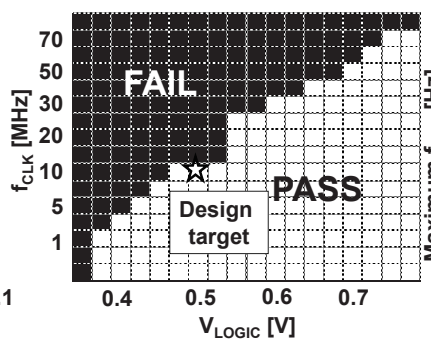

Fig. 8. Measured shmoo for SIMD.

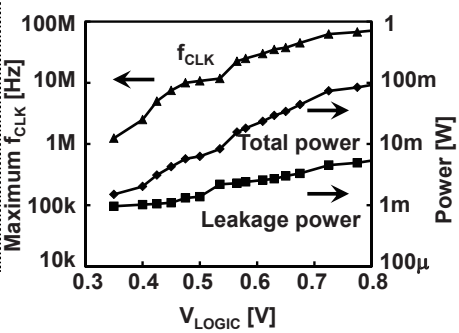

Fig. 9. Measured SIMD frequency and power consumption characteristics.

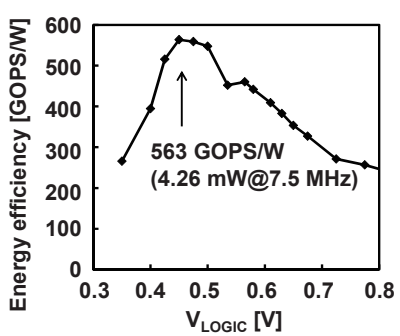

Fig. 10. Measured SIMD energy efficiency.

Table II Comparison with previous SIMD.

	Ref. [6]	This work
SIMD	16 bit	4 bit
CMOS technology	45 nm SOI	40 nm bulk
Supply voltage	0.53 V	V_{LOGIC}=0.45 V V_{CLK}=0.565 V
Frequency	144 MHz	7.5 MHz
Power	19.3 mW	4.26 mW
GOPS/W	59.6	x 9.4
GOPS/W normalized to 4 bit	239	563 x 2.4

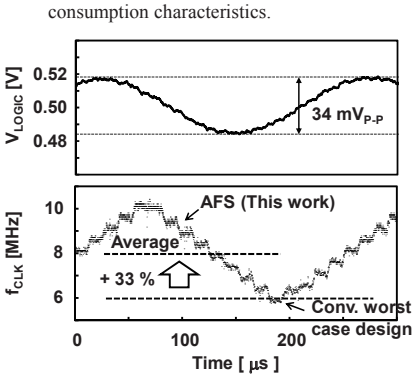

Fig. 11. Measured waveforms of V_{LOGIC} and f_{CLK} with AFS.