A 0.6-V Input 94% Peak Efficiency CCM/DCM Digital Buck Converter in 40-nm CMOS with Dual-Mode-Body-Biased Zero-Crossing Detector

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***Abstract*—A 0.6-V input, 0.3-0.55V output buck converter is developed in 40-nm CMOS, for low-voltage low-power wireless sensor network systems. The buck converter is able to automatically select DCM or CCM operation, therefore improving the power efficiency and enlarging the output current range, by virtue of the proposed low-power CCM/DCM controller. A dual-mode-body-biased (DMBB) (forward body bias & zero body bias) low-voltage zero-crossing detector is designed to enable DCM operation with both low supply voltage and normal supply voltage. The proposed buck converter achieves a peak efficiency of 94% with an output current range of 50μA to 10mA. Thanks to the DCM operation, the efficiency at an output current of 100μA is improved by 20% and 9%, with an output voltage of 0.35V and 0.5V, respectively.**

I. Introduction

With the widely use of near/sub-threshold digital circuits in low-power systems like wireless sensor nodes and bio-medical applications [1-2], there is a strong demand of voltage converters which can regulate the power supply voltage at from 0.3V to 0.55V, with the output current of from 50μA to 10mA. On the other hand, such low-power systems often prefer a self-powered energy source, i.e., solar cells, than a battery, to avoid the trouble of frequent battery replacing. For a typical single solar cell, the max power point is around 0.6V as its output voltage. Therefore, a low-voltage high efficiency step-down voltage converter which generates a 0.3V to 0.55V output voltage (V_{OUT}) from a 0.6V input voltage (V_{IN}) is of great importance to such low-power systems.

Low-dropout regulators (LDOs) are commonly used as a step-down voltage converter. However, due to the fact that the efficiency of LDO is limited by the ratio of V_{OUT} over V_{IN}, there is considerable loss when adaptive power supply voltage (V_{DD}) control is applied to the digital load [2-3].

The buck converter can have two modes of operation: continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In CCM, the inductor current is always positive, while in DCM, the inductor current is sometimes down to zero. This characteristic makes DCM a more suitable mode of operation for a light load situation. CCM operation at light load situation is undesirable, because the reverse inductor current introduces additional losses. Therefore, a buck converter with CCM for the heavy load situation and DCM for the light load situation is strongly required to achieve the high power efficiency across a wide output current range.

Conventional buck converter either requires an external control signal to switch between CCM and DCM [4], or uses a complex synchronous logic circuit to realize CCM/DCM selection [5]. The drawback of [4] is obvious that it relies on external signal to switch modes. The drawback of [5] is that the complex logic circuit would increase the total gate number and therefore increase the power consumption. So it is not suitable for the light load situation. Moreover, in the low-voltage synchronous logic circuit design, setup and hold errors should be carefully avoided [6].

Ref. [7] is a low-voltage buck converter, but it has fixed V_{IN} due to delay chain based pulse width modulation (PWM), and it uses a large inductor (47mH) to accommodate low inductor current, because it has only CCM operation. In this paper, a low-voltage buck converter is presented with a new automatic CCM/DCM controller. The CCM/DCM controller composes of a simple combination logic circuit, thus it is power efficient and suitable for low-voltage design. A dual-mode-body-biased (DMBB) zero-crossing detector is also proposed to enable low-voltage DCM operation.

This paper is organized as follows. The top-level architecture and the operation sequences of the proposed buck converter are described in Section II. Section III shows the detailed circuit implementation of key building blocks. The experimental results are shown in Section IV, followed by the conclusion in Section V.

II. System Architecture

The top-level block diagram of the proposed buck converter is shown in Fig. 1. The proposed buck converter consists of a clock generator, a CCM/DCM controller, a

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power stage, and a digital PWM controller. The system clock (CK1) frequency is 6.4MHz. A clock generator is employed to generate different frequency for sub-blocks in the digital PWM controller based on the main clock. CK1 of 6.4MHz is used by DFFs. CK2 of 100kHz is used by the clocked comparator. CK3 is used by the bi-directional shift register (SR). The CCM/DCM controller is employed to automatically generate the required gate signals (CKP and CKN) for M_P and M_N either in CCM or DCM operation. It will be explained in detail in section III. The power stage consists of gate drive buffers, power MOS (M_P and M_N), and a LC filter.

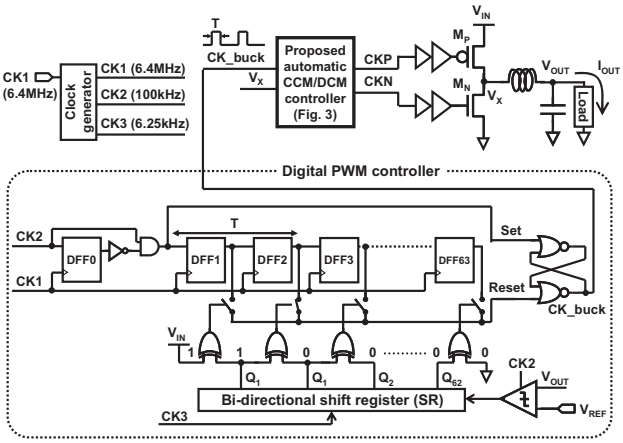

Fig. 1. Top level diagram of proposed buck converter.

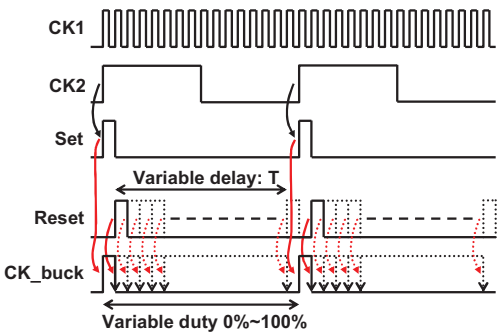

Fig. 2. Timing diagram of digital PWM controller.

In order to fit with the low supply voltage (0.6V), a digital feedback architecture is more attractive than an analog feedback. The digital PWM controller plays an important role in the buck converter, and the timing diagram is shown in Fig. 2. Set signal is generated from CK1 and CK2 by DFF0 and two logic gates. A comparator is used to compare V_{OUT} with V_{REF}, thereafter control the shifting direction of the bi-directional shift register (SR). The output of SR, i.e., $Q_{1\text{-}62}$, then enables one of the switches to select one of the DFFs' outputs to connect to Reset. Therefore, a variable delay "T" is obtained to generate variable duty cycle for CK_buck. CK_buck carrying appropriate duty information is later used to drive the power stage and to regulate V_{OUT} towards V_{REF}.

III. Key Building Blocks

The circuit diagram of proposed automatic CCM/DCM controller is shown in Fig. 3. In DCM, a zero-cross switching is achieved to maximize the efficiency. The controller consists of only digital standard cells and a proposed dual-mode-body-biased (DMBB) zero-crossing detector. The zero-crossing detector is used to compare V_X with ground, therefore detect if the voltage at V_X has crossed 0V. The rest digital standard cells generate the required gate driving signals (CKP and CKN), and automatically switch between CCM and DCM operations. A pulse converter is realized with inverters and AND gate, to convert a clock signal IN1 into a pulse signal OUT1. The pulse signals are used to set or reset the inputs of the SR-latch to generate CKN. The timing diagram of the proposed automatic CCM/DCM controller is shown in Fig. 4. In CCM condition (Fig. 4 (a)), when load current is high, inductor current (I_L) is always larger than zero. CKP is approximately equal to CK_buck. When CKP goes high, meaning M_P is turned off, a Set1 signal is generated by the pulse converter, and then CKN is set to high, so M_N is turned on accordingly. When M_P is turned off, V_X is always less than 0V due to the conduction voltage drop of M_N, and the output of zero-crossing detector (ZCD) and Reset_DCM is always zero. CKN is then reset to zero by Reset_CCM. In contrast, in DCM condition (Fig. 4 (b)), I_L sometimes drops to zero. CKN is set to high by the similar way as CCM. Then at the zero-crossing point (V_X = 0V when M_P is turned off), a pulse is generated for Reset_DCM and then CKN is reset to zero. In this way, the zero-cross switching (M_N is turned off when I_L becomes zero) is accomplished.

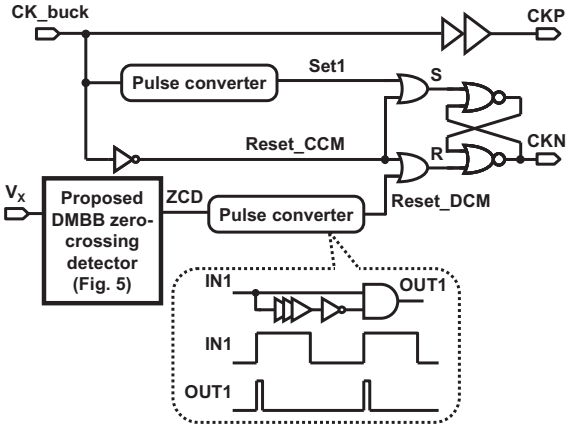

Fig. 3. Circuit diagram of the proposed automatic CCM/DCM controller.

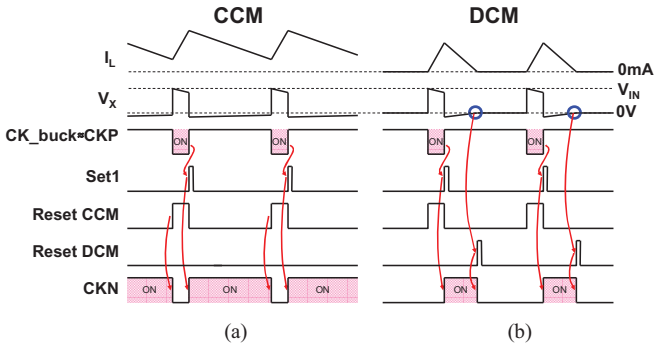

Fig. 4. Timing diagram of the proposed automatic CCM/DCM controller with (a) CCM, (b) DCM operation.

A key building block of the proposed CCM/DCM controller is the zero-crossing detector, which is shown in Fig. 5. A dual-mode-body-biased (DMBB) low-voltage zero-crossing detector is proposed to enable DCM operation with both low supply voltage (0.6V) and normal supply voltage. The DMBB zero-crossing detector is based on a differential amplifier. M_{P1} and M_{P2} serve as the differential input pair, M_{P3} provides bias current for the amplifier, M_{N1} and M_{N2} are the mirroring components. At low V_{DD}, a voltage headroom of the amplifier is quite limited. In order to have enough gm, either transistor size or bias current needs to be enlarged, which are definitely not desired for low-power design. A forward body bias is therefore beneficial in this design to alleviate the lack of voltage headroom with V_{DD}. The bodies of M_{P1-3} are connected to ground to enable the forward body bias, therefore reduce the threshold voltage of them.

However, such forward body bias is only applicable when V_{DD} is low, otherwise the body diode of PMOS would be turned on, and large forward current would flow through the diode. As shown in Fig. 6, I_{VDD} of the zero-crossing detector increases exponentially with V_{DD}. In order to avoid the large leak current from V_{DD}, forward body bias must be turned off when V_{DD} is larger than 0.7V. An ultra low-power voltage detector [8] is therefore employed to switch body connection with regarding to different V_{DD}, as shown in Fig. 5. $V_{Trigger}$ is set to around 0.7V in this design. Thus, when V_{DD} is lower than 0.7V, the DMBB zero-crossing detector is forward body biased. In contrast, when V_{DD} is higher than 0.7V, the detector is zero body biased. Therefore, the DMBB architecture achieves both a fast voltage detection operation at low V_{DD} and small body diode leak current at high V_{DD}.

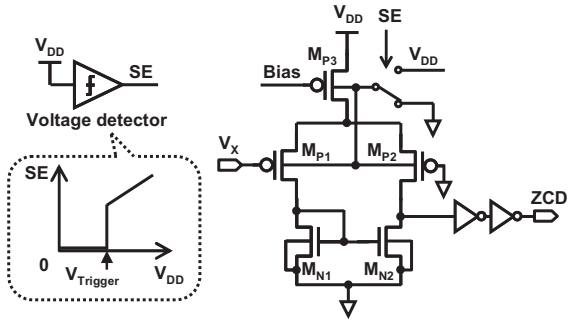

Fig. 5. Low voltage dual-mode-body-biased zero-crossing detector.

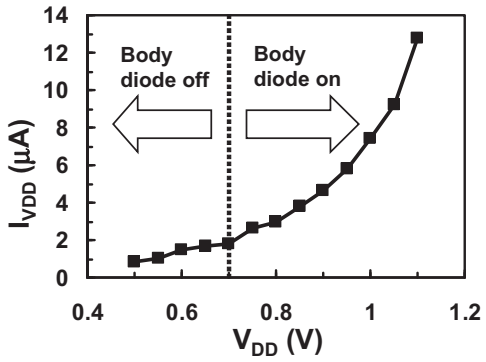

Fig. 6. Measured I_{VDD} of zero-crossing detector when forward body bias is enabled

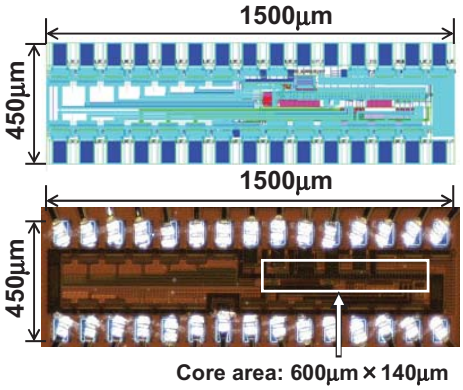

Fig. 7. Layout and die photo.

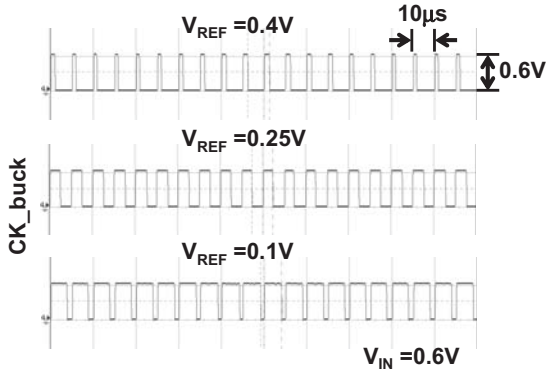

Fig. 8. Measured CK_buck waveforms of digital PWM controller with different V_{REF}.

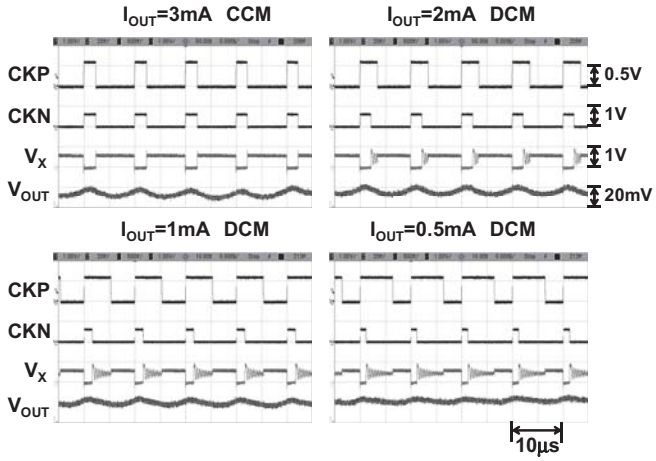

Fig. 9. Measured waveforms of buck converter in CCM and DCM at V_{IN} = 0.6V and V_{OUT} = 0.35V.

IV. Experimental Results

The proposed buck converter is fabricated with 40-nm CMOS process. Fig. 7 shows the layout and the chip micro-photograph. The active area is 0.084mm^2.

Fig. 8 shows the measured output signals of the digital PWM controller, i.e., CK_buck, at different V_{REF}. It is observed that duty cycle of CK_buck changes as V_{REF} changes,

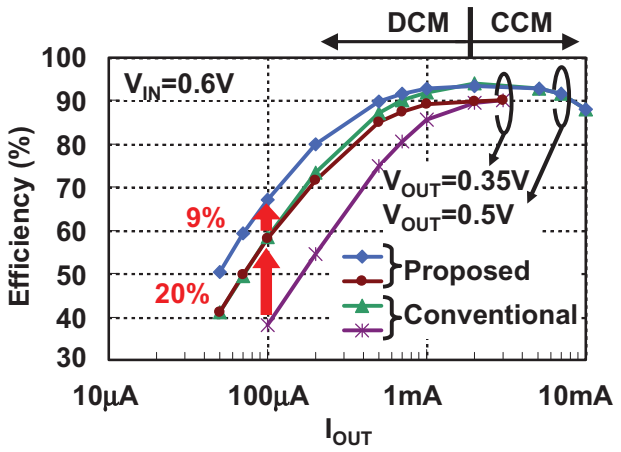

Fig. 10. Measured efficiency of proposed and conventional buck converter.

TABLE I. COMPARISON OF LOW-VOLTAGE BUCK CONVERTERS

	[4] JSSC 2011	[5] VLSI 2010	[6] ISSCC 2007	[7] VLSI 2012	This work
V_{IN} (V)	2.8-4.2	1.8	1.2	0.45	0.6-1.1
V_{OUT} (V)	0.6-1.2	0.575	0.5	0.34-0.44	0.3-0.55
I_{OUT}	20µA-100mA	0.7µA-107µA	2µA-200µA	0.67µA-410µA	50µA-10mA
Peak efficiency	87.4%	90%	86%	97%	94%
L	10µH	-	2µH	47mH	220µH
Switching frequency	2MHz	-	-	20kHz	100kHz
Operating mode	CCM/DCM	CCM/DCM	DCM	CCM	CCM/DCM

meaning successful modulation of the pulse width of the buck converter.

Fig. 9 shows the measured waveforms of the proposed buck converter at V_{IN} = V_{DD} = 0.6V and V_{OUT} = 0.35V with different output current (I_{OUT}). At I_{OUT} of 3mA, the buck converter is in CCM operation, because CKN is in the same shape with CKP. At I_{OUT} from 2mA to 0.5mA, CKN transits to zero before CKP goes to zero, meaning both M_N and M_P are turned off when I_L is zero. The worst case output voltage ripple is 11mV (peak-to-peak) at I_{OUT}=2mA.

Fig. 10 shows the measured power efficiency of proposed buck converter with both CCM and DCM operation, and conventional one with only CCM operation. V_{IN} is set to 0.6V, and V_{OUT} is set to 0.35V and 0.5V. When I_{OUT} is larger than 2mA, both proposed and conventional buck converters are in CCM operation, therefore the same efficiency is achieved. In contrast, when I_{OUT} is less than 2mA, the proposed buck converter is in DCM operation, therefore significant efficiency improvement is achieved. The power efficiency at I_{OUT} of 100µA is improved by 20% and 9%, at V_{OUT} of 0.35V and 0.5V, respectively. The peak efficiency of 94% is achieved by the proposed buck converter at I_{OUT} of 2mA, thanks to the proposed low-power CCM/DCM controller and the low-power digital PWM controller.

Table I shows the comparison with the published low-voltage buck converters [4-7]. Compared with [4-6], the proposed buck converter achieves higher peak efficiency and lower V_{IN} and V_{OUT}. While compared with [7], the proposed buck converter has wider V_{IN} range and smaller inductor value.

V. CONCLUSIONS

In this paper, a low-voltage low-power buck converter is proposed for wireless sensor network systems. An automatic CCM/DCM controller is proposed to adaptively select CCM or DCM operation, therefore improving the power efficiency and enlarging the output current range. A low-voltage DMBB zero-crossing detector is proposed to enable DCM operation with both low supply voltage and normal supply voltage. A digital PWM controller is implemented for voltage regulation. By virtue of the low power controller, the proposed buck converter achieves a peak efficiency of 94% with an output current range of 50µA to 10mA. Thanks to the DCM operation, the efficiency at an output current of 100µA is improved by 20% and 9%, with an output voltage of 0.35V and 0.5V, respectively.

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