1 μm-Thickness Ultra-Flexible and High Electrode-Density Surface Electromyogram Measurement Sheet With 2 V Organic Transistors for Prosthetic Hand Control

Hiroshi Fuketa, *Member, IEEE*, Kazuaki Yoshioka, Yasuhiro Shinozuka, Koichi Ishida, *Member, IEEE*, Tomoyuki Yokota, Naoji Matsuhisa, Yusuke Inoue, Masaki Sekino, *Member, IEEE*, Tsuyoshi Sekitani, Makoto Takamiya, *Member, IEEE*, Takao Someya, *Member, IEEE*, and Takayasu Sakurai, *Fellow, IEEE*

***Abstract*—A 64-channel surface electromyogram (EMG) measurement sheet (SEMS) with 2 V organic transistors on a 1 μm-thick ultra-flexible polyethylene naphthalate (PEN) film is developed for prosthetic hand control. The surface EMG electrodes must satisfy the following three requirements; high mechanical flexibility, high electrode density and high signal integrity. To achieve high electrode density and high signal integrity, a distributed and shared amplifier (DSA) architecture is proposed, which enables an in-situ amplification of the myoelectric signal with a fourfold increase in EMG electrode density. In addition, a post-fabrication select-and-connect (SAC) method is proposed to cope with the large mismatch of organic transistors. The proposed SAC method reduces the area and the power overhead by 96% and 98.2%, respectively, compared with the use of conventional parallel transistors to reduce the transistor mismatch by a factor of 10.**

***Index Terms*—Electromyogram, organic large-area electronics, surface EMG measurement.**

I. Introduction

SURFACE electromyogram (EMG), which measures a voltage waveform produced by skeletal muscles on a skin, is an important tool for applications detecting the human will of motion, such as for prosthetic hands [1]–[3]. In this paper, electrodes for measuring surface EMG are focused on, as shown in Fig. 1. In the application to a prosthetic hand, the electrodes must satisfy the following three requirements to achieve reliable and precise hand control.

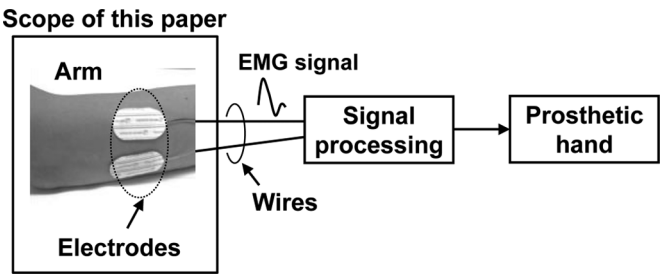


Fig. 1. Prosthetic hand control system with surface EMG.

1) High Mechanical Flexibility: The EMG electrodes are placed on the skin and if the electrodes are rigid, measurement over a long time period is annoying. Thus, the electrodes should be mechanically flexible.

2) High Electrode Density: A multipoint EMG measurement is required to precisely control the hand [4], [5].

3) High Signal Integrity: As shown in Fig. 1, the EMG signals on the electrodes are obtained through wires. These wires are sensitive to cable motion artifacts [6]. The number of the wires between the electrodes and the front-end circuits increases with increasing number of measurement points, which degrades signal integrity of EMG. Signal integrity should be taken into account, since the voltage of the measured surface EMG is significantly small, typically ranges from tens of micro-volt amplitude to several milli-volt amplitude [7], [8].

It is difficult for the conventional passive electrodes [4], [5], [8]–[10] and active electrodes [11] to satisfy all of these requirements. Thus, a surface EMG measurement sheet (SEMS), on which an EMG electrode array and a front-end amplifier array with 2 V organic transistors are integrated on a 1 μm-thick ultra-flexible film, is developed in this paper to address these challenges. The front-end amplifiers in the proposed SEMS can reduce the output impedance and increase the S/N ratio, which improves the signal integrity.

The design challenges of organic circuits for the amplifier array are as follows: 1) the decrease in the electrode density due

Manuscript received October 14, 2013; revised November 29, 2013; accepted March 02, 2014. Date of publication June 10, 2014; date of current version January 15, 2015. This paper was recommended by Associate Editor S. Gambini.

H. Fuketa, K. Yoshioka, M. Takamiya, and T. Sakurai are with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan, and also with Exploratory Research for Advanced Technology (ERATO), Japan Science and Technology Agency (JST), Tokyo 113-0032, Japan (e-mail: fuketa@iis.u-tokyo.ac.jp).

Y. Shinozuka was with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan. He is now with the Corporate Research and Development Center, Toshiba Corporation, Kawasaki 212-8582, Japan.

K. Ishida was with the Institute of Industrial Science, University of Tokyo, Tokyo 153-8505, Japan. He is now with the Dresden University of Technology, 01069 Dresden, Germany.

T. Yokota, N. Matsuhisa, Y. Inoue, M. Sekino, T. Sekitani, and T. Someya are with the Department of Electrical Engineering and Information Systems, School of Engineering, University of Tokyo, Tokyo 113-8656, Japan, and also with Exploratory Research for Advanced Technology (ERATO), Japan Science and Technology Agency (JST), Tokyo 113-0032, Japan.

Digital Object Identifier 10.1109/TBCAS.2014.2314135

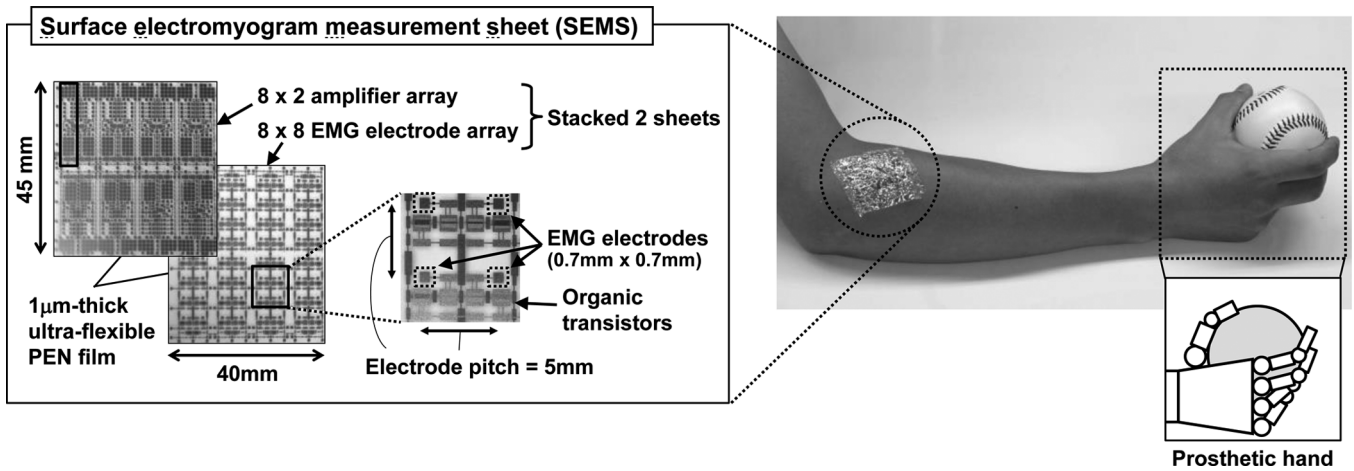


Fig. 2. Developed 64 channel surface electromyogram measurement sheet (SEMS).

to the large area of the amplifier, and 2) the mismatch of amplifiers due to the large mismatch of organic transistors. To solve these problems, we propose 1) a distributed and shared amplifier (DSA) architecture for the in-situ amplification of the myoelectric signal with a fourfold increase in EMG electrode density, and 2) a post-fabrication select-and-connect (SAC) method that reduces the area and power overhead by 96% and 98.2%, respectively, compared with the use of conventional parallel transistors to reduce the transistor mismatch by 1/10 times. Both the DSA architecture and the SAC method will be essential in the large-scale-array measurement of biomedical signals with flexible and printed electronics.

The feasibility of SEMS has been demonstrated in [12]. The major contributions of this paper beyond the preliminary work are as follows: 1) The gain of amplifiers with a pMOS-only inverter is analytically evaluated, and 2) Two types of the SAC method are proposed and compared in terms of the area and power overhead.

This paper is organized as follows. Section II describes the details of the developed SEMS and DSA. The proposed SAC method is explained in Section III. Section IV shows measurement results of the organic amplifier implemented SEMS and measured waveforms of the surface EMG obtained by SEMS. Finally, Section V concludes this paper.

II. Surface Electromyogram Measurement Sheet

A. Overview

Fig. 2 shows a photograph of the developed 45×40 mm^2 64-channel surface EMG measurement sheet (SEMS). In SEMS, an 8×8 EMG electrode array sheet and an 8×2 front-end amplifier array sheet with 2 V organic transistors are stacked. These organic transistors are fabricated on a 1 μm-thick polyethylene naphthalate (PEN) film, which enables ultra-flexibility as shown in Fig. 3.

We use 2 V organic pMOS transistors with the organic semiconductor of DNTT [13] and the gate dielectric of a self aligned monolayer (SAM) technology [14], as shown in Fig. 4, which requires a pMOS-only circuit design. SAM technology enables a total gate oxide thickness of 6 nm and 2 V operation, and

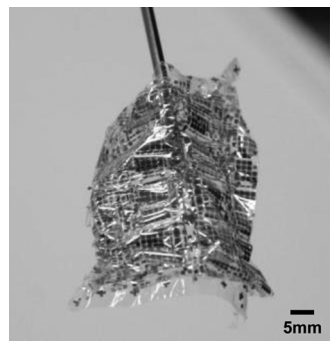


Fig. 3. Photograph of ultra-flexible SEMS, which is fabricated on 1 μm-thick PEN film with 2 V organic transistors.

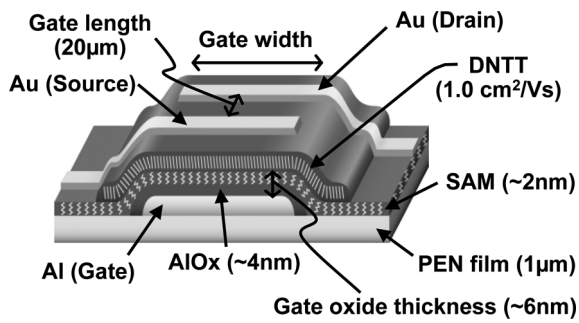


Fig. 4. Device structure of 2 V organic pMOS transistor.

DNTT is stable material with a high mobility of 1.0 cm^2/Vs [15]. The minimum gate length is 20 μm. The minimum gate length is determined by the metal mask resolution [16]. The details about the organic transistors fabricated on the ultra-thin PEN film have been described in [17]. The mechanical stability of the transistors has been also demonstrated in [17].

Table I compares SEMS with the conventional EMG electrodes. The passive electrodes can be implemented on flexible substrates [4], [5], [8]–[10], which enables high mechanical flexibility and high electrode density, since they only include electrodes and do not include any active devices, such as amplifiers. The previous works about the EMG electrodes for the prosthetic hand control [4], [5] have reported that the

TABLE I
COMPARISON BETWEEN CONVENTIONAL ELECTRODES AND SEMS

	Passive electrode [4,5] (Conv.)	Active electrode [11] (Conv.)	SEMS (This work)
Mechanical flexibility	Flexible ✓	Rigid	Ultra-flexible ✓
Electrode density	High ✓ (2~5 channels/cm²)	Low (<1 channels/cm²)	High ✓ (3.6 channels/cm²)
Signal integrity	Low (without amplifiers)	High ✓ (with amplifiers)	High ✓ (with amplifiers)

electrode pitch of from 5 to 7 mm and the electrode density of from 64 channels per 31 cm^2 to 130 channels per 27 cm^2 are used to achieve precise control. However, signal integrity of the passive electrode is low, because amplifiers are not located near electrodes. In the active electrodes [11], on the other hand, amplifiers are located near electrodes, and hence high signal integrity can be achieved. However, the amplifiers are rigid and large, which makes mechanical flexibility and electrode density low. Although the flexible active electrodes have been demonstrated in [18], the electrodes are not arrayed and the gain of the amplifier of the active electrodes is small.

Therefore, it is difficult for the conventional passive and active electrodes to satisfy all the three requirements of electrodes for the prosthetic hand control; high mechanical flexibility, high electrode density, and high signal integrity. In contrast, both the surface EMG electrodes and organic amplifiers are fabricated on the 1 μm-thick PEN film in the proposed SEMS, which enables ultra-flexible electrodes with high electrode density and signal integrity as shown in Table I.

B. Distributed and Shared Amplifier (DSA) Architecture

One of the design issues of organic circuits is the increase in electrode density due to the large area of the organic amplifier, which will be explained in Section II.C. To address this issue, distributed and shared amplifier (DSA) architecture for the in-situ amplification of the myoelectric signal is proposed.

Fig. 5 shows the circuit schematic of SEMS to which the proposed DSA is applied. In SEMS with DSA, one amplifier is shared with four EMG electrodes, which increases the electrode density fourfold. In addition, the EMG electrode array and the amplifier array are fabricated on separate sheets and the sheets are stacked [19] to further increase the electrode density.

In Block00, one of the four EMG electrodes is selected by local word line (LWL) signals LWL0 to LWL3, and the source-followered signal is amplified by the amplifier. Then, the two outputs of the amplifiers are selected by global word line (GWL) signals GWL0 and GWL1. Although eight columns (LWL0–LWL7) are implemented in the developed SEMS as shown in Fig. 5, the columns of SEMS can be easily expanded by adding GWL signals.

With the proposed DSA architecture, the electrode pitch of 5 mm and the electrode density of 64 channels per 18 cm^2 are achieved. It corresponds to 3.6 channels/cm^2 and is comparable with that of the conventional passive electrodes as listed in Table I.

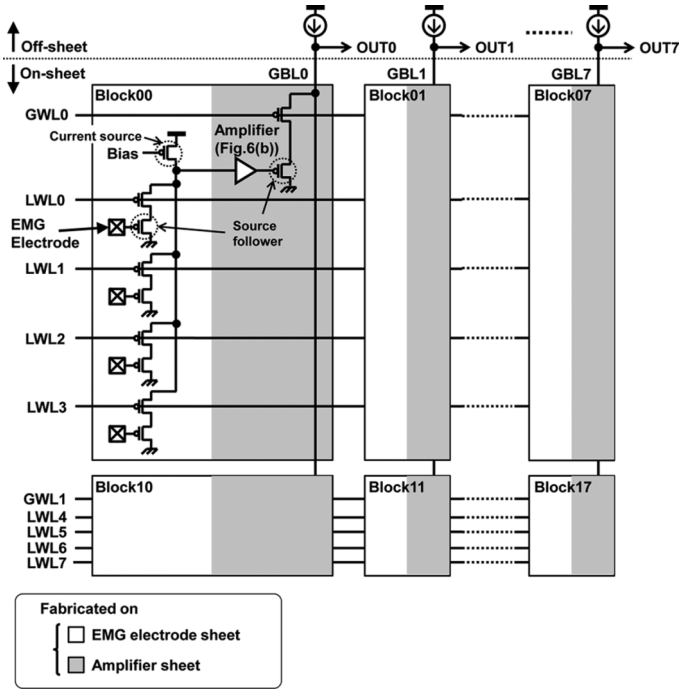


Fig. 5. Circuit schematic of SEMS with proposed distributed and shared amplifier (DSA) architecture.

C. Inverter-Based Amplifier Design

As described in Section II.A, we use organic pMOS process, which requires a pMOS-only circuit design. Therefore, an amplifier based on a pMOS-only inverter is investigated in this section.

In pMOS-only circuit design, it is difficult to increase the gain of an amplifier. An amplifier based on a pseudo-CMOS inverter [19], [20] shown in Fig. 6(a) achieves a high gain [19], although it requires a negative voltage [V_{SS} in Fig. 6(a)]. Therefore, in this work, a pMOS-only amplifier with an AC-coupled load based on [21] is used, which does not require a negative voltage. Fig. 6(b) shows a circuit schematic of the pMOS-only amplifier with the AC-coupled load. For comparison, a conventional diode load is also shown. In Fig. 6, R_1 is required to determine the bias voltage of the input signal of the inverter-based amplifier.

In this section, the frequency dependences of the gains of the pMOS-only amplifiers with the diode load and AC-coupled load analytically are evaluated. In this evaluation, the gain of the inverter is discussed when an AC signal is input to the pMOS-only inverter as shown in the inset of Fig. 7. For simplicity, any parasitic resistances and capacitances of the transistors are ignored.

A_D denotes the gain of the pMOS-only amplifier with the diode load and is given by

$$|A_D| = g_{m2}\left(\frac{1}{g_{ds2}} \parallel \frac{1}{g_{ds1}} \parallel \frac{1}{g_{m1}}\right) = \frac{g_{m2}}{g_{ds2} + g_{ds1} + g_{m1}} \tag{1}$$

where $g_{m1(2)}$ and $g_{ds1(2)}$ are the transconductance and output conductance of transistor M1(M2), respectively.

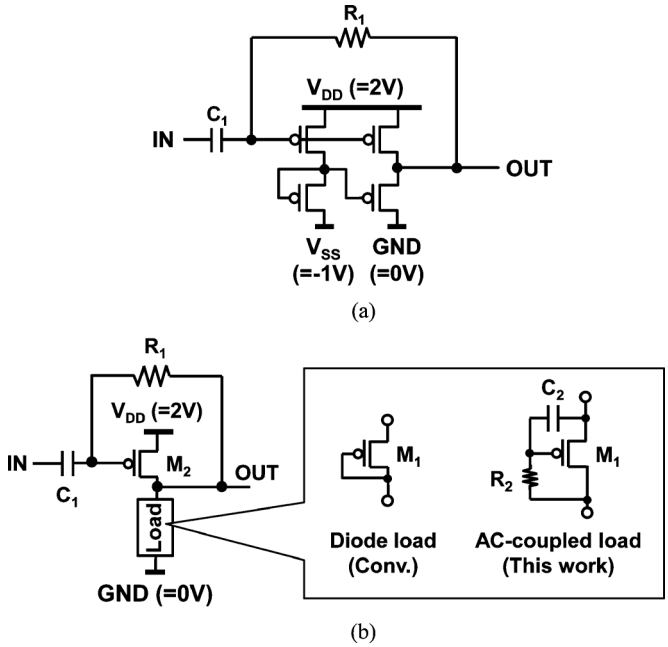


Fig. 6. Circuit schematic of amplifier with 2 V organic pMOS. (a) Amplifier based on pseudo-CMOS inverter [19]. (b) Amplifier based on pMOS-only inverter.

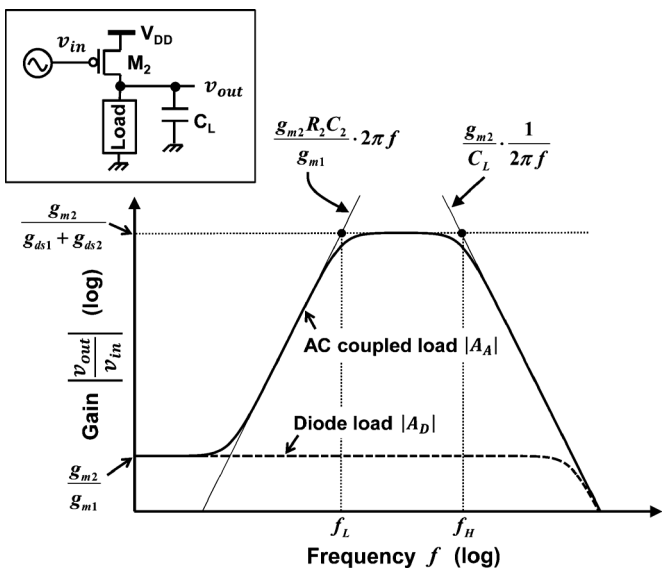


Fig. 7. Gain dependence on frequency of pMOS-only amplifiers.

Typically, g_{m1} is much larger than g_{ds1} and g_{ds2}. Thus, A_D is approximated as

$$|A_D| \cong \frac{g_{m2}}{g_{m1}}. \tag{2}$$

This equation indicates that the gain of the pMOS-only amplifier with the diode load is small.

In contrast, the gain of the amplifier with the AC-coupled load A_A is expressed as

$$A_A(s) = g_{m2}\left(\frac{1}{g_{ds2}} \parallel \frac{1}{g_{ds1}} \parallel \frac{1+R_2C_2s}{g_{m1}}\right). \tag{3}$$

The frequency dependence of A_A is shown in Fig. 6. A_A can be approximated as

$$|A_A| \cong \frac{g_{m2}}{g_{ds2}+g_{ds1}} \, (f_L < f < f_H) \tag{4}$$

where f_L and f_H are lower and higher cutoff frequencies, respectively, and they are expressed as

$$f_L = \frac{1}{2\pi R_2 C_2} \cdot \frac{g_{m1}}{g_{ds1}+g_{ds2}}, \tag{5}$$

$$f_H = \frac{g_{ds1}+g_{ds2}}{2\pi C_L}. \tag{6}$$

Equation (4) indicates that the gain of the amplifier with the AC-coupled load is much larger than that with the diode load (shown in (2)), since g_{ds1} and g_{ds2} are typically smaller than g_{m1}.

One of disadvantages of the amplifier with the AC-coupled load is that the pseudo-CMOS inverter has a constant gain, whereas the gain of the amplifier with the AC-coupled load decreases in the low frequency region as shown in Fig. 7. Since the lower cutoff frequency f_L is inversely proportional to R_2C_2 as indicated in (5), R_2C_2 must be determined such that f_L satisfies the frequency band required for the surface EMG, which is typically 10-to-500 Hz [7]. In addition, R_1C_1 in Fig. 6 also determines the lower cutoff frequency. In this paper, C_1 and C_2 are 47 nF, and R_1 and R_2 are implemented by always-off (i.e., the gate voltage is always tied to V_{DD}) transistors. R_1 and R_2 are typically larger than 100 MΩ, and the influence of resistance variations in R_1 and R_2 is small because large enough capacitances C_1 and C_2 of 47 nF are used. The measurement results of the amplifier with AC-coupled load will be shown in Section IV.

III. Select-and-Connect Method to Reduce Mismatch

A. Overview

Fig. 8 shows the measured I_{DS}-V_{DS} characteristics of 11 organic pMOS transistors. As shown in this figure, variations of characteristics of organic transistors are large. Therefore, one of the design challenges of organic circuits for the amplifier array is the mismatch of amplifiers due to such large mismatch of organic transistors.

In order to reduce such large mismatch, parallel transistors are conventionally used. However, the area and power overhead in the conventional parallel transistors are large. In this paper, a post-fabrication select-and-connect (SAC) method that reduces the transistor mismatch with small area and power overhead is proposed. Fig. 9 explains the proposed SAC method. The SAC method is divided into the following three steps.

First (step 1), the I-V characteristics (e.g., threshold voltage and ON-current (I_{ON})) of each transistor are measured. 2N measurements are required when the number of parallel transistors is N.

Then (step 2), N_1 and N_2 transistors are selected from the left and right groups, respectively, as shown in Fig. 9(c), on the basis of the results of calculation to minimize the target mismatch.

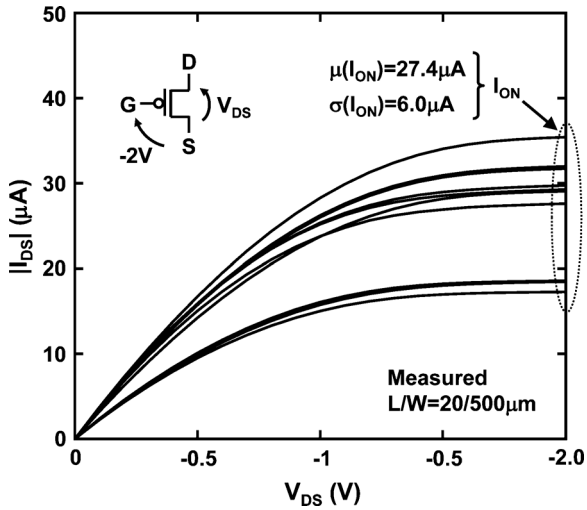


Fig. 8. Measured I_{DS}-V_{DS} characteristics of 11 organic pMOS transistors.

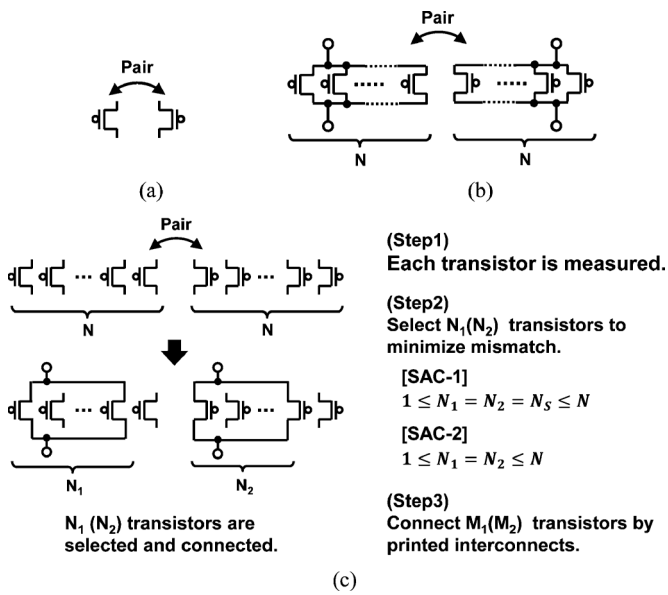


Fig. 9. Conventional and proposed transistor mismatch reduction techniques. Post-fabrication select-and-connect (SAC) method is proposed. (a) Single transistor. (b) Parallel transistors. (c) Proposed select-and-connect (SAC) method.

In this paper, two types of the transistor selection methods are considered; SAC-1 and SAC-2. In SAC-1, N_1 and N_2 are fixed to a certain value N_S ($N_1 = N_2 = N_S \le N$). N_S is chosen independently of N. In SAC-2, N_1 and N_2 are equal to or less than N ($N_1 = N_2 \le N$). The numbers of combination of SAC-1 and SAC-2 are listed in Table II.

Finally (step 3), the selected N_1 (N_2) transistors are connected by inkjet-printed interconnects. Fig. 10 shows a photograph of inkjet-printed interconnects when N is 4 and N_1 is 2. In this work, the width of interconnects is 10 μm. In [22], it has been demonstrated that the minimum line and space of inkjet-printed interconnects is 1 μm. In contrast, the width of metal wire lines in SEMS is several hundreds of micrometers. Therefore, it is feasible to print interconnects by the inkjet printer.

TABLE II
COMPARISON BETWEEN CONVENTIONAL PARALLEL TRANSISTORS AND PROPOSED SAC

	Single transistor	Parallel transistors (Conv.)	SAC-1 (Proposed)	SAC-2 (Proposed)
Area	1	N	N	N
Power	1	N	N_S ($\le$ N)	< N
Mismatch	1	$\frac{1}{\sqrt{N}}$	$< \frac{1}{\sqrt{N}}$	$< \frac{1}{\sqrt{N}}$
# of combinations	1	1	$\left({}_N C_{N_S}\right)^2$	$\sum_{i=1}^{N} \left({}_N C_i\right)^2$

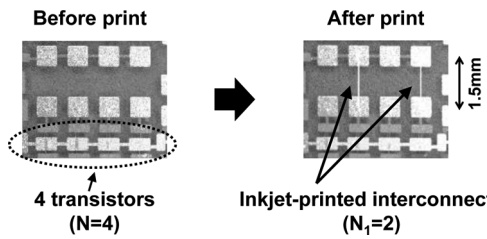


Fig. 10. Photograph of inkjet-printed interconnects used in proposed SAC method when N is 4 and N1 is 2.

Although the proposed SAC is too costly and hence it is impractical in the silicon VLSI technology, the SAC takes advantage of the printed/printable electronics.

Table II summarizes the comparison between the conventional N parallel transistors and the proposed SAC method in terms of the number of combinations, area, power, and mismatch. In the SAC method, the mismatch and power are less than $\sqrt{N}$-fold and N-fold, respectively, at the cost of an N-fold area increase. The details about the mismatch reduction and the area and power overhead will be discussed in Section III.B.

B. Simulation Results

In this work, the target mismatch is I_{ON}. It should be noted that the proposed SAC is also applicable to the mismatch reduction of other characteristics, such as threshold voltage. On the basis of the measured $\mu(I_{ON})$ and $\sigma(I_{ON})$, I_{ON} mismatch is simulated by Monte-Carlo simulations assuming that I_{ON} is normally distributed, and the conventional parallel transistors (Fig. 9(b)) and the proposed SAC (Fig. 9(c)) are compared. It should be noted that SAC can reduce any random variations, which cause mismatch, and does not depend on their distributions. The number of trials of the Monte-Carlo simulations is one million.

Fig. 11 shows the simulated N dependence of I_{ON} mismatch. The I_{ON} mismatch of the parallel transistors is proportional to $1/\sqrt{N}$ according to Pelgrom's law. In contrast, the I_{ON} mismatch of the proposed SAC is much smaller than that of the conventional parallel transistors and SAC-2 is always better than SAC-1 in terms of the mismatch reduction at the identical N. The number of combinations of SAC-2 is, however, larger than that of SAC-1 as listed in Table II, which means the cost to find

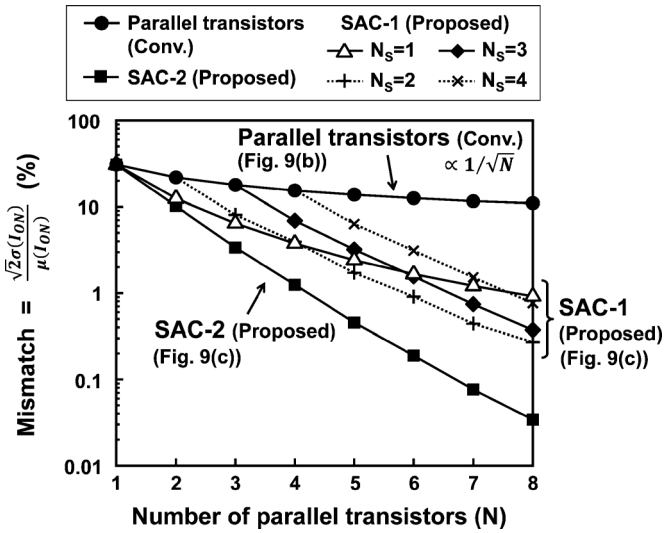


Fig. 11. Simulated N dependence of I_{ON} mismatch.

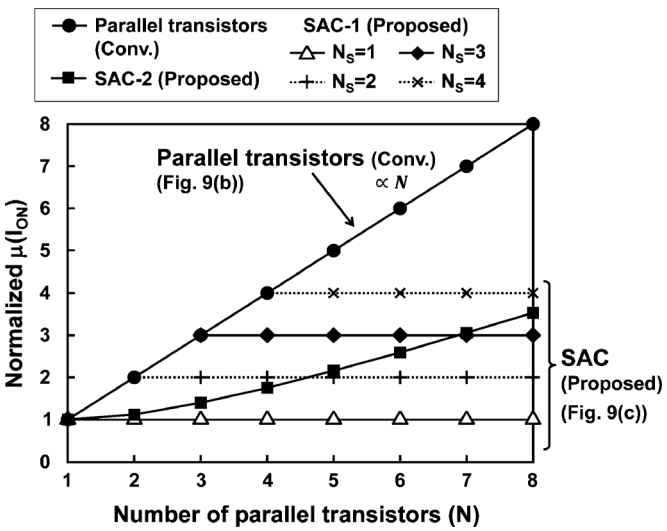


Fig. 12. Simulated N dependence of average I_{ON}.

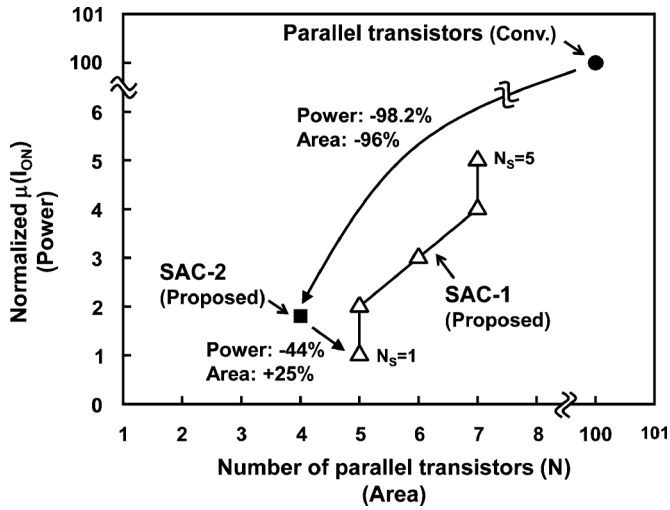


Fig. 13. Proposed SAC-1 and SAC-2 methods are compared with conventional parallel transistors in terms of area and power to reduce mismatch by 1/10 times.

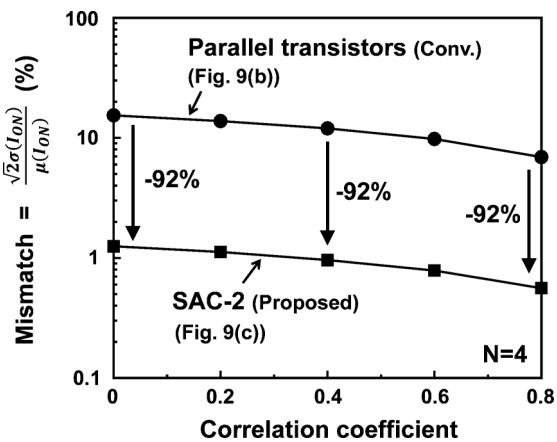


Fig. 14. Simulated dependence of I_{ON} mismatch on correlation coefficient in conventional parallel transistors and proposed SAC method when I_{ON} is normally distributed with correlations. Number of parallel transistors (N) is 4.

the optimum combination in SAC-2 is larger compared with SAC-1.

Fig. 12 shows the N dependence of $\mu(\mathrm{I_{ON}})$ (= average power). $\mu(\mathrm{I_{ON}})$ of the conventional parallel transistors is proportional to N. In SAC-1, the number of selected transistors is fixed to $\mathrm{N_S}$ regardless of N, and hence $\mu(\mathrm{I_{ON}})$ does not depend on N. In SAC-2, on the other hand, $\mu(\mathrm{I_{ON}})$ rises as N increases because the number of selected transistors in SAC-2 is less than or equal to N. In both SAC-1 and SAC-2 the mismatch and power can be reduced compared with the conventional parallel transistors at the same N (= area).

Finally, SAC-1 and SAC-2 are compared in Fig. 13 in terms of the area and power. In this figure, the case where the mismatch is reduced by a factor of 10 is considered. In the conventional parallel transistors, $\mathrm{N} = 100$ is required, because the mismatch of the parallel transistors is proportional to $1/\sqrt{N}$. Consequently, 100-fold power ($= \mu(\mathrm{I_{ON}})$) is required. In contrast, N is just 4 in SAC-2, which corresponds to 96% and 98.2% reductions in the area and power overhead, respectively, compared with those of the parallel transistors. If the area is not a primary concern, SAC-1 ($\mathrm{N} = 5$ and $\mathrm{N_S} = 1$) can further reduce the power by 44% at the cost of 25% area increase compared with SAC-1. This means that the SAC-1 method achieves the 1/10 times reduction in the mismatch with the smallest power overhead and the SAC-2 method achieves it with the smallest area overhead. Therefore, which method is better differs case by case. In both cases, the area and power are much smaller than those of the conventional parallel transistors. The measurement cost of SAC is one of the problems. However, N is just 4, which means only 8 measurements need to be taken, to reduce the mismatch by a factor of 10. Therefore, the measurement cost is not large.

In the abovementioned discussion, it is assumed that I_{ON} is normally distributed without correlations. Finally, we investigate the case when I_{ON} is normally distributed with correlations. Fig. 14 shows the simulated dependence of I_{ON} mismatch on the correlation coefficient in the conventional parallel transistors and the proposed SAC-2 method when N is 4.

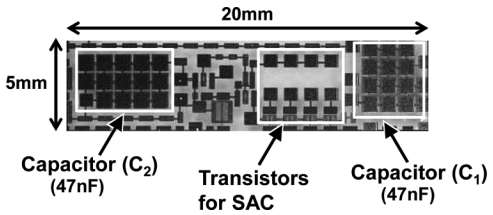


Fig. 15. Photograph of pMOS-only amplifier with AC-coupled load. Circuit schematic is shown in Fig. 6(b).

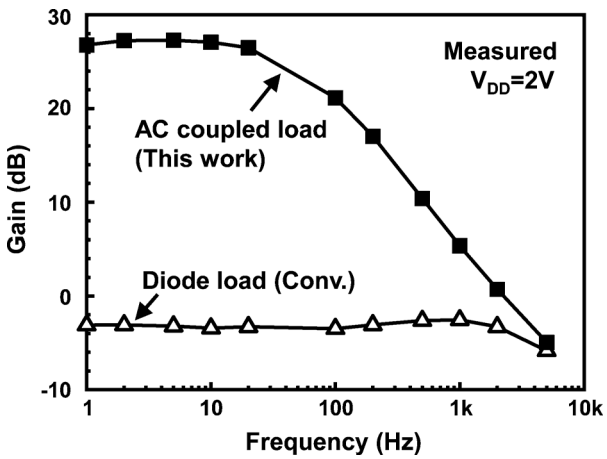


Fig. 16. Measured frequency dependence of gain of amplifiers with different loads.

Even if I_{ON} is distributed with correlations, SAC-2 is still effective, and can reduce I_{ON} mismatch by 92% compared with the conventional parallel transistors, regardless of the correlation coefficient.

IV. Measurement Results

The photograph of the pMOS-only amplifier with the AC-coupled load used in this work is shown in Fig. 15. The size of the amplifier is 20 mm $\times$ 5 mm. C_1 and C_2 are implemented by MIM capacitors, whose capacitance is 700 nF/cm^2 [19], and R_1 and R_2 are implemented by always-off transistors.

Fig. 16 shows a measured frequency dependence of the gain of the amplifiers when the supply voltage is 2 V. The gain of the amplifier with the AC-coupled load is much higher than that with the diode load, which agrees the analytical evaluation described in Section II.C. The power consumption of the amplifiers with the AC-coupled load is 30 μW. The target specifications of the amplifier are "gain at 100 Hz$>$ 20 dB" and "gain at 500 Hz $>$ 10 dB", because the typical amplitude and frequency band of the surface EMG are from tens of micro-volt to several milli-volt and from 10 Hz to 500 Hz, respectively. In Fig. 16, the measured gains at 100 Hz and 500 Hz are 21 dB and 10 dB, respectively, which satisfy the target specification. The measured unity gain frequency is 2 kHz. In Fig. 16, The gain of the amplifier with the diode load is less than 0 dB, because g_{m2} is smaller than g_{m1} in (2).

Fig. 17 shows the measurement setup and measured waveforms of the surface EMG with the organic amplifier. In this measurement, two electrodes are used. Wires are connected to the organic amplifier using a conductive epoxy. The maximum

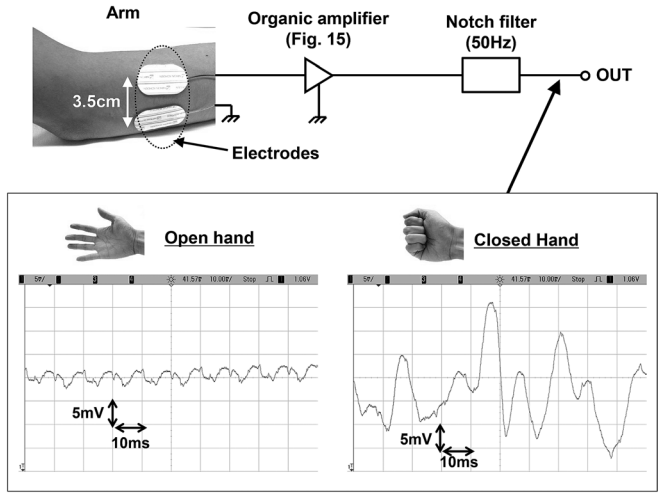


Fig. 17. Measurement setup and measured raw waveforms with organic amplifier.

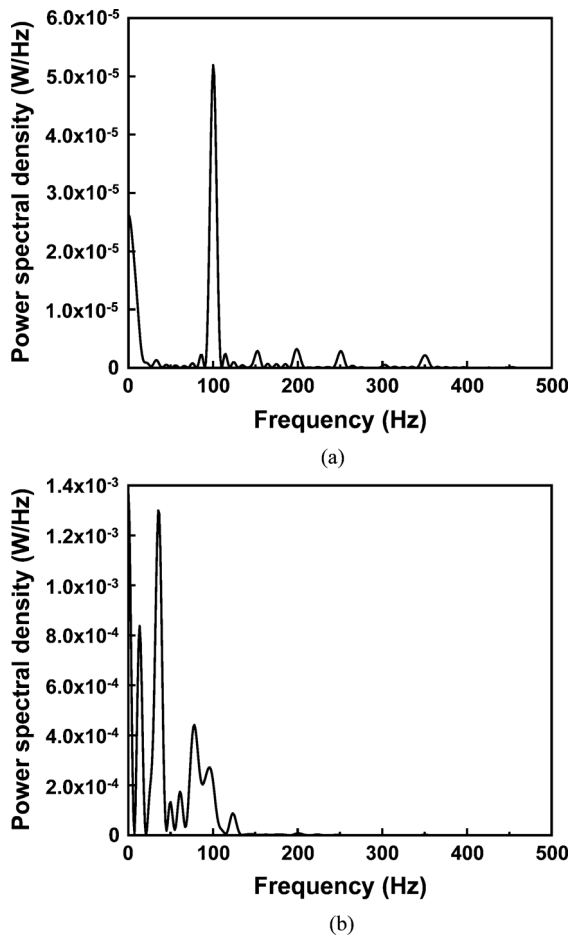


Fig. 18. Power spectrum of measured waveforms shown in Fig. 17. (a) Open hand. (b) Closed hand.

amplitude and the frequency of the waveforms with closed hand are 35 mV and 100 Hz, respectively. Fig. 18 illustrates the power spectrum of the measured waveforms shown in Fig. 17. When the hand is open (Fig. 18(a)), only harmonics of 50 Hz are observed, whereas signals between 50–150 Hz are observed when the hand is closed (Fig. 18(b)). From the shape of the power

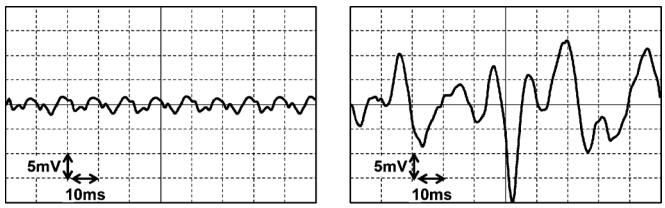


Fig. 19. Band-pass filtered waveforms of the raw data shown in Fig. 17. Cutoff frequencies are 20 and 500 Hz. (a) Open hand. (b) Closed hand.

TABLE III
KEY FEATURES AND PERFORMANCE SUMMARY

Organic transistors	
Semiconductor material	DNTT (Mobility=1.0 cm^2/Vs)
Gate oxide material, thickness	SAM 2nm + AlOx 4nm = 6nm
Minimum gate length	20µm
Surface electromyogram measurement sheet (SEMS)	
Sheet size	45mm x 40mm
Number of amplifiers	16
Number of EMG electrodes	8 x 8 (5mm pitch)

spectrum, these signals are considered as the surface EMG and the signals below 50 Hz may be caused by motion artifacts. This means the difference between the waveforms with open hand and closed hands is clearly observed. Fig. 19 shows the waveforms that are band-pass filtered with the cutoff frequencies of 20 and 500 Hz [7], [23]. In this paper, it is assumed that such filtering is performed in signal processing in Fig. 1.

Table III summarizes key features.

V. CONCLUSION

In this paper, a 64-channel surface electromyogram (EMG) measurement sheet (SEMS) were developed for prosthetic hand control. For reliable and precise hand control, the following three requirements must be satisfied for the surface EMG electrodes; high mechanical flexibility, high electrode density and high signal integrity. The developed SEMS was fabricated on 1 μm-thick ultra-flexible PEN film with 2 V organic transistors and the distributed and shared amplifier (DSA) architecture was applied for the in-situ amplification of the myoelectric signal, which enables ultra-flexibility, high electrode density and high signal integrity. Furthermore, we have to deal with the large mismatch of organic transistors. To address this challenge, the post-fabrication select-and-connect (SAC) method was proposed in this paper. To reduce the transistor mismatch by a factor of 10, the proposed SAC method can reduce the area and the power overhead by 96% and 98.2%, respectively, compared with the use of conventional parallel transistors.

REFERENCES

[1] S. Nishimura, Y. Tomita, and T. Horiuchi, "Clinical application of an active electrode using an operational amplifier," *IEEE Trans. Biomed. Eng.*, vol. 39, no. 10, pp. 1096–1099, Oct. 1992.

[2] O. Fukuda, T. Tsuji, M. Kaneko, and A. Otsuka, "A human-assisting manipulator teleoperated by EMG signals and arm motions," *IEEE Trans. Robot. Autom.*, vol. 19, no. 2, pp. 210–222, Apr. 2003.

[3] S. Morita, T. Kondo, and K. Ito, "Estimation of forearm movement from EMG signal and application to prosthetic hand control," in *Proc. IEEE Int. Conf. Robotics and Automation*, 2001, pp. 3692–3697.

[4] P. Liu, D. Brown, F. Martel, D. Rancourt, and E. Clancy, "EMG-to-force modeling for multiple fingers," in *Proc. IEEE Annu. Northeast Bioengineering Conf.*, 2011, pp. 1–2.

[5] D. Staudenmann, I. Kingma, D. Stegeman, and J. Dieën, "Towards optimal multi-channel EMG electrode configurations in muscle force estimation: A high density EMG study," *Elsevier J. Electromyogr. Kinesiology*, vol. 15, no. 1, pp. 1–11, Feb. 2005.

[6] J. Xu, R. Yazicioglu, B. Grundlehner, P. Harpe, K. Makinwa, and C. Van Hoof, "A 160 μW 8-channel active electrode system for EEG monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 555–567, Dec. 2011.

[7] R. Merletti and P. Parker, *Electromyography Physiology, Engineering, and Noninvasive Applications*. Hoboken, NJ, USA: Wiley-Interscience, 2004.

[8] B. Lapatki, J. Dijk, I. Jonas, M. Zwarts, and D. Stegeman, "A thin, flexible multielectrode grid for high-density surface EMG," *Amer. Phys. Soc. J. Appl. Phys.*, vol. 96, no. 1, pp. 327–336, Jan. 2004.

[9] L. Guo, G. S. Guvanasen, X. Liu, C. Tuthill, T. R. Nichols, and S. P. DeWeerth, "A PDMS-based integrated stretchable microelectrode array (isMEA) for neural and muscular surface interfacing," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 1, pp. 1–10, Feb. 2013.

[10] D. H. Kim, J. V. , J. J. Amsden, J. Xiao, L. Vigeland, Y. S. Kim, J. A. Blanco, B. Panilaitis, E. S. Frechette, D. Contreras, D. L. Kaplan, F. G. Omenetto, Y. Huang, K. C. Hwang, M. R. Zakin, B. Litt, and J. A. Rogers, "Dissolvable films of silk fibroin for ultrathin conformal bio-integrated electronics," *Nature Mater.*, vol. 9, pp. 511–517, Apr. 2010.

[11] Surface EMG Sensors [Online]. Available: http://www.delsys.com

[12] H. Fuketa, K. Yoshioka, Y. Shinozuka, K. Ishida, T. Yokota, N. Matsuhisa, Y. Inoue, M. Sekino, T. Sekitani, M. Takamiya, T. Someya, and T. Sakurai, "1 μm thickness 64 channel surface electromyogram measurement sheet with 2 V organic transistors for prosthetic hand control," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 2013, pp. 104–105.

[13] T. Yamamoto and K. Takimiya, "Facile synthesis of highly π-extended heteroarenes, dinaphtho[2,3-b:2',3'-f]chalcogenopheno[3,2-b]chalcogenophenes, and their application to field-effect transistors," *J. Amer. Chem. Soc.*, vol. 129, no. 8, pp. 2224–2225, Aug. 2007.

[14] H. Klauk, U. Zschieschang, J. Pflaum, and M. Halik, "Ultralow-power organic complementary circuits," *Nature*, vol. 445, pp. 745–748, Feb. 2007.

[15] K. Ishida, T. Huang, K. Honda, Y. Shinozuka, H. Fuketa, T. Yokota, U. Zschieschang, H. Klauk, G. Tortissier, T. Sekitani, H. Toshiyoshi, M. Takamiya, T. Someya, and T. Sakurai, "Insole pedometer with piezoelectric energy harvester and 2 V organic circuits," *IEEE J. Solid-State Circuits*, vol. 48, no. 1, pp. 255–264, Jan. 2013.

[16] K. Ishida, N. Masunaga, Z. Zhou, T. Yasufuku, T. Sekitani, U. Zschieschang, H. Klauk, M. Takamiya, T. Someya, and T. Sakurai, "Stretchable EMI measurement sheet with 8×8 coil array, 2 V organic CMOS decoder, and 0.18 um silicon CMOS LSIs for electric and magnetic field detection," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 249–259, Jan. 2010.

[17] M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. B. Gogonea, S. Bauer, and T. Someya, "An ultra-lightweight design for imperceptible plastic electronics," *Nature*, vol. 499, pp. 458–463, July 2013.

[18] D. H. Kim, N. Lu, R. Ma, Y. S. Kim, R. H. Kim, S. Wang, J. Wu, S. M. Won, H. Tao, A. Islam, K. J. Yu, T. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H. J. Chung, H. Keum, M. McCormick, P. Liu, Y. W. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, and J. A. Rogers, "Epidermal electronics," *Science*, vol. 333, no. 6044, pp. 838–843, Aug. 2011.

[19] T. Yokota, T. Sekitani, T. Tokuhara, U. Zschieschang, H. Klauk, T.-C. Huang, M. Takamiya, T. Sakurai, and T. Someya, "Sheet-type organic active matrix amplifier system using Vth-tunable, pseudo-CMOS circuits with floating-gate structure," in *Proc. IEEE Int. Electron Devices Meeting , Tech. Dig.*, 2011, pp. 335–338.

[20] K. Ishida, T. Huang, K. Honda, T. Sekitani, H. Nakajima, H. Maeda, M. Takamiya, T. Someya, and T. Sakurai, "100-V AC power meter system-on-a-film (SoF) integrating 20-V organic CMOS digital and analog circuits with floating gate for process variation compensation and 100-V organic PMOS rectifier," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 2011, pp. 218–219.

[21] H. Marien, M. Steyaert, E. Veenendaal, and P. Heremans, "A fully integrated $\Delta\Sigma$ ADC in organic thin-film transistor technology on flexible plastic foil," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 276–284, Jan. 2011.
[22] T. Yokota, T. Sekitani, Y. Kato, K. Kuribara, U. Zschieschang, H. Klauk, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, and T. Someya, "Low-voltage organic transistor with subfemtoliter inkjet source-drain contacts," *MRS Commun.*, vol. 1, pp. 3–6, Jun. 2011.
[23] A. Merlo and C. Isabella, "Technical aspects of surface electromyography for clinicians," *Open Rehabil. J.*, vol. 3, pp. 98–109, 2010.

Hiroshi Fuketa (S'07–M'10) received the B.E. degree from Kyoto University, Kyoto, Japan, and the M.E. and Ph.D. degrees in information systems engineering from Osaka University, Osaka, Japan, in 2002, 2008 and 2010, respectively.

Currently, he is a Research Associate with Institute of Industrial Science, The University of Tokyo, Tokyo, Japan. His research interests include ultra-low-power circuit design and large area electronics with organic transistors.

Dr. Fuketa is a member of IEICE.

Kazuaki Yoshioka received the B.S. degree in electronic engineering from The University of Tokyo, Tokyo, Japan, in 2012.

Currently, he is studying in the Department of Electrical Engineering and Information Systems, Graduate School of Engineering, The University of Tokyo. His research interests are in the field of low power circuits and power supply noise.

Yasuhiro Shinozuka received the B.S. degree, and the M.S. degree in electronic engineering from The University of Tokyo, Tokyo, Japan, in 2011 and 2013, respectively.

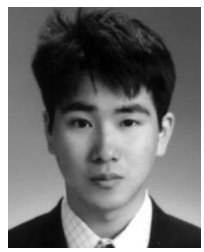
In 2013, he joined the Corporate Research and Development Center, Toshiba Corporation, Kawasaki, Japan. His research interests are in the field of in-package DC/DC converters and 3D integrated circuits, and CMOS analog circuits.

Mr. Shinozuka is a member of IEICE.

Koichi Ishida (S'00–M'06) received the B.S. degree in electronics engineering from the University of Electro-Communications, Tokyo, Japan, and the M.S. and Ph.D. degrees in electronics engineering from The University of Tokyo, Tokyo, Japan, in 1998, 2002, and 2005, respectively.

In 1989, he joined Nippon Avionics Company Ltd., Yokohama, Japan, where he developed high-reliability hybrid microcircuits for aerospace programs. From 2005 to 2007, he worked on CMOS analog and RF circuits at the Tokyo Institute of Technology, Yokohama, Japan. From 2007 to 2012, he worked on on-chip power supply circuits and organic electronics circuits at the Institute of Industrial Science, The University of Tokyo. Since July 2012, he has been working as Chair for Circuit Design and Network Theory, Dresden University of Technology, Dresden, Germany. His research interests include low-voltage low-power CMOS analog circuits, on-chip power supply circuits, and large-area flexible electronics.

Dr. Ishida is a member of IEICE.



Tomoyuki Yokota received the B.S., M.S., and Ph.D. degrees in applied physics from The University of Tokyo, Tokyo, Japan, in 2008, 2010, and 2013, respectively.

Currently, he is a Research Assistant in the Department of Electrical and Electronic Engineering, The University of Tokyo. His research interests include printed electronics, large-area electronics, and organic electronics.

Naoji Matsuhisa received the B.S. and M.S. degrees in electronic engineering from The University of Tokyo, Tokyo, Japan, in 2012 and 2014, respectively.

Currently, he is working toward the Ph.D. degree in the Department of Electrical Engineering and Information Systems, Graduate School of Engineering, The University of Tokyo. His research interests are in the field of organic electronics, flexible electronics, and stretchable electronics.

Yusuke Inoue received the Ph.D. degree in medical science from The University of Tokyo, Tokyo, Japan, in 2011.

From 2011 to 2012, he was a Research Fellow in the Graduate School of Medicine, The University of Tokyo. Since 2012, he has been a Research Fellow in the Department of Electrical and Electronic Engineering, The University of Tokyo. His research interests are Flexible electronics and biomedical engineering.

Masaki Sekino (M'03) received the B.S. degree in mechanical engineering and the Ph.D. degree in electronics engineering from The University of Tokyo, Tokyo, Japan, in 2000 and 2005, respectively.

From 2005 to 2006, he was a Research Associate in the Graduate School of Medicine, The University of Tokyo. From 2006 to 2010, he was a Research Associate in the Graduate School of Frontier Sciences, The University of Tokyo. Since 2011, he has been an Associate Professor in the Department of Electrical Engineering and Information Systems, The University of Tokyo.

Tsuyoshi Sekitani received the B.S. degree from Osaka University, Osaka, Japan, and the Ph.D. degree in applied physics from The University of Tokyo, Tokyo, Japan, in 1999 and 2003, respectively.

From 1999 to 2003, he was with the Institute for Solid State Physics (ISSP), The University of Tokyo. From 2003 to 2009, he was a Research Associate of the Quantum-Phase Electronics Center, The University of Tokyo. Since 2011, he has been an Associate Professor in the Department of Electrical and Electronic Engineering, The University of Tokyo.

Makoto Takamiya (S'98–M'00) received the B.S., M.S., and Ph.D. degrees in electronic engineering from The University of Tokyo, Tokyo, Japan, in 1995, 1997, and 2000, respectively.

In 2000, he joined the NEC Corporation, Japan, where he was engaged in the circuit design of high speed digital LSIs. In 2005, he joined The University of Tokyo, where he is an Associate Professor of the VLSI Design and Education Center. Since 2013, he has been at the University of California, Berkeley, CA, USA, as a Visiting Scholar. His research interests include the circuit design of the low-power RF circuits, the ultra low-voltage logic circuits, the low-voltage power management circuits, and the large area and flexible electronics with organic transistors.

Dr. Takamiya is a member of the technical program committee for the IEEE Symposium on VLSI Circuits. He received 2009 and 2010 IEEE Paul Rappaport Awards and the Best Paper Award at the 2013 IEEE Wireless Power Transfer Conference.

Takao Someya (M'03) received the Ph.D. degree in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1997.

In 1997, he joined the Institute of Industrial Science (IIS), The University of Tokyo, as a Research Associate and was appointed to be a Lecturer of the Research Center for Advanced Science and Technology (RCAST), The University of Tokyo, in 1998, and an Associate Professor of RCAST in 2002. From 2001 to 2003, he worked for the Nanocenter (NSEC) of Columbia University and Bell Labs, Lucent Technologies, as a Visiting Scholar. From 2003 to 2009, he was an Associate Professor in the Department of Applied Physics and Quantum-Phase Electronics Center, The University of Tokyo. Since 2009, he has been a Professor of Electrical and Electronic Engineering, The University of Tokyo. His current research interests include organic transistors, flexible electronics, plastic integrated circuits, large-area sensors, and plastic actuators.

Dr. Someya is a member of the IEEE Electron Devices Society, the Materials Research Society (MRS), and the Japanese Society of Applied Physics.

Takayasu Sakurai (S'77–M'78–SM'01–F'03) received the Ph.D. degree in electrical engineering from The University of Tokyo, Tokyo, Japan, in 1981.

In 1981, he joined Toshiba Corporation, where he designed CMOS DRAM, SRAM, RISC processors, DSPs, and SoC Solutions. He has worked extensively on interconnect delay and capacitance modeling known as Sakurai model and alpha power-law MOS model. From 1988 to 1990, he was a Visiting Researcher at the University of California, Berkeley, CA, USA, where he conducted research in the field of VLSI CAD. Since 1996, he has been a Professor at The University of Tokyo, working on low-power high-speed VLSI, memory design, interconnects, ubiquitous electronics, organic ICs, and large-area electronics. He has authored more than 400 technical publications, including 100 invited presentations and several books, and has filed more than 200 patents.

Dr. Sakurai is the executive committee chair for VLSI Symposia and a steering committee chair for IEEE A-SSCC since 2010. He served as a conference chair for the Symposium on VLSI Circuits, and ICICDT, a vice chair for ASPDAC, a TPC chair for the A-SSCC, and VLSI Symposia, an executive committee member for ISLPED and a program committee member for ISSCC, CICC, A-SSCC, DAC, ESSCIRC, ICCAD, ISLPED, and other international conferences. He was a recipient of the 2010 IEEE Donald O. Pederson Award in Solid-State Circuits, the IEEE Paul Rappaport Award (2009 and 2010), 2010 IEICE Electronics Society Award, 2009 Achievement Award of IEICE, 2005 IEEE ICICDT Award, 2004 IEEE Takuo Sugano Award, 2005 P&I Patent of the Year Award, and four product awards. He gave the keynote speech at more than 50 conferences including ISSCC, ESSCIRC, and ISLPED. He was an elected AdCom member for the IEEE Solid-State Circuits Society and an IEEE CAS and SSCS distinguished lecturer. He is an IEICE Fellow.