An 85-mV Input, 50-µs Startup Fully Integrated Voltage Multiplier with Passive Clock Boost Using On-Chip Transformers for Energy Harvesting

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***Abstract*— A fully integrated voltage multiplier with low startup voltage (V_{START}) and fast startup is developed for the energy harvesting (e.g. thermoelectric energy harvester). The generation of the high frequency clock signal with large amplitude without using off-chip components is a key to achieve the voltage multiplier. The proposed passive clock boost using two on-chip transformers with the winding turns ratio of three reduces V_{START}. The 138-MHz clock generation with a fully integrated LC oscillator enables the fast startup. The voltage multiplier fabricated in 65-nm CMOS achieves the lowest cold V_{START} of 85mV in the published fully integrated voltage multiplier and the shortest startup time of 50µs.**

I. INTRODUCTION

A wide variety of distributed tiny wireless devices including sensor devices for Internet of Things (IoT), wearable wellness devices, and implanted medical devices require the energy autonomy. One of the key enabling technologies for the energy autonomous systems is the energy harvesting [1]. The output voltage of the energy harvester, however, is often too low for the electronic devices. For example, the output voltage of the thermoelectric generator is in the range of 10mV/K to 50mV/K. For body-wearable applications, the output voltage is less than 100mV for the temperature difference of 2K. The single-cell solar cell generates 500-600mV in the outdoor and 100-200mV in the dark office environment. Therefore, a step-up DC-DC converter is required to boost the harvested (sub) 100mV to above 1V for the electronic devices. The key requirements for the low-input step-up DC-DC converter are (1) the fully integrated solution to reduce the size and the cost due to the off-chip components, (2) sub-100mV cold startup voltage (V_{START}) for the thermoelectric generator and the single-cell solar cell in the dark office environment, and (3) sub-100µs startup time (t_{START}) for the quick wake-up of the energy autonomous systems.

Though the fully integrated solutions with the capacitive voltage multiplier were reported [2-4], V_{START} of them are above 120mV, because they use CMOS ring oscillators to generate the clock for the voltage multiplier and the lower limit of V_{START} is determined by the minimum supply voltage (V_{DDmin}) of the ring oscillators [5]. Theoretically, the lower limit of V_{DDmin} is 36 mV at room temperature [6], but actually V_{DDmin} is more than 100 mV due to manufacturing variations and large subthreshold slope [7]. To solve the V_{DDmin} problem, transformer-based oscillators and LC oscillators are proposed and boost converters with V_{START} of less than 50mV were reported [8-10]. The boost converters, however, require a bulky off-chip transformer [8, 9] or off-chip inductors [10], which are not the fully integrated solution. t_{START} of the boost converter is 6ms [10], which is beyond our design target of sub-100µs, because the switching frequency of the boost converter is 25kHz. To achieve t_{START} of sub-100µs, the frequency should be increased.

In this paper, a fully integrated voltage multiplier with a passive clock boost using on-chip transformers is proposed to solve these problems. The voltage multiplier fabricated in a 65-nm CMOS process achieves the lowest cold V_{START} of 85mV in the published fully integrated voltage multiplier and the shortest t_{START} of 50µs.

This paper is organized as follows. The clock generation techniques for the voltage multiplier with the passive clock boost using on-chip transformers are described in Section II. Section III shows the circuit implementation of the voltage multiplier. The experimental results are shown in Section IV. Finally, Section V concludes this paper.

II. CLOCK GENERATION FOR VOLTAGE MULTIPLIER

Various low-voltage input step-up DC-DC converters with a voltage multiplier have been proposed for the energy harvester. The circuit architecture is illustrated in Fig. 1. The clock signal (CLK) is generated with an oscillator using the low DC input voltage (V_{IN}). The n-stage voltage multiplier boosts V_{IN} to the output voltage (V_{OUT}). Consequently, V_{OUT} is given by $V_{IN} + nV_{CLK}$ under the ideal condition, where V_{CLK} is the amplitude of CLK. Thus, large V_{CLK} can reduce n required to obtain a certain V_{OUT}, such as 1V. The high frequency clock signal is also required to reduce t_{START} to sub-100µs. Therefore, the generation of the high frequency clock signal with large amplitude without using off-chip components is a key to achieve the voltage multiplier.

Fig. 2 summarizes various clock generation techniques for the low-voltage input step-up DC-DC converters. In a ring

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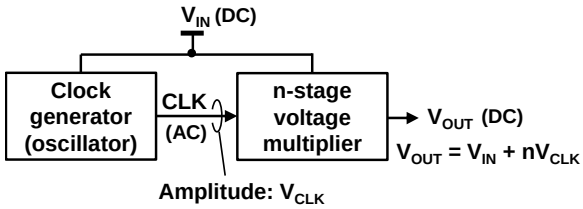


Fig. 1. Circuit architecture of low-voltage input step-up DC-DC converter with voltage multiplier.

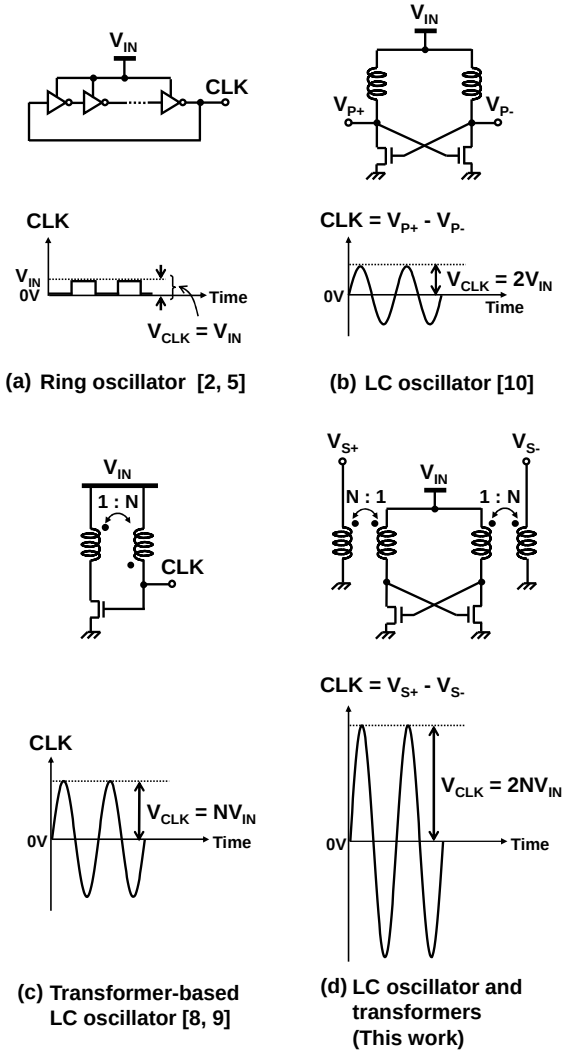


Fig. 2. Clock generation techniques for low-voltage input step-up DC-DC converters with (b) ring oscillator, (c) LC oscillator, (d) transformer-based LC oscillator, and (e) proposed LC oscillator with transformers.

oscillator in Fig. 2(a) [2, 5], it is suitable for the fully integrated converter, since it can be implemented by only CMOS logic gates. The amplitude of V_{CLK} in the ring oscillator, however, is limited to V_{IN}. Another technique for generating V_{CLK} is an LC oscillator in Fig. 2(b) [10]. In this case, the amplitude of V_{CLK} is $2V_{IN}$. To increase the amplitude, a transformer-based LC oscillator in Fig. 2(c) is proposed [8, 9]. When N is the winding turns ratio and the transformer is assumed to be ideal, the amplitude of V_{CLK} is NV_{IN}, In the conventional works [8, 9], the off-chip transformers with N=60 and N=100 are used. Thus,

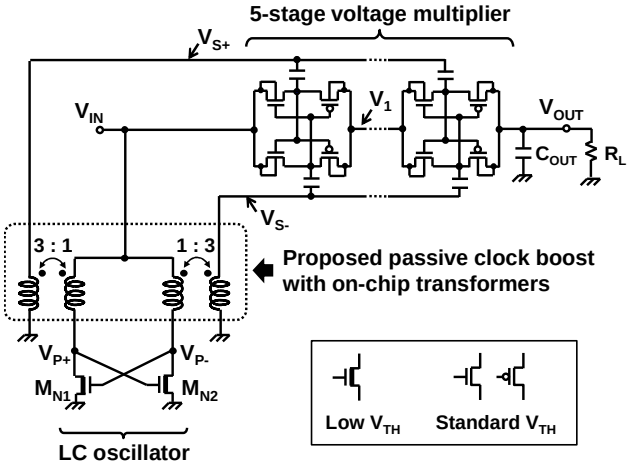


Fig. 3. Circuit schematic of proposed voltage multiplier with passive clock boost using on-chip transformers.

V_{IN} less than 100mV can be directly boosted to above 1.0V. This means the voltage multiplier can be removed. The off-chip transformer, however, is the large overhead in terms of the size and the cost.

To solve the problems, the passive clock boost using on-chip transformers is proposed. Fig. 2(d) shows the LC oscillator and two on-chip transformers for the proposed passive clock boost. By adding two transformers to the LC oscillator shown in Fig. 2(b), the amplitude of V_{CLK} is increased to $2NV_{IN}$. Compared with the transformer-based LC oscillator in Fig. 2(c), the amplitude of V_{CLK} of the proposed Fig. 2(d) is doubled because of the differential outputs. The overhead of the two transformers is alleviated by the on-chip integration. In the on-chip transformer, it is difficult to achieve high winding turns ratio. By using two transformers, the amplitude of V_{CLK} is doubled, which is equivalent to doubling the winding turns ratio. Therefore, the proposed passive clock boost using two on-chip transformers is effective for the fully integrated step-up DC-DC converter.

III. Circuit Implementation

Fig. 3 shows the circuit schematic of the proposed voltage multiplier with passive clock boost using on-chip transformers. 138-MHz clock signal is generated by the LC oscillator operating at V_{IN}. Low threshold voltage (V_{TH}) transistors are used for M_{N1} and M_{N2} of the LC oscillator to increase the transconductance at low V_{IN}, which makes possible V_{START} of less than 100 mV. The clock signals (V_{P+}, V_{P-}) are triply boosted by the proposed passive clock boost assuming the transformers are ideal. The 5-stage cross-coupled MOSFET voltage doublers with boosted clock signals (V_{S+}, V_{S-}) boost V_{IN} to V_{OUT}.

Fig. 4 illustrates the SPICE simulated waveforms of the proposed voltage multiplier. When V_{IN} is larger than V_{START}, the LC oscillator generates the clock signal (V_{P+}). V_{P+} is boosted to V_{S+} by the proposed passive clock boost. The amplitude of V_{S+} (V_{AS}) is N times as large as V_{AP}, where N is the transformation ratio of the transformers. Ideally, N is equivalent to the winding turns ratio of 3. In the actual implementation, N is 2.2 at 138MHz without load based

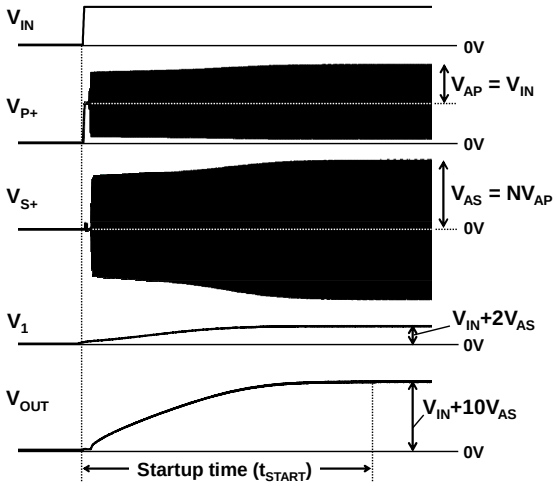


Fig. 4. Simulated waveforms of the proposed voltage multiplier.

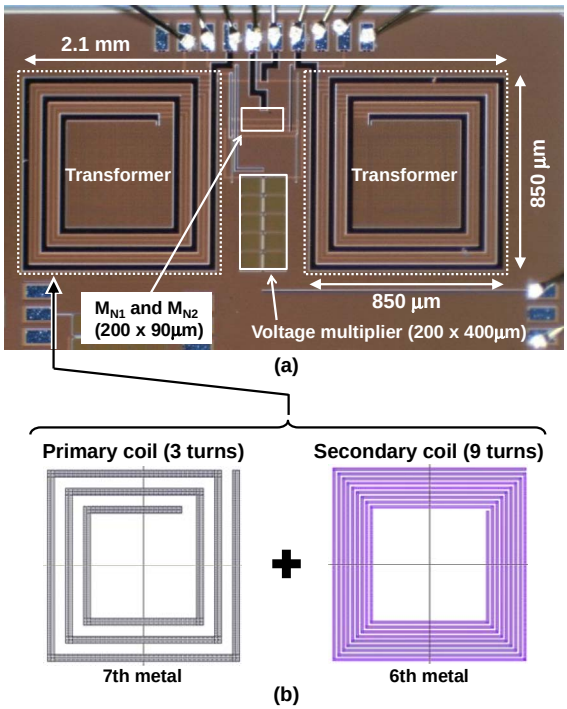


Fig. 5. (a) Chip micrograph and (b) layout of on-chip transformer.

on the electromagnetic simulation (Momentum). The boosted clock signal (V_{S+}) is given to the 5-stage voltage multiplier. The output voltage of the first stage of the voltage multiplier (V_1) is $V_{IN}+2V_{AS}$. Consequently, the output voltage of the 5-stage voltage multiplier is ideally given by

$$V_{OUT} = V_{IN} + 10 \cdot V_{AS} = V_{IN} + 10 \cdot N \cdot V_{IN}. \quad (1)$$

Strictly speaking, V_{AP} is smaller than V_{IN} at low V_{IN} [10], and the voltage drop is caused by the transistors of the voltage doubler. Thus, actual V_{OUT} is less than that calculated by (1)

Fig. 5(a) shows a die photo of the proposed voltage multiplier with the passive clock boost using on-chip transformers. The chip is fabricated in a 65-nm CMOS process

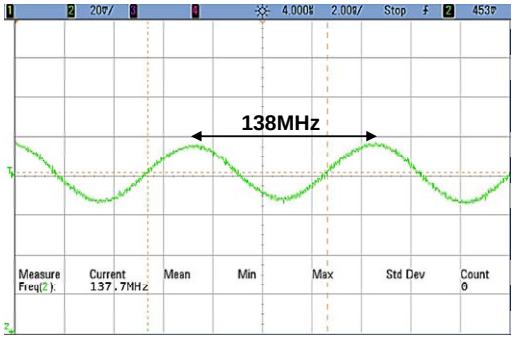
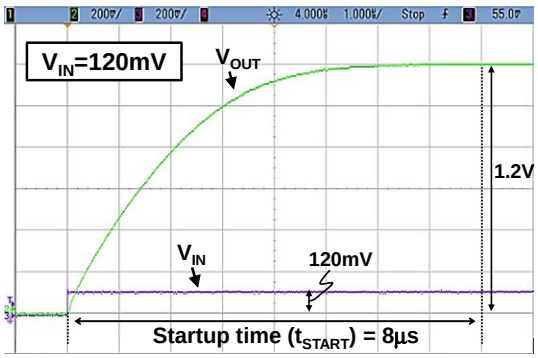
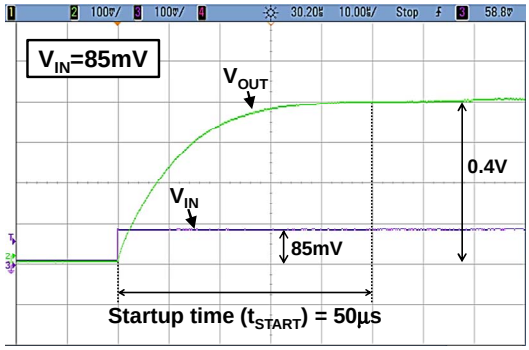


Fig. 6. Measured output waveform of LC oscillator (V_{P+}) in Fig. 3.



(a)



(b)

Fig. 7. Measured startup waveform when R_L is 1MΩ at (a) V_{IN}=120mV and (b) V_{IN}=85mV.

with 7 metal layers. The size of the transformer is 850µm square. The core area including the two transformers is 2.1mm x 0.85mm and the active area excluding the transformers is 0.1mm^2. Fig. 5(b) shows a layout of the on-chip transformer with the 3-turn primary coil at the 7-th (top) metal layer and the 9-turn secondary coil at the 6-th metal layer. The inductances of the primary and secondary coils are 8.5 and 80 nH, respectively.

IV. Measurement Results

Fig. 6 depicts the measured waveform of V_{P+} (Fig. 3). The measured frequency of the LC oscillator is 138MHz. It should be noted that the amplitude of the measured V_{P+} is reduced due to the output buffer. The measured power consumption of the LC oscillator is 280µW and 680µW at V_{IN} of 85mV and 120mV, respectively. Fig. 7 shows the measured startup waveforms at V_{IN}=120mV and V_{IN}=85mV when the load

TABLE I COMPARISON WITH CONVENTIONAL LOW-VOLTAGE INPUT STEP-UP DC-DC CONVERTERS

	LTC3108 [8]	JSSC13 [10]	ASP-DAC12 [2]	ISSCC14 [3]	This work
External components	1 transformer	4 inductors	None (Fully integrated)		
Voltage step-up mechanism	Transformer	Boost converter	Voltage multiplier		Voltage multiplier with passive clock boost
CMOS process	NA	65 nm	65 nm	130 nm	65 nm
Die area	NA	1.0 mm^2	0.78 mm^2	0.066 mm^2	1.8 mm^2 (Active area: 0.1 mm^2)
Minimum startup voltage (V_{START})	20mV	50mV	120mV	180mV	85mV
Frequency of boost converter or voltage multiplier	NA	25 kHz	1 MHz / 20 MHz	250 kHz	138 MHz
Startup time (t_{START})	NA	6ms (*1) (@ V_{IN}=100mV)	NA	NA	8µs (@ V_{IN}=120mV) 50µs (@ V_{IN}=85mV)
Maximum output power	600 µW (@ V_{IN}=500mV)	280 µW (@ V_{IN}=100mV / V_{OUT}=1.2V)	3 µW (@ V_{IN}=120mV / V_{OUT}=0.77V)	10 µW (@ V_{IN}=180mV / V_{OUT}=0.5V)	10 µW (@ V_{IN}=120mV / V_{OUT}=0.77V)
# of stages of voltage multiplier (@ no load)			10 (V_{IN}=120mV → V_{OUT}=1.0V)	3 (V_{IN}=180mV → V_{OUT}=0.62V)	5 (V_{IN}=120mV → V_{OUT}=1.2V)

(*1) Estimated from measured waveform

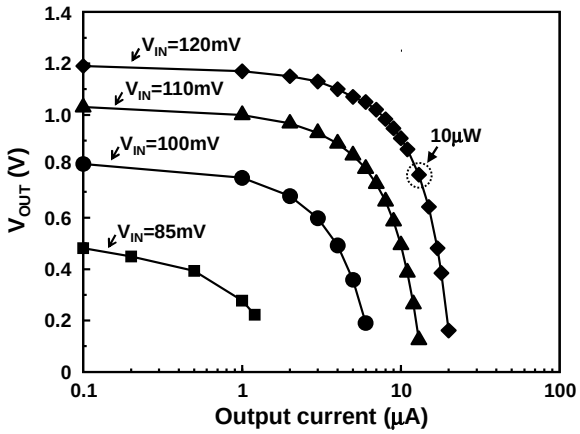


Fig. 8. Measured dependence of V_{OUT} on output current.

resistance (R_L) is 1MΩ and the output capacitance (C_{OUT}) is 10pF (Fig. 3). When V_{IN} is 120mV (Fig. 7(a)), V_{OUT} is 1.2V and t_{START} is 8µs. The lowest V_{IN} (=V_{START}) is 85mV. In this case (Fig. 7(b)), V_{OUT} is 0.4V and t_{START} is 50µs. Fig. 8 shows the measured dependence of V_{OUT} on the output current with varied V_{IN}. The maximum output power is 10µW when V_{IN} is 120mV and V_{OUT} is 770mV.

In Table I, this work is compared with the previously published step-up DC-DC converters for the energy harvesting. Though the transformer-based LC oscillator [8] and the boost converter [10] achieve V_{START} of less than 50mV, they require the off-chip components (transformer or inductors). In contrast, this work provides the fully integrated solution. Compared with the previously published fully integrated voltage multipliers [2, 3], this work achieves the lowest V_{START} of 85mV thanks to the proposed passive clock boost. Compared with [2] in the same 65-nm CMOS process and the same V_{IN} of 120mV, the maximum output power is increased from 3µW to 10µW thanks to the proposed passive clock boost, though the number of the stages of the voltage multiplier is reduced from 10 to 5. t_{START} of this work is less than 1/1000 of [10] and the shortest in the published low-voltage input step-up DC-DC converters thanks to the high clock frequency of 138MHz.

V. CONCLUSIONS

In this paper, the fully integrated voltage multiplier with low V_{START} and the fast startup was proposed for the energy harvesting. The proposed passive clock boost using the two on-chip transformers achieved the lowest V_{START} of 85mV in the published fully integrated voltage multiplier. The high frequency (138MHz) clock generation with the LC oscillator enables the shortest startup time of 50µs and 8µs at V_{IN} of 85mV and 120mV, respectively, in the published low-voltage input step-up DC-DC converters.

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