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Design Guidelines of Steep Subthreshold TFET to Minimize Energy of Logic Circuits

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Abstract

A tunneling field effect transistor (TFET) attracts attention, because TFET circuits can achieve better energy efficiency than conventional MOSFET circuits. Although design issues, such as the minimum operatable voltage (V_{DDmin}), in ultra-low power MOSFET logic circuits, have been investigated, V_{DDmin} for TFET logic circuits have not been discussed. In this paper, V_{DDmin} of TFET logic circuits is evaluated for the first time, and based on the evaluation, the design guideline is presented for the device engineers of TFET's that the within-die threshold voltage variation should be reduced as the subthreshold swing becomes steeper.

1. Introduction

A tunneling field effect transistor (TFET) is drawing attention with the expectation that a TFET circuit provides better energy efficiency than a normal MOSFET counterpart by reducing leakage in ultra-low supply voltage (V_{DD}) domain [1]. Fig. 1 shows calculated power-delay (PD) product, that is, the energy of TFET and MOSFET logic circuits. ξ is an effective time ratio and normally around 10^{-3} for logic [2]. V_{OPT} is the voltage at which the energy is minimized, and V_{OPT} of TFET logic circuits is 0.1V as indicated in Fig. 1. Thus, the circuit must be operated at V_{DD}=V_{OPT} to achieve the maximum energy efficiency. However, such ultra-low V_{DD} operation could cause functional errors. A minimum operatable voltage (V_{DDmin}) is the lowest voltage at which these functional errors do not occur [3]. When V_{DDmin} is higher than V_{OPT}, minimum energy operation is not achieved. Therefore, investigations on V_{DDmin} are essential for ultra-low V_{DD} TFET logic circuits. Although variations in TFET devices have been analyzed in [4], it is not clear how such variations affect V_{DDmin}. In this paper, V_{DDmin} of TFET logic circuits due to the within-die threshold voltage (V_{TH}) variation (σ_{VT}) is investigated for the first time, and based on the investigation, the design guideline for TFET circuits is presented.

2. TFET model used for simulation with V_{TH} variability

To perform TFET circuit investigation under V_{TH} variability, a device model is needed. A measured Si TFET device as an example is shown in Figs. 2 and 3. A compact model is elaborated and is implemented as a SPICE Verilog-A model, whose calculation result is shown in Fig.4 and shows good agreement with the measurement [5,6]. Discrepancy in very low current region is due to the gate leakage but the region is not used in the simulations in this paper. With this manufactured device, however, it is impossible to achieve steep-S feature at ultra-low V_{DD} region. Thus, in the simulation below, a work function parameter is modified and Si is changed to Ge to enable low V_{DD} operations. The resultant I_{DS}-V_{DS} characteristics which are used in this paper are shown in Fig. 5.

I_{DS}-V_{GS} characteristics in Figs. 5 (c) and (d) show the cases when V_{TH} is shifted by ±30mV through changing the work function parameter. The exact physical origin of the V_{TH} variation is not in focus here but rather the existence of the V_{TH} variation is important since V_{TH} changes the current exponentially, which in turn affects the circuit behavior strongly. The compact model, being different from a table model, enables the V_{TH} variability simulation.

3. Minimum operatable voltage (V_{DDmin}) of logic circuits

The closed-form expression for estimating V_{DDmin} for MOSFET logic circuits has been proposed in [3]. Since I-V characteristics of TFET's in low V_{DS} region differ from those of conventional MOSFET's, an approximate expression of I_{DS} characteristics of TFET's is introduced and shown in Fig. 6 to derive V_{DDmin} expression for TFET logic circuits. Strictly speaking, S has voltage dependence in TFET as shown in Fig. 6. However, the voltage dependence is small at ultra-low V_{DD}. Hence, S is approximated as an average over 0V and 0.1V. The derived V_{DDmin} expression for TFET logic circuits is shown in Fig. 7.

Fig. 7 shows V_{DDmin}'s of TFET inverter chains obtained by Monte Carlo simulations with the compact model and by the V_{DDmin} expression. Monte Carlo simulations to obtain V_{DDmin} in this paper comply with the procedure described in [3]. The coincidence of theory and simulation show the validity of the approximation illustrated in Fig. 6. The V_{DDmin} dependence of TFET logic circuits on the number of gates and σ_{VT} is same as that of MOSFET logic circuits. The derivation is based on inverters but it was shown that the expression works well with NAND's and NOR's [3].

In order to achieve minimum energy operation, circuits must be functional at V_{OPT}, that is, V_{DDmin} is less than V_{OPT}. The expression of V_{OPT} for conventional MOSFET circuits has been derived in [7]. In this paper, V_{OPT} for TFET logic circuits is derived by using the approximate I_{DS} characteristics of TFET's shown in Fig. 6. From the expressions of V_{DDmin} and V_{OPT}, $\sigma_{VT,max}$, which is the maximum σ_{VT} for V_{DDmin}<V_{OPT}, is derived. Fig. 8 shows $\sigma_{VT,max}$ for 1M and 10B-gate logic circuits, which indicates that V_{TH} variation

must be reduced as S becomes steeper. With TFET technology described in this paper (S=30mV/dec), $\sigma_{VT,max}$ is 15mV for 1M-gate logic circuits, that is, σ_{VT} has to be controlled within 15mV to achieve operation at V_{OPT} of 0.1V.

Acknowledgements

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References

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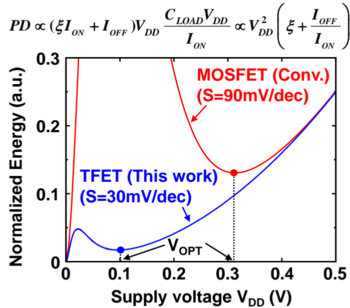


Fig. 1. Energy of TFET circuits. ξ is effective time ratio.

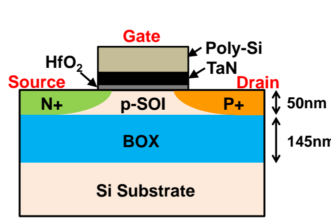


Fig. 2 Cross-section of p-type TFET (pTFET).

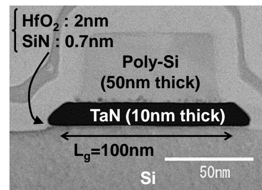


Fig. 3 Cross-sectional TEM image of pTFET.

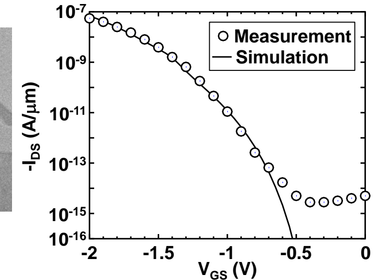
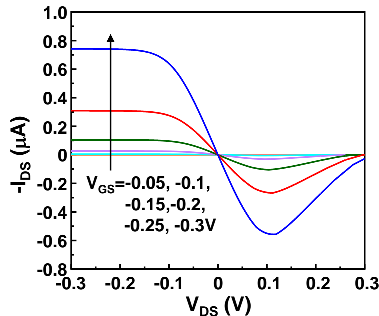
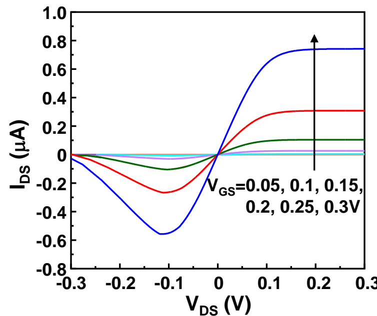


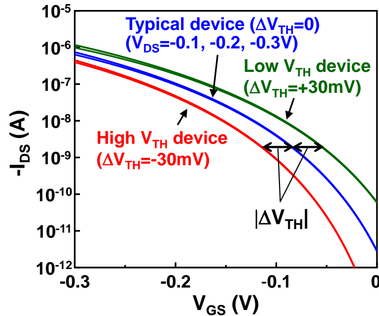
Fig. 4 Measured and simulated characteristics of pTFET.



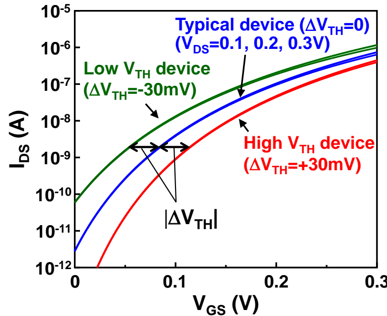
(a) I_{DS}-V_{DS} characteristics of pTFET



(b) I_{DS}-V_{DS} characteristics of nTFET



(c) I_{DS}-V_{GS} characteristics of pTFET



(d) I_{DS}-V_{GS} characteristics of nTFET

Fig. 5. I-V characteristics of p-Type TFET (pTFET) and n-type TFET(nTFET). ΔV_{TH} represents V_{TH} shift from center value due to V_{TH} variation.

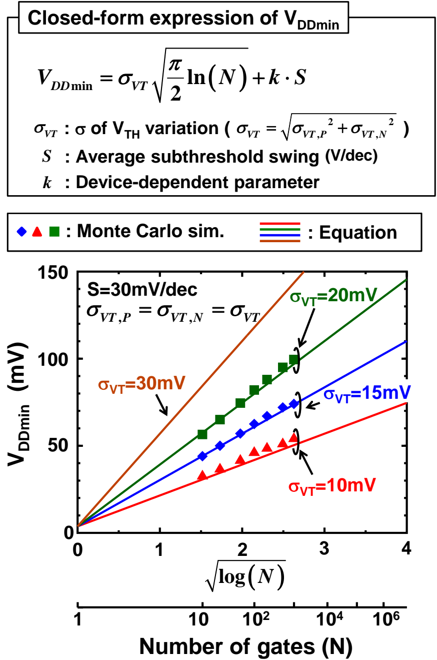


Fig. 7. V_{DDmin}'s of TFET inverter chains obtained by Monte Carlo simulations and closed-form expression.

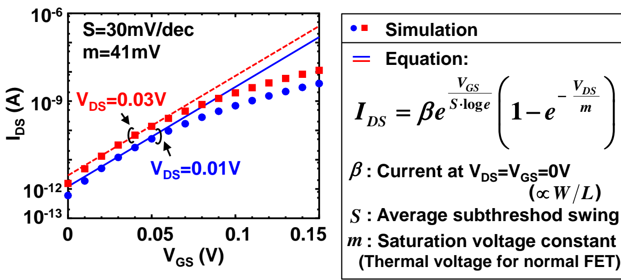


Fig. 6. Comparison of I_{DS}-V_{GS} characteristics of nTFET obtained by simulations with compact model and calculated by equation used to derive closed-form expression of V_{DDmin} shown in Fig. 7.

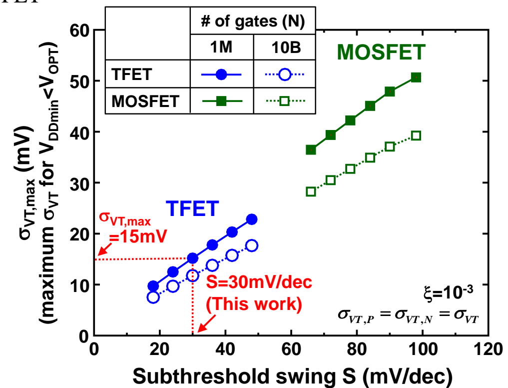


Fig. 8. Dependence of $\sigma_{VT,max}$, which is maximum σ_{VT} for $V_{DDmin}<V_{OPT}$, on subthreshold swing S for logic circuits ($\xi=10^{-3}$). For MOSFET, it is assumed that the strengths of pMOS and nMOS are perfectly balanced.